SPECTRA 02

PRODUCT REFERENCE MANUAL

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SPECTRA MULTIFUNCTION TEST PANEL

The Spectra Multifunction Test Panel is an improved version of the original board and is a test tool for use with all Spectra controllers. Attachment to the controller is made through a 20 pin flat ribbon cable. The controller has a 20 pin test socket for each microprocessor, i.e. disk section and host CPU section. The test panel should be connected to the appropriate test socket depending upon which microprocessor is to be examined. To determine which test socket is associated with which microprocessor, refer to the controller's logic diagram.

The test panel is able to halt the microsequencer and step through the firmware while displaying the addresses. Or it can store the information in trace memory and read it out later. The board has 256 words (16 bits) of trace memory with selectable pre-or post-trigger. That is, an address, data pattern, or combination of both can be selected and a switch can be set such that the trace stops with the match condition. This can all be done without halting or otherwise affecting the processor.

A 20 pin dip clip can be connected via cable to the test panel. The dip clip is used to look at data or other signals on a controller. It is possible to breakpoint on any of these signals, to input any sixteen lines into the trace buffer, and to display all 20 signals on the LEDs.

The display consists of two rows of 11 LEDs, a row of 4 LEDs, a RUN LED, power ON LED, and breakpoint MATCH LED. The upper row will be multiplexed between the next address, trace buffer address, and dip clip pins 1 to 10. The bottom row will display the current address, trace buffer data, and dip clip pins 11 to 20. The row of four LEDs can be connected to the dip clip so that other signals may be monitored while tracing microword addresses. The displays are selected by a three position switch.

A jumper will select whether the breakpoint MATCH LED is latched or not. Another jumper can be inserted to issue a RESET only on address match. If switch clock and stop clock logic is not available on the controller, this is sensed by the test panel and supplied.

The following is a description of the switch and display functions of the test panel and how to use them.

SWITCH	FUNCTION
ADDRESS COMPARE	The three thumbwheel switches are used to set a hexadecimal address of a specific microword which will be compared against the current address being executed. The rightmost switch is the least significant hex digit. When a match occurs the MATCH LED is lit. If CPU BKPT is also on when a match occurs, the sequencer halts.
DISP AD/DC/TR	DISP AD (up position) displays the next address on the upper row and current address on the lower row of LEDs. DISP DC (center position displays dip clip pins 1-10 on the upper row and pins 11-20 on the lower row of LEDs. DISP TR (down position) displays the trace buffer address (00-FF) on the upper row and the trace contents on the lower row of LEDs.
LAMP TEST	Verifies that all LEDs will light.
PRE TRIG	When the switch is in the up position, Post Trigger is in effect. Upon breakpoint match Post Trigger will halt the trace address counters. The trace buffer will contain the 255 words prior to the breakpoint. When PRE TRIG is set, (down position), a breakpoint match will start the trace address counters at 00 and they will count up to FF. Thus the trace buffer will contain the 255 words following the breakpoint.
TRACE READ	When the switch is in the up position it allows writing into the trace buffer. TRACE READ allows a read.
TRACE DC	The switch in the up position determines that a microword address will be written into the trace buffer. TRACE DC writes data from the dip clip.
STEP TRACE	Allows stepping through contents of trace buffer when in trace read mode.
CNT DOWN	Determines whether the trace address counters will count up or down.

SWITCH	FUNCTION
CPU BKPT	Causes the microsequencer and trace to halt after a match occurs between the address set into the thumbwheel address compare switches and the current address being executed. The sequencer will halt either prior to executing the instruction whose address is on the thumbwheel switches, or after the instruction is executed, depending on the phase of the clock on which the sequencer is set to stop. If the dip clip is selected, the comparison is between the data on the dip clip and the pattern set into the dip switches. When this switch is in the up position the trace will halt at breakpoint without affecting the CPU.
CYCLE	Causes a reset and restart to occur based on single shot time-out. Time-out is adjustable by variable resistor T1.
RESET	Causes the microprocessor and sequencer to be reset. Microprogram starts at location zero.
HALT	Causes the microprocessor and sequencer to halt at the end of the current instruction being executed in the pipeline register.
START	Causes the microprocessor and sequencer to start executing microcode. If the HALT switch is set, then START acts as a single instruction cycle switch. START also resets the trace circuitry and the match latch.
SW CLK	Inverts clock phase when clock is stopped. Only active when attached controller has no stop clock logic.
CLK INV	Causes the clock from the controller to be inverted coming into the test panel.
SW1 (Dip Switch 2C)	Dip Clip bits 1-10 go via SW1 to one side of a comparator.
SW2 (Dip Switch 2D)	SW2 forces the inputs to the other side of the comparator low or high when closed or open. (Bits 1-10)
SW3 (Dip Switch 2B)	Dip Clip bits 11-20 go via SW3 to one side of a comparator.
SW4 (Dip Switch 2A)	SW4 forces the inputs to the other side of the comparator low or high when closed or open. (Bits 11-20)

LED	FUNCTION
ON	Indicates power is on; 5V power is supplied through cable from controller.
RUN	Indicates the microprocessor is cycling.
MATCH	Indicates an address match occurred between the hex address set into the address switches and the current address being executed, or a match between the dip switches and the signals on the dip clip. (Depending upon the mode of operation).
A,B,C,D	Displays the four most significant bits of trace memory. The dip clip inputs to these locations may be connected at jumpers WA,WB,WC, and WD. (A write to these locations is performed whenever a write to trace memory occurs. This allows a simultaneous trace of microword addresses and four bits from the dip clip.)
NA 0-11	Indicates the next microword address to be executed. (DISP AD)
CA 0-11	Indicates the current microword address being executed. (DISP AD)
DC 1-10	Displays dip clip pins 1-10 (DISP DC)
DC 11-20	Displays dip clip pins 11-20 (DISP DC)
TA 0-7	Displays trace buffer address (00-FF). (DISP TR)
TD 0-11	Displays contents of trace buffer. (DISP TR)

CONNECTOR	FUNCTION
J1	20 pin header used to connect the test panel to the controller.
J2	26 pin header used to connect the test panel to the dip clip.

JUMPER	FUNCTION
W1	When inserted this jumper latches the breakpoint MATCH LED. START resets it.
W2	W2A allows normal CYCLE operation. When in CYCLE mode W2B allows a reset to occur only upon an address match.
W3	W3A determines that a breakpoint will occur on address match. W3B determines that a breakpoint will occur on dip clip data match. When W3 is open, a breakpoint will occur only when both conditions are true.
W4-W7	Connects dip clip data bits 1 or 2, 9 or 10, 11 or 12, and 19 or 20 to the comparators. See Table 1.
WA-WD	Determines what dip clip data bits will be stored in the four most significant bits of trace memory. These bits are displayed on the LEDs labeled A,B,C,D. WA-WD may be connected to any of the dip clip pins via the wirewrap pins labeled 1-20.

TEST POINT	FUNCTION
CYCLE RESET	The RESET pulse at this point can be observed while adjusting T1 to establish the time-out duration when using the CYCLE switch.
MATCH HI	This point will be a logical one when a match condition occurs.
GND	Logic ground.

POST-TRIGGER

In this mode the 255 addresses preceding the breakpoint address are stored in the trace memory.

All switches should be in the up position except DISP TR. If CPU BKPT is set, the CPU as well as the trace circuitry will halt at the breakpoint. Otherwise the CPU will not be affected. Set the desired address in the strip switches. Hit START to reset the breakpoint circuitry. Watch the MATCH LED to see when the breakpoint is reached; jumper W1 may be inserted to latch MATCH LED if necessary. After the breakpoint occurs set TRACE READ and CNT DOWN. Use STEP TRACE to decrement the trace buffer address and examine the contents of trace memory. The upper row of LEDs (TA) display the trace buffer address. The lower row (TD) displays the contents of trace memory, which will be the breakpoint address and preceding addresses. The breakpoint address may be stored in any location in trace memory. It is useful to note this address after the breakpoint has occurred.

PRE-TRIGGER

In this mode the 255 addresses following the breakpoint address are stored in the trace memory.

All switches should be in the up position except DISP TR and PRETRIG. If CPU BKPT is set, the CPU as well as the trace circuitry will halt at the breakpoint. Otherwise the CPU will not be affected. Set the desired address in the strip switches. Hit START to reset the breakpoint circuitry. Watch the MATCH LED to see when the breakpoint is reached; jumper W1 may be inserted to latch MATCH LED if necessary. After the breakpoint occurs set TRACE READ. Use STEP TRACE to increment the trace buffer address and examine the contents of trace memory. The upper row of LEDs (TA) displays the trace buffer address. The lower row (TD) displays the contents of trace memory, which will be the breakpoint address and following addresses. The breakpoint address will be contained in trace memory address 0.

SETTING DATA BREAKPOINT

In this mode it is possible to breakpoint on any combination of signals from the dip clip.

The breakpoint must be selected. Bits 3-8 and 13-18 are hardwired. One bit of each of the bit pairs 1 or 2, 9 or 10, 11 or 12, and 19 or 20 can be selected (see Table 1) for a possible total of 16 bits. Each of the 16 bits has two switches associated with it on either SW1 and SW2 or SW3 and SW4 (see Table 2). SW1 and SW3 are tied directly to the dip clip. SW2 and SW4 are connected to the other side of the comparators and force the input low when closed or high when open. Thus when both switches for a bit are open that bit is a don't care. When a switch on SW1 or SW3 is closed a match will occur when that bit is low or high when the same switch on SW2 or SW4 is closed or open, respectively. W3B must be jumpered to allow a breakpoint on dip clip data match. The toggle switches can be set for the desired breakpoint as described in PRE or POST TRIGGER. The only difference is that TRACE DC should be set.

JUMPER	BIT
W4A	1
W4B	2
W5A	9
W5B	10
W6A	11
W6B	12
W7A	19
W7B	20

Table 1

BIT	SW1 (2C)/SW2 (2D)	BIT	SW3 (2B)/SW4 (2A)
1/2	1	11/12	1
3	2	13	2
4	3	14	3
5	4	15	4
6	5	16	5
7	6	17	6
8	7	18	7
9/10	8	19/20	8

Table 2