SPECTRA LOGIC CORPORATION
1227 INNSBRUCK DRIVE
SUNNYVALE, CALIFORNIA 94086

408 744-0930
TWX 910 339-9566
TELEX 172524 SPL SUVL

SPECTRA 20

PRODUCT REFERENCE MANUAL

SPECTRA LOGIC

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1.0 GENERAL INFORMATION

1.1 INTRODUCTION

The SPECTRA 20 is the industry's first multifunction disk and tape controller for Data General computers. The SPECTRA 20 is contained on a single DG compatible board and attaches both industry standard formatted tape drives and SMD disk drives. The SPECTRA 20 provides the long awaited solution to the Winchester disk back-up problem by providing a cost effective controller able to attach both disks and 1/2" tape drives. The SPECTRA 20 allows the user to use industry standard 1/2" tape thereby maintaining Data General (and IBM) tape compatibility.

When utilizing 80MB SMD drives and formatted tape drives, emulation of both the DG 6067 disk and 6021 tape subsystems is provided. In addition to these two emulating functions, the SPECTRA 20 provides unique functions not offered by Data General. Among these is the ability to support both "streaming" and "start/stop" tape drives.

The SPECTRA 20 can be operated in either DG software transparent (unmodified) mode or enhanced capability mode which utilizes parameter changes to the DG RDOS/AOS software. These optional parameter changes may be used to provide additional capacity or performance features.

1.2 FEATURES

1.2.1. Performance

The SPECTRA 20 has many important performance features:

1.2.1.1. 11 bit burst Error Correction Code (ECC), with local buffer correction of data transparent to system software.

1.2.1.1. Overlapped Seek to improve access time.

1.2.1.3. Three sector data buffer of 1536 bytes to eliminate "data lates".

1.2.1.4. A data channel throttle control providing a switch selectable burst of 1 to 256, with the host microprocessor fixing the "Off Channel" time in firmware. Up to 256 words are transferred consecutively, then a fixed period of time is observed before generating additional data requests to allow data channel access by other devices.

1.2.1.5. Multiple sector transfers up to 8K words per read or write command to avoid lost disk rotations.

1.2.2. Single Printed Circuit Board - The SPECTRA 20 occupies only one slot in the DG Nova/Eclipse®. The single board design provides cost savings in chassis, power, ease of maintenance, spares, and enhanced reliability.

1.2.3. Full Emulation - The SPECTRA 20/A is transparent to standard RDOS and AOS operating system software and is also diagnostic compatible. Emulation of both the DG 6067 disk and 6021 tape subsystems is provided by the SPECTRA 20/A when used with 80MB SMD disk and formatted tape drives.

1.2.4. System Compatibility - The SPECTRA 20 is compatible with all models of Data General Nova/Eclipse® systems or equivalents.

1.2.5. Disk Drive Attachment - Up to four 80MB SMD compatible drives may be attached to the SPECTRA 20 without any modification to the operating system. SMD drives of any capacity may be attached through the expanded emulation mode. Either removable media, fixed Winchester, or combination fixed/removable drives may be attached.

1.2.6. Tape Drive Attachment - Controls two of any combination of 9 track NRZI/PE industry standard Pertec compatible "formatted tape transports". Each "formatted transport" further allows daisy chain attachment of up to three additional NRZI/PE tape transports for a total of 8 tape transports on one SPECTRA 20. This includes both standard 1/2" start/stop and lower cost streamer tape drives (i.e.; Cipher and Kennedy tape streamers).

1.2.7. Advanced Architecture - Dual bipolar microprocessors provide separate and dedicated control over both host/tape and disk interfaces. This architecture allows the disk and tape to perform as if they had separate, dedicated controllers.

1.2.8. Reliability and Maintainability - The SPECTRA 20 provides high reliability through a single PCB, use of pretested IC's, and elimination of multi-PCB interconnections and power supplies. On-board self-test microdiagnostics provide simple diagnosis, and LED's aid in fault isolation. In addition, system level diagnostics may be used to verify controller operations.

1.2.9. System Features - Expanded Mode

The SPECTRA 20 is the first product in the industry to combine both disk and tape control functions onto a single DG compatible board. In addition, the SPECTRA 20 accommodates suitably equipped tape drives in both Start/Stop and Streaming (100 ips) mode. Streaming mode is ideal for use in literal disk copying since the tape continues across the inter-record gap (IRG) at full speed. Other features not provided by Data General include:

1.2.9.1. On The Fly Read/Write - Allows successive Read/Write commands to be issued such that the transport continues across the interrecord gap (IRG) at full speed. See 2.3.1

This modification halves the time required to cross the IRG's.

1.2.9.2. 8 Transport Capability - Attaches a second string of 4 tape transports through use of a formatter address signal (FADI-DOA bit 13).

1.2.9.3. Maximum Memory Address - Standard DG software allows 32K word direct memory addressing during data channel transfers. This option expands memory addressing to 64K during data channel transfers. See 2.3.3.

1.2.9.4. Speed Select or Density Select - A new feature permits switching between high and low speed on "streaming tape drives" using the least significant transport address bit. In addition, 800 bpi NRZI or 1600 bpi PE tape format may be selected using the same feature if the "start-stop" transport has its density select switch set to the "remote" position (if so equipped). See 2.3.2. for details.

The advantage of the new feature is the transparency of software when switching speed or density.

Prior to this enhancement, speed or density switching was provided by the SPECTRA 20 through a special software control; this capability is retained in addition to the new feature.

1.3. FUNCTIONAL CHARACTERISTICS

1.3.1. Disk Control Functional Characteristics

1.3.1.1. Computer Interface - The controller is compatible with any DG Nova/Eclipse® computer interface. Data transfer occurs over the standard or high-speed data channel.

1.3.1.2. Disk Interface - The disk interface is compatible with the industry standard Storage Module Drive flat cable interface. Up to four drives, either utilizing removable or fixed media, may be attached. The control cable is daisy chained to the four drives and the data cables are attached radially to each drive.

1.3.1.3. Software Transparency - The SPECTRA 20 emulates the DG 6067 disk subsystem when using an 80MB SMD and runs RDOS, AOS, IRIS, and BLIS/COBOL without modification.

1.3.1.4. Disk Data Buffering - A 1536 byte (three sector) high speed RAM buffer is provided for buffering data to/from the disk and DG Nova/Eclipse®. The buffer eliminates "data late" conditions and achieves optimum speeds by smoothing the differences in transfer rates between the disk and data channel.

1.3.1.5. Configurations - In addition to the standard DG 6067 emulation, the expanded emulation mode permits attachment of other SMD type drives, including the CMD 9448. The 6060 Series command set is used for both modes, with parameter extensions in the expanded emulation mode. Removable pack SMD disk drives may be mixed with fixed Winchester type SMD compatible drives.

1.3.1.6. Error Detection and Correction - A 32 bit ECC polynomial is used to detect and correct data errors up to 11 onsecutive bits in length. Error detection occurs on the fly, with error correction being performed either transparently within the controller's data buffer or by the Nova/Eclipse® in main memory.

1.3.1.7. Bad Blocks - Bad block or defective sector flagging is provided under standard DG software control.

1.3.1.8. Position Verification - The controller performs automatic position verification by reading and comparing the cylinder, head, and sector numbers contained in the header prior to any non-format read or write operation. An automatic 16 bit CRC check is also performed on the header information to ensure its validity. These two checks eliminate addressing errors.

1.3.1.9. Self-Test - An automatic microdiagnostic self-test is performed upon each power up. In the event an error is detected, an LED is lit.

1.3.1.10. Memory Address Range - The range of memory addressing by the controller for data transfers is Ø to 64K words. Memory mapping is handled by the Nova/Eclipse®.

1.3.1.11. Device Codes - Disk and tape device addresses are switch selectable with 27_8 (disk) and 22_8 (tape) as standard and 67_8 (disk) and 62_8 (tape) as alternates.

1.3.1.12. Interrupt Priority - The disk interrupt priority is jumper selectable between 6 and 7 with 7 as standard. The tape interrupt priority is jumper selectable between 9 and 10 with 10 as standard.

1.3.1.13. Dual Port - As a standard feature, the SPECTRA 20 supports suitably equipped dual ported disk drives.

1.3.2 Tape Control Functional Characteristics

1.3.2.1. Computer Interface - Any Data General Nova/Eclipse® compatible CPU.

1.3.2.2. Tape Interface - Controls two of any combination of 9 track NRZI/PE industry standard Pertec compatible "formatted tape transports". Each "formatted transport" further allows daisy chain attachment of up to three additional NRZI/PE tape transports for a total of 8 tape transports on one SPECTRA 20. This includes both standard 1/2" start/stop and lower cost streamer tape drives (i.e., Cipher and Kennedy tape streamers).

1.3.2.3. Software Transparency - Utilizes standard DG operating system and diagnostic software. Fully emulates the DG 6021 tape subsystem under RDOS/AOS operating systems when attaching formatted transports.

1.3.2.4. Media Compatibility - Provides IBM (industry compatible) 800 BPI NRZI or 1600 BPI PE tape format containing odd parity.

1.3.2.5. Design Architecture - Dual bipolar microprocessors provide separate dedicated control over both the host/tape and disk interfaces. This advanced architecture allows both disk and tape drives to perform as if they had separate dedicated controllers.

1.3.2.6. Tape Data Buffer - A 64 byte FIFO tape buffer is provided in addition to the three sector buffer utilized for disk buffering.

1.3.2..7. Error Checking - Data integrity is provided through Data General compatible error detection methods. For 9 track NRZI format, an odd parity bit is appended to each data byte. Even longitudinal parity for each track is provided by an appended longitudinal parity check character (LRCC). Also appended to the end of each record is an 8 bit byte Cyclic Redundancy Check Character (CRCC). For 9 track PE format, an industry standard odd parity bit is appended to each data byte.

1.3.2.8. Tape Speeds - Attaches any mix of transports with speeds between 12.5 and 125 ips.

1.4. SPECIFICATIONS

1.4.1 Single P.C. Board - The controller is contained on one DC equivalent PCB, 15" x 15", multilayer. The controller mounts in one slot of the CPU or expansion chassis. The embedded single board design saves space, provides high reliability, and ease of maintenance.

1.4.2. Error Display - Two sets of LEDs, one for each microprocessor, display error status for convenient user diagnosis.

1.4.3. Drivers and Receivers - SMD compatible balanced line drivers and receivers assure reliable operation of the disk drives up to 50 feet from the Nova/Eclipse computer.

1.4.4. Cable Connectors - A 60 pin control cable ('A' cable) connector is provided at the edge of the PCB; mates to 30 TWP flat cable.

Four 26 pin data cable (B' cable) connectors are provided at the back edge of the PCB, allowing attachment of up to 4 SMD disk drives; mate to 26 conductor flat shielded ribbon cables. Two 50 pin connectors using flat ribbon cable attach up to two tape formatter; 8 tape drives.

1.4.5. Power - Uses internal +5V at 9 amps, and -5V at .3 amps.

1.4.6. Enviormental - Exceeds all Nova/Eclipse temperature and humidity specifications.

1.5. SPECTRA 20 MODELS

Characteristics	S20/A			20/D
Tape Emulation	DG 6021	DG 6021	DG 6021	DG 6021
Formatted Tape Drives	All Pertec Compatible Cipher F880 Kennedy 6809	All Pertec Compatible Cipher F880 Kennedy 6809	All Pertec Compatible Cipher F880 Kennedy 6809	All Pertec Compatible Cipher F880 Kennedy 6809
Disk Emulation	6067(50MB)	6067(50MB)	6067(50MB)	6067(50MB)
SMD Compatible Drives	CDC 9762 SMD CDC 9733 MMD Ampex 980 Century Data T-82	CDC 9762 SMD CDC 9733 MMD Ampex 980 Century Data T-82	CDC 9766 Ampex 9300 Century Data T302	CDC CMD9448 Ampex DFR-900
Drive Capacity (MB)	80	80	300	32/64/96
Media Type	Removable; Fixed Winchester	Removable; Fixed Winchester	Removable	Fixed- Removable
Emulation Mode	Standard	Expanded	Expanded	Expanded
Sector per Track	24	32	32	32
Track per Cylinder	5	5	19	2/4/6
Cylinder per Drive	815	823	823	823
Sector Size(Bytes)	512	512	512	512
Formatted Capacity (MB)	50.1	67.4	256.4	27.0/53.9/80.9
Disk Firmware Version	A	A	A	D

2.0 INSTALLATION

2.1.0. INSTALLATION PROCEDURES

This section contains the information needed to install a SPECTRA 20 disk controller. The SPECTRA 20 can be installed in any Data General Nova/Eclipse or equivalent. Maintenance personnel should be familiar with both DG hardware and the specific SMD type drive and Mag Tape drive being installed.

2.1.0.1. Inspection

Perform a thorough visual inspection of the SPECTRA 20 P.C.B., SMD interface cables, and Mag Tape interface cables after removal from their shipping container. Note any damage and notify the freight carrier immediately as Spectra Logic's warranty does not cover shipping damage. The damage claim is to be filed through the carrier with its insurance company.

Check for any broken components or bent pins, and ensure that all IC's in sockets are securely in place. DO NOT remove IC's from sockets unless absolutely necessary to re-seat properly. If any are re-inserted, observe correct seating with respect to pin 1 of the socket.

2.1.0.2. Configuration Verification

Ensure the disk device select code is set for 27_8 or 67_8 in the switch at location 12J. Ensure the Mag Tape device select code is set for 22_8 or 62_8 in the switch at location 12M. Set the switches in location 3AA for the operation desired as described in paragraph 2.2.2. Set the switches in location 3K for the configuration of the drive attached; refer to paragraph 2.2.3. Ensure magtape options are selected as required; refer to paragraphs 2.3.1. and 2.3.2.

2.1.0.3. P.C.B. Installation

The SPECTRA 20 P.C.B. is to be installed only after inspection and switch settings are verified. Check the back panel sockets in the slot intended for use to ensure keys will align properly with the slots in the P.C.B.

Prior to insertion, ensure the interrupt priority chain (INTP IN, INTP OUT) on backpanel pins A96 and A95 are connected but not shorted or bypassed on the slot intended for the SPECTRA 20. In addition, check the data channel priority chain (DCHP IN, DCHP OUT) on backpanel pins A94 and A93 to ensure they are also connected but not shorted or bypassed.

After completing the visual inspection, configuration switch check, backpanel preparation, and ensuring that POWER IS OFF, insert the SPECTRA 20 P.C.B. Insertion should be accomplished without forcing it into the backpanel. Once it makes contact with the backpanel connectors, use the P.C.B. extractor levers to "pull" the P.C.B. into a final seating position. If any warpage exists, exert slight pressure above or below the P.C.B. while determining visually if the card edge connectors are aligning properly with the backpanel while pushing into the initial seating position. Ensure the P.C.B. seats fully and components face the same direction as on other boards.

2.1.0. INSTALLATION PROCEDURES (cont.)

2.1.0.4. SMD Cable Installation

The SMD cables are to be connected after installing the SPECTRA 20 in the chassis. Ensure that pin 1 of the cables mates with pin 1 of the P.C.B. Both the 60 pin and the 26 pin cable connectors and the P.C.B. headers have a small arrowhead designating pin 1.

Attach the 60 conductor "A" cable and 26 conductor "B" cable to the headers on the back end of the P.C.B. If less than four drives are to be attached, any of the four headers provided may be used. Attach the two 50 conductor flat cables to headers J6 and J7 on the back edge of the SPECTRA 20 PCB, and the other ends to the edge connectors of the tape formatter PCB. Route the cables out of the chassis neatly, using folds as required. If the chassis is rack mounted, ensure the cables will permit extension of the rack. If multiple disk drives are installed, ensure a "daisy chain" cable is connected between disk drives and a terminator is installed on the last drive. To ensure proper system grounding, a braided gound strap is to be connected from the CPU chassis to the first drive and between the add-on drives.

Note: If the cables are not supplied by Spectra Logic, check for the following:

A. Clean termination of cable into connector with no long wires or shorts. Cable should be cut flush with edge of connector.

B. Ensure the "B" cable shield is connected to ground at both ends.

C. If a shielded "A" cable is used, check that the shield is grounded.

2.1.0.5. Tape Drive Cable Installation

Attach one 50 conductor flat cable to header J6 on the SPECTRA 20 and to P1 of the tape formatter PCB in the drive. Attach one 50 conductor flat cable to header J7 on the SPECTRA 20 and to P2 of the tape formatter.

If the tape drive connectors are not designated as P1 and P2 (Cipher), then ensure J6 attaches to the drive connector containing IW 0-7 signals and J7 to the connector with IRWD, IEOT etc. signals.

2.1.0.5. Power On

Upon completion of the above, power up the system. Ensure no LED's are lit on the SPECTRA 20. You may now proceed to initialize the disk and run diagnostics to verify correct operations. Refter to Appendix B, "troubleshooting checklist" if problems occur.

2.2.0. SPECTRA 20 SWITCHES

2.2.1. Switch A — Location 12J

SW1 — Switch Clock
This switch is used in fault diagnosis during manufacturing. It is used to switch the phase of the clock in which the clock is stopped when used with the Spectra Logic test panel.

SW2 — Not used.

SW3-8 — Disk Device Select 0-5
These switches are used to select the DG device code of the controller. The standard device code is 27 — switches 3, 5 are on; switches 4,6,7,8 are off. The alternate device code is 67 — switch 5 is on; switches 3,4,6,7,8 are off.

2.2.2. Switch B — Location 12M

SW1-2 — Not used.

SW3-8 — Tape Device Select 0-5

These switches are used to select the DG device code of the tape controller. The standard device code is 22—switches 3, 5, 6, and 8 on; switches 4 and 7 off. The alternate device code is 62—switches 5, 6, and 8 on; switches 3, 4, and 7 off.

2.2.3. Switch C Location 3AA

SW1

ECC Buffer Correct
If this switch is off, the DG software will correct any ECC disk errors. If this switch is on, the controller will correct any ECC disk error transparently to the DG software.

SW2-4

Command Decode Options
The DG disk commands STOP DRIVE and WRITE DISABLE may be interpreted by the SPECTRA 20 controller to do other functions for diagnostic aid. The way these commands are interpreted is decided by these 3 switches as shown in the table below:

SW4	SW3	SW2	Stop Drive Command	Write Disable Command
Off	Off	Off	Stop Drive	Write Disable
Off	Off	On	Stop Drive	No-Op
Off	On	Off	No-Op	Write Disable
Off	On	On	No-Op	No-Op
On	—	—	Read w/ECC	Write w/ECC

SW5

Dual Ported Disk Drives
This switch is normally set to OFF. It should be set to ON if any other controllers are attached to dual ported drive(s) cabled to the SPECTRA 20.

SW6-8

Burst Rate
These switches are used to vary the number of words the controller will transfer at its maximum rate before pausing to give lower priority devices a chance to gain access to the Data Channel. The number of words transferred in one burst is as shown below:

SW6	SW7	SW8	
Off	Off	Off	2 words
Off	Off	On	4 words
Off	On	Off	8 words
Off	On	On	16 words
On	Off	Off	32 words
On	Off	On	64 words
On	On	Off	128 words
On	On	On	256 words

2.2.4. Switch D Location 3K

2.2.4.1. For version A or B of the Firmware

Version A is identified by having PROM number 4A20Axx in location 4A, Version B by having PROM number 4E20BXX in location 4E.

SW1-2 Maximum Cylinder Number

The switches should be set according to the maximum cylinder number of the drive attached to the controller as given in the table below:

SW1	SW2	
Off	Off	815 cylinders or less
Off	On	823 cylinders
On	Off	1645 cylinders
On	On	More than 1645 cylinders

For mixed drive configurations, the switches should be set according to the highest cylinder number of any of the drives.

SW3 Maximum Sector Number

If this switch is OFF, the controller assumes there are 24 sectors per track. If this switch is ON, the controller assumes there are 32 sectors per track. NOTE: The disk drive sector count must also be set within the drive. Consult the disk drive user manual. This switch MUST BE off for PRIAM or BASF Drives with 13,440 bytes per track.

SW4-8 Maximum Head Number

These switches should be set to the maximum head number of the drive attached to the controller.

e.g.:

	SW4	SW5	SW6	SW7	SW8
CDC9766=19 heads	On	Off	Off	On	On
CDC9762=5 heads	Off	Off	On	Off	On

For mixed drive configurations, these switches should be set according to the highest head number of any of the drives.

2.2.4.2 For version D of the Firmware

This version is identified by having PROM number 4A20Dxx in location 4A. It will support up to two physical CMD or Lark type disk drives. Each physical drive is divided into two logical drives, one being the fixed part of the media and the other being the removable part.

SW1 Logical to Physical Mapping Option

If SW1 is Off

Logical drive 0 = Physical drive 0, Removable part
Logical drive 1 = Physical drive 0, Fixed part
Logical drive 2 = Physical drive 2, Removable part
Logical drive 3 = Physical drive 2, Fixed part

If SW1 is On

Logical drive 0 = Physical drive 0, Fixed part
Logical drive 1 = Physical drive 0, Removable part
Logical drive 2 = Physical drive 2, Fixed part
Logical drive 3 = Physical drive 2, Removable part

Please note that the physical drives should only have either a 0 or a 2 plug.

SW2 Maximum Cylinder

SW2	
Off	Maximum cylinder number is 815 or less
On	Maximum cylinder number is 823

SW3

SW3	
Off	Maximum sector number is 24
On	Maximum sector number is 32

SW4 CDC Lark Drive (Firmware Rev A6 or above in location 4A)

SW5-8 Maximum Head (Fixed Part)

These Switches should be set to the number of fixed heads in drive attached to the controller.

e.g.:

	SW5	SW6	SW7	SW8
96MB CMD= 5 fixed heads	Off	On	Off	ON
CDC Lark	OFF	OFF	ON	OF

The logical drive number of the removable part has only one addressable head, head 0.

2.3. MAG TAPE OPTIONS

2.3.1. Streamers/On-the-fly Options

The Spectra 20 by default operates in the "On-the-fly" mode. This means that it will terminate any read/write command at the trailing edge of DBY, data busy, and before the selected transport has come to a stop. This allows the software to send a new command and to keep the transport running at a high speed. In the case of streamers, this allows the software the opportunity of sending a new command within the re-instruct window and so avoid re-positioning.

Most transports restrict the acceptance of a new command during this slowing down or re-instruct time to commands of only the same type, i.e. read or write, the same direction and the same transport. In the case of the SPECTRA 20, the firmware itself does this check and if the conditions are not met by the new command the controller will wait until FBY, formatter busy, goes false indicating the previous command has been fully completed. This allows standard software to be run with all types of transports.

If for some reason this option is not required, it is possible to change a link on the controller such that commands will not terminate until FBY goes false. This link is named W7 and is located next to the IC at location 3BB. The square pad is linked to the round pad B on the circuit side of the board by a trace in artwork. To change this link, this trace should be cut and a wire added from the square pad of W7 to the round pad A.

2.3.2. Speed Select/Density Select

A new feature for the SPECTRA 20 is available starting with PCB s/n 0057 to allow switching of speed on streamers or density on dual density transports usingthe least significant transport address bit.

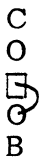
All PCB's prior to s/n 0057 provided the switching capability through a wire link (W9), permitting special software control using DOA bit 9 to select high speed or density. This capability is retained in addition to the new feature, allowing a choice of software transparent speed/density switching by transport address assignment or through the use of special software. SPECTRA STREAM RDOS works with either feature.

By default the SPECTRA 20 will select low density on dual density transports, or low speed on dual speed streaming transports. Density selection will normally be overridden by a switch on the transport itself. The speed/density switching feature prior to s/n 0057 required removal of the SPECTRA 20 from the chassiss and moving a jumper in order to use standard DG software. The new speed/density switching option overcomes this inconvenience by using the least significant transport address bit to perform the switch (when appropriately jumpered) thereby becoming transparent to software other than logical unit assignment.

DOA 9 Speed/Density Switching

When using streaming transports or dual density transports software control of speed select or density select may be performed using DOA bit 9. This bit would be used by standard software to select even parity, which is not used on the SPECTRA 20. In order to do this it is necessary to move the link on W9, located beneath IC's IT and IU. By default the square pad is connected to the round pad B. In order to change this the link should be moved to connect the square pad to round pad C. The transport address Speed/Density Switch feature is to be disabled as described later.

W9 default:



W9 software select:

Transport Address Speed/Density Switching

This feature uses the least significant transport address bit to determine high speed/density or low speed/density selection. With this option installed, even transport addresses (0, 2, etc) will select low speed on streamer transports and low density on dual density transport with the density select switch set to "remote". Odd transport addresses (1,3, etc) will select high speed on streamer transports and high density on dual density transports.

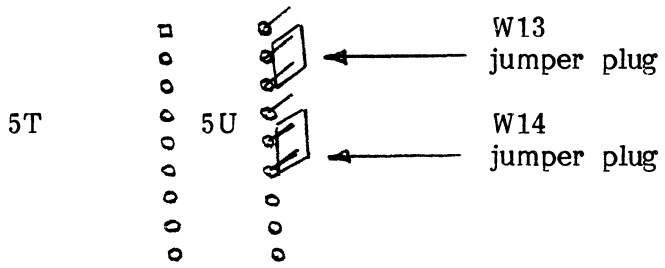
All transports attached to the controller must be set up to respond to even transport addresses.

Example: If two streaming tape drives are to be attached to the controller with this option installed, the transports should be configured as transport 0 and transport 2. The software will then see 4 transports "on line" such that:

Logical transport 0 = Physical transport 0, low speed.
Logical transport 1 = Physical transport 0, high speed.
Logical transport 2 = Physical transport 2, low speed.
Logical transport 3 = Physical transport 2, high speed.

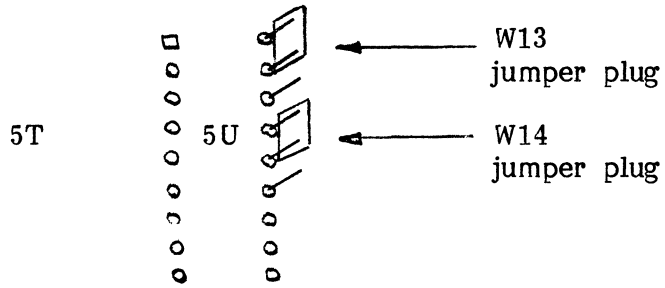
Two new jumpers have been added in location 5U using Flextronic jumper plugs to allow this option to be selected. The SPECTRA 20 will normally be shipped with this option disabled.

Refer to S20 commponent location reference figure.



Component view, option disabled.

With this option disabled, as shown above, the jumper on W9 below location IU has the definition described above under the DOA 9 Speed/Density Switching option. To enable the transport address speed/density switching option, the jumper plugs for W13 and W14 should be moved up as shown below.

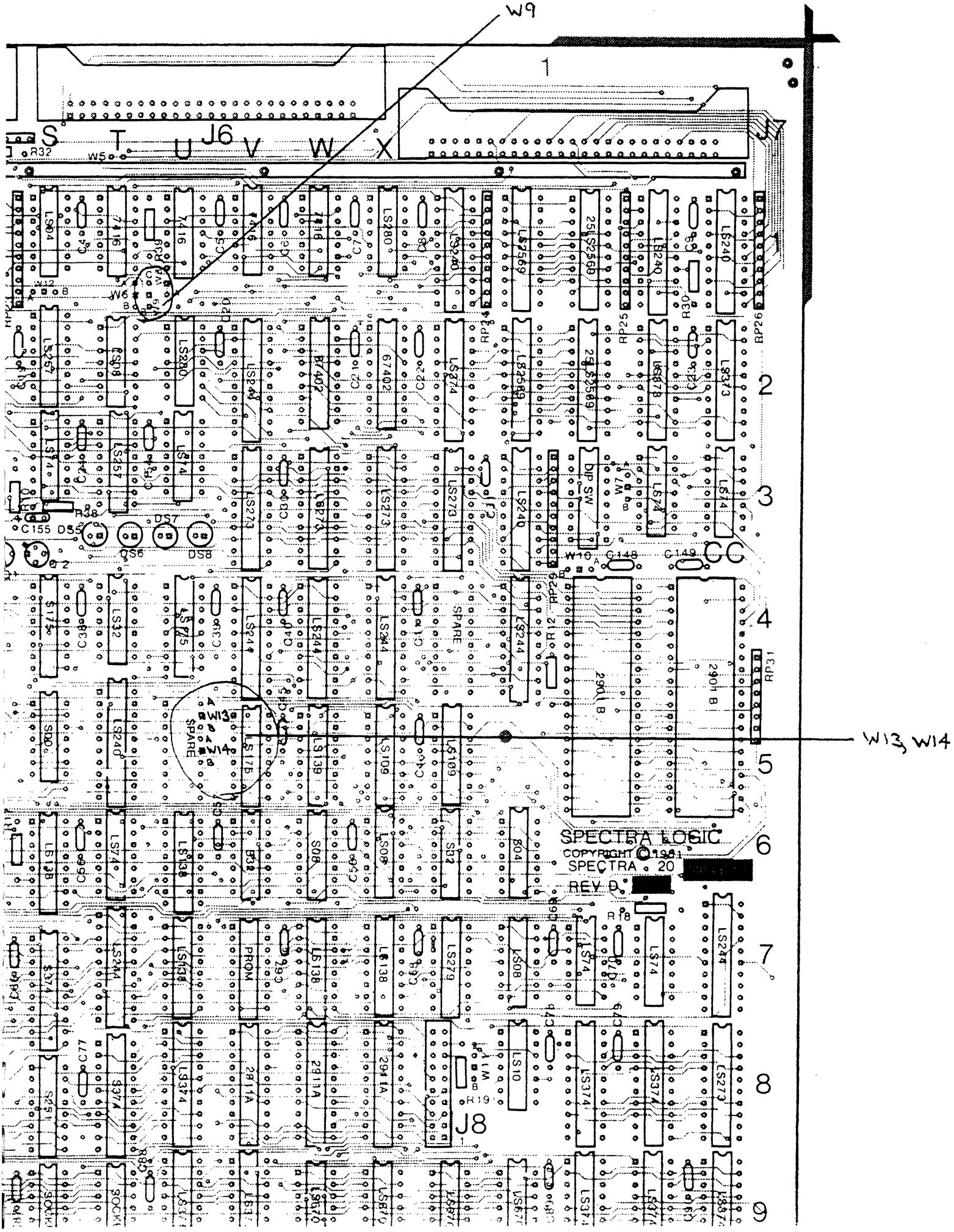


Component view, option enabled.

Note that it is also necessary to have the jumper in W9 below location IU installed such that the square pad is connected to the pad marked "B"; as called out above for the default position under DOA 9 Speed/Density Switching.

2.3.3. Expanded Memory Addessing

Standard software has access to 32K words of memory. Users writing their own software may wish to expand this to 64K words. This may be done by allowing the user to write to bit 0 of the memory address with a DOB command. In order to do this it is necessary to change the link W4 on the PCB. This link is located next to the IC at 11Z. The square pad is by default connected to the round pad B by a trace on the circuit side of the board. This trace should be cut and a wire added from the square pad to the round pad A in order to expand the memory addressing to 64K.


W9
W13, W14
SPECTRA LOGIC
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REV D
[redacted]
J6
J8
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U
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W
X
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7
8
9
SPARE
PROM
DIP SW
2901 B
2911A

3.0 THEORY OF OPERATION

The SPECTRA 20 controller is based on a dual microprocessor design. The CPU processor controls all the software visible registers except for Drive Status, First ECC Word, and Second ECC Word. It is responsible for decoding all commands, initiating commands, Data Channel transfers, and final termination of the commands for both disk and tape. The software visible registers themselves are implemented in hardware, and they are read or written by the DG buss directly by hardware. The hardware ensures that the controller meets the timing limitations imposed by the DG buss. The CPU processor allocates time to the disk and tape units during concurrent data transfer operations. The DISK processor controls the disk interface and the Drive Status, First ECC Word, and Second ECC Word registers.

The two processors communicate with each other via the first 512 bytes of a 2K byte RAM buffer. The rest of this buffer is used to buffer 3 sectors of data between the two processors. This buffer is therefore called the Sector Buffer. In addition, there are two flip-flops used for communication between the two processors. The first one is called GO. This is set by the CPU processor to inform the DISK processor that there is a command to perform. All information pertaining to this command will be available in the Communications Area of the Sector Buffer. When the DISK processor accepts this command, it will reset the GO flip-flop. The second flip-flop is called ATTENTION. This is set by the DISK processor to inform the CPU processor that it has finished a data transfer command and has updated all relevant status conditions. The CPU processor will wait for ATTENTION before completing the termination and setting DONE. It will also reset the ATTENTION flip-flop at this time in preparation for the next command. A 64 byte FIFO is used to buffer data between the formatted tape drive and the CPU.

A common oscillator running at 22MHZ is shared by the two microprocessors. Each microprocessor operates on a clock phase opposite the other. This permits the RAM buffer to be accessed by both microprocessors without contention.

Whenever the SPECTRA 20 does not have a command active, both microprocessors go into idle loops. The CPU microprocessor essentially waits for a new command while the DISK microprocessor polls the four disk drive ports to update and maintain drive status. Any drive switching from a NOT READY to a READY state will cause an appropriate attention flag to set.

3.1 DISK INSTRUCTION FORMATS AND REGISTER DEFINITIONS

3.1.1. Instruction Formats

SPECIFY COMMAND AND DRIVE

R/W DN	CLR SEEK DONE					COMMAND				DRIVE			NOT USED		(DOA)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

SPECIFY CYLINDER

Context: The previous DOA specified a seek operation.

NOT USED										CYLINDER					(DOC)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

SPECIFY SURFACE, SECTOR AND COUNT

Context: The previous DOA did not specify a seek operation.

SURFACE ADDRESS						SECTOR ADDRESS				SECTOR COUNT					(DOC)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ SURFACE, SECTOR AND COUNT

SURFACE ADDRESS						SECTOR ADDRESS						SECTOR COUNT			(DIC)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

SPECIFY MEMORY ADDRESS

EMA LSB	MEMORY ADDRESS													(DOB)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ MEMORY ADDRESS

Context: Alternate instruction mode 1

EMA LSB						MEMORY ADDRESS									(DIA)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ DRIVE STATUS

INV ST	RES	TSP	RDY	BSY	OFF	WR DIS		ILL ADR	ILL CMD	DC FLT	UNS	POS FLT	CLK FLT	WR FLT	(DIB) DRV FLT
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ DATA TRANSFER STATUS

CNT FUL	R/W DN	SEEK DONE				PAR	SEC ADD	ECC	BAD SEC	CYL ADD	SEC SRF	VFY	R/W TIM	DAT LAT	(DIA) R/W FLT
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ FIRST ECC WORD

Context: Alternate instruction mode 2

						FIRST ECC WORD									(DIA)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ MEMORY ADDRESS

Context: Alternate instruction mode 1

EMA LSB						MEMORY ADDRESS									(DIA)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ DRIVE STATUS

INV ST	RES	TSP	RDY	BSY	OFF	WR DIS		ILL ADR	ILL CMD	DC FLT	UNS	POS FLT	CLK FLT	WR FLT	(DIB) DRV FLT
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ DATA TRANSFER STATUS

CNT FUL	R/W DN	SEEK DONE				PAR	SEC ADD	ECC	BAD SEC	CYL ADD	SEC SRF	VFY	R/W TIM	DAT LAT	(DIA) R/W FLT
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ FIRST ECC WORD

Context: Alternate instruction mode 2

					FIRST ECC WORD										(DIA)
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ SECOND ECC WORD

Context: Alternate instruction mode 2

SECOND ECC WORD (DIB)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

S, C, and P Functions

f = S Sets the Busy flag to 1; sets the Done flag to 0. Starts the following operations: READ, WRITE, FORMAT, READ BUFFERS and VERIFY.
f = C Sets the Busy flag and Done flag to 0 and stops all data transfer operations.
f = P Starts the following operation: SEEK, RECALIBRATE, OFFSET, STOP, WRITE, DISABLE, RELEASE, and TRESPASS. (Does not affect the Busy flag or Done flag)

IORST Performs all operations listed under f = C and initiates a recalibrate operation on the lowest numbered ready drive if it is not reserved by the other processor. Clears the sector, sector count, and surface address. Resets the command register to 0000(read).

3.1.2. Disk Register Definitions

SPECIFY COMMAND AND DRIVE

DOA	(f)		ac,		DSKP										
0	1	1	AC		0	1	0	F		0	1	0	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Loads bits 5-8 of the specified accumulator into the controller's command register, loads bits 9-10 of the specified accumulator into the controller's drive select register. Clears the done/attention flags selected by bits 0-4 of the specified accumulator. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The contents of the specified accumulator remain unchanged; its format is as follows:

R/W	CLR	SEEK	DONE		COMMAND				DRIVE		NOT USED				
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0	Clear R/W Done	Clears the status register's read/write Done flag. Clears all the read/write error flags except read/write timeout.
1-4	Clear Atten (0-3)	Clears the drive attention flags for drive 0-3 respectively.
5-8	Command	Specifies the command to be transmitted to the selected drive as follows: 0000 Read 0001 Recalibrate 0010 Seek 0011 Stop Drive 0100 Offset forward 0101 Offset reverse 0110 Write disable 0111 Release 1000 Trepass 1001 Set Alternate mode 1 1010 Set Alternate mode 2 1011 No operation 1100 Verify 1101 Read Buffer 1110 Write 1111 Format
9-10	Drive	Specifies drive 0-3 to be selected.
11-15	Reserved	Not used

SPECIFY CYLINDER
DOC (f) ac, DSKP
Context: The previous DOA specified a seek operation.

0	1	1		AC		1	1	0		F		0	1	0	1	1	1
0	1	2	3	4		5	6	7	8		9	10	11	12	13	14	15

Loads bits 6-15 of the specified accumulator into the controller's cylinder address register. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The contents of the specified accumulator remain unchanged; its format is as follows:

										CYLINDER					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0-5	—	Reserved for future use. Bit 5 is implemented as cylinder 1024 bit.
6-15	Cylinder	Specifies the desired cylinder for a seek operation.

SPECIFY SURFACE,SECTOR AND COUNT
DOC (f) ac, DSKP
Context: The previous DOA did not specify a seek operation.

0	1	1		AC		1	1	0		F		0	1	0	1	1	1
0	1	2	3	4		5	6	7	8		9	10	11	12	13	14	15

Loads bits 1-5 of the specified accumulator into the controller's surface address register, loads bits 6-10 of the specified accumulator into the controller's sector address register, and loads bits 11-15 of the specified accumulator into the controller's sector count register. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The contents of the specified accumulator remain unchanged; its format is as follows:

	SURFACE ADDRESS					SECTOR ADDRESS					SECTOR COUNT				
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0	—	Not used
1-5	Surface	Selects the starting surface (head) for a read, write, format or verify operation.
6-10	Sector	Selects the starting sector for a read, write, format or verify operation.
11-15	Sector Count	Specifies the two's complement of the number of sectors to be transferred in one operation (maximum of 40_8).

READ SURFACE, SECTOR AND COUNT

DIC (f) ac, DSKP

0	1	1		AC		1	0	1		F		0	1	0	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

Places the contents of the controller's surface address register in bits 1-5 of the specified accumulator, places the contents of the controller's sector address register in bits 6-10 of the specified accumulator, and places the contents of the controller's sector count register in bits 11-15 of the specified accumulator. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The format of the accumulator is as follows:

NOT USED	SURFACE ADDRESS				SECTOR ADDRESS						SECTOR COUNT					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

BITS	NAME	MEANING WHEN 1
0	---	Not used
1-5	Surface	Indicates the current surface for a read, write, format or verify operation.
6-10	Sector	Indicates the sector immediately following the last which was transferred.
11-15	Sector Count	Indicates the two's complement of the number of sectors remaining to be transferred.

SPECIFY MEMORY ADDRESS

DOB (f) ac, DSKP

0	1	1		AC		1	0	0		F		0	1	0	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

Loads bit 0 of the specified accumulator into the least significant bit (lsb) of the controller's extended memory address register, and loads bits 1-15 of the specified accumulator into the controller's memory address register. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The contents of the specified accumulator remain unchanged; its format is as follows:

EMA LSB					MEMORY ADDRESS										
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0	Extended Memory address	Specifies the lsb of the extended memory address or the data channel map selection.
1-15	Memory Address	Specifies the starting address for data channel transfers.

READ MEMORY ADDRESS

DIA (f) ac, DSKP
Context: Alternate instruction mode 1

0	1	1		AC	0	0	1		F	0	1	0	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Places the contents of the lsb of the controller's extended memory address register in bit 0 of the specified accumulator, and places the contents of the controller's memory address register in bits 1-15 of the specified accumulator. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The format of the accumulator is as follows:

EMA LSB					MEMORY ADDRESS										
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	MEANING WHEN 1
0	Extended Memory address	Indicates the lsb of the extended memory address or the NOVA 3 map selection.
1-15	Memory address	Indicates the location of the next word in memory for a data channel transfer.

READ DRIVE STATUS

DIB (f) ac, DSKP

0	1	1		AC	0	1	1		F	0	1	0	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Places the drive status flags for the drive selected by the previous DOA in bits 0-6 and 8-15 of the specified accumulator; sets bit 7 to 0. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The format of the accumulator is as follows:

INV ST	RES	TSP	RDY	BSY	OFF	WR DIS		ILL ADR	ILL CMD	DC FLT	UNS	POS FLT	CLK FLT	WR FLT	DRV FLT
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	MEANING WHEN 1
0	Invalid Status	The disk drive is not selected and bits 5-6 and 8-15 should be ignored.
1	Reserved	The drive is reserved by the other processor
2	Trespassed	One of the drives was trespassed upon by the other processor.
3	Ready	The drive is ready to accept commands.
4	Busy	The drive is busy executing a position command or reporting an aborted seek or a trespass by the other processor.
5	Offset	The positioner is offset forward or reverse.
6	Write Disable	The write circuits are disabled.
7	—	Reserved for future use.
8	Invalid address	The surface or cylinder capacity of the drive was exceeded.
9	Illegal command	The drive received an illegal read/write or position command.
10	DC Fault	The disk drive power supply has a DC voltage problem.
11	Disk unsafe	An unsafe condition exists preventing operation.
12	Positioner fault	The head positioner malfunctioned.
13	Clock fault	The servo clock malfunctioned.
14	Write fault	The write or head select circuits malfunctioned.
15	Drive fault	Any of the above faults (bits 8-14).

READ DATA TRANSFER STATUS

DIA (f) ac, DSKP

0	1	1		AC		0	0	1		F		0	1	0	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

Places the contents of the controller's done flags and read/write status flags in bits 0-15 of the specified accumulator. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The format of the accumulator is as follows:

CNT FUL	R/W DN	SEEK DONE				PAR	SEC ADD	ECC	BAD SEC	CYL ADD	SEC SRF	VFY	R/W TIM	DAT LAT	R/W FLT
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	MEANING WHEN 1
0	Control Full	The drive command initiated by the previous IOPULSE or IOREST has not yet been issued to the selected drive.
1	R/W Done	The read/write operation initiated by the previous START has terminated. (This is the same as the device Done flag.)
2-5	Drive 0-3 Done	The respective drives have executed a positioner command, have rejected an illegal positioner command, have been trespassed upon, or have changed their ready status.
6	Parity	A parity error occurred on a data transfer between the controller and the adapter. Not used.
7	Illegal sector	The sector address exceeded the capacity of the drive.
8	ECC	A data error was detected by the ECC circuits.
9	Bad sector	A bad sector flag was detected during a sector header check.
10	Cylinder error	A cylinder address error was detected during a sector header check.
11	Surf/sect error	A surface or sector address error was detected during a sector header check.
12	Verify error	A data error was detected during a verify operation.
13	Read/write timeout	The read/write operation initiated by the previous START was not completed in 1 second.
14	Data late	The FIFO overflowed during a read or underflowed during a write.
15	Read/write fault	Any of the above faults or a drive fault on the drive currently selected by the read/write channel.

READ FIRST ECC WORD

DIA (f) ac, DSKP

0	1	1		AC		0	0	1		F		0	1	0	1	1	1
0	1	2	3	4		5	6	7	8	9		10	11	12	13	14	15

Places bits 0-15 of the controller's ECC remainder register in bits 0-15 of the specified accumulator. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The format of the accumulator is as follows:

FIRST ECC WORD

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	MEANING WHEN 1
0-15	a_{31}-a_{16}	Indicates the coefficients of the high order bits of the ECC remainder following a read operation.

READ SECOND ECC WORD

DIB (f) ac, DSKP

Context: Alternate instruction mode 2

0	1	1		AC		0	1	1		F		0	1	0	1	1	1
0	1	2	3	4		5	6	7	8	9		10	11	12	13	14	15

Places bits 16-31 of the controller's ECC remainder register in bits 0-15 of the specified accumulator. After the data transfer, sets the controller's Busy and Done flags and initiates operations according to the function specified by F. The format of the accumulator is as follows:

SECOND ECC WORD

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	MEANING WHEN 1
0-15	a_{15} - a_0	Indicates the coefficients of the low order bits of the ECC remainder following a read operation.

3.2. Tape Instruction Formats and Register Definitions

3.2.1. Formats

DATA FORMATS

NINE TRACK

	BYTE 1								BYTE 2							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

ACCUMULATOR FORMATS

SPECIFY COMMAND AND UNIT

											Command			UNIT(DOA)	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

COMMANDS

000	Read	100	Space Reverse
001	Rewind	101	Write
010	Reserved	110	Write EOF
011	Space Forward	111	Erase

READ STATUS (DIA)

ERR	DATA LATE	REW	ILL	HI DEN	PAR ERR	EOT	EOF	BEG TAPE	9 TRK	BAD TAPE	SEND CLK	lst CHAR	WR LOCK	ODD CHAR	UNIT RDY
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

LOAD MEMORY ADDRESS COUNTER (DOB)

MAINT							MEMORY ADDRESS								
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

READ MEMORY ADDRESS COUNTER (DIB)

							MEMORY ADDRESS								
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

LOAD WORD COUNTER

OPTIONAL FOR PE TAPES															(DOC)
									WORD COUNT						
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

S, C and P FUNCTIONS

S	Set Busy to 1, Done to 0 and start the command.
C	Set all error flags to 0, select unit 0 as the addressed transport and Read command.
P	No effect.

Data General supplies two types of industry compatible tape subsystems, NRZI and PE. NRZI tape drives are available in both 7 or 9 track format; at 556 and 800 bits per inch (BPI); and in even or odd parity. The PE tape drive operates at 1600 BPI in 9 track format. Depending on the particular transport, the data transfer rate ranges from 3,480 words/second to 36,000 words/second.

The DG controller used in the NRZI subsystem can simultaneously accommodate up to 8 transports in any combination. The DG controller used in the PE subsystem can accommodate up to 4 transports. In either type of subsystem, only one transport can be reading, writing or spacing at any one time, but any number of transports can be rewinding simultaneously.

Records on the tape are composed of groups of words ranging in length from 2 to 65,536 words per record, depending on the subsystem. Files are composed of groups of records. The format of the record and file structure is shown on the following page. The number of files which can be placed on a reel of tape is dependent on the length of the tape, the information density, the number of words per record and the number of records per file. A full 10-1/2 inch reel of 1.5 mil tape can store more than 11 million 16 bit words in an NRZI subsystem or more than 22 million 16 bit words in a PE subsystem.

Data is verified during Write operations by a combination of lateral and longitudinal parity checks in a read-after-write error checking system. The same system is used when the tape is read.

INSTRUCTIONS

The tape transport controller contains four registers: a 15 bit Memory Address Counter, a 16 bit Status Register, a 12 or 16 bit Word Counter, and a 6 or 7 bit combined Command/Transport Select Register. The Memory Address Counter is self-incrementing and contains the memory location of the next word to be either read from or written on the tape. The Status Register contains all the information flags for the controller and the selected transport. The Word Counter contains the two's complement of the number of words to be read from or written on the tape or the two's complement of the number of records to be skipped in a spacing operation. The combined Command/Transport Select Register contains the last command issued to the tape subsystem and the unit number of the transport currently selected.

Five instructions are used to program data channel transfers to and from the tape subsystem. Three of these instructions are used to supply all of the necessary data to the controller for any tape operation. The remaining two instructions allow the program to determine, in detail, the current state of the selected tape transport.

The tape subsystem controller's Busy and Done flags are controlled using two of the device flag commands as follows:

f = S Set the Busy flag to 1, the Done flag to 0 and set the transport in operation for the command contained in the Command Register. Providing the Illegal flag is set to 0, all error indicating flags in the Status Register are set to 0.

f = C Set the Busy flag, the Done flag, and all error indicating flags in the Status Register to 0. The error indicating flags are: Data Late, Illegal, Parity Error, Bad Tape, End of File, and Odd Character. After a Clear command is issued, the selected transport is unit 0 and the specified command is Read.

f = P No effect.

3.2.2. Tape Register Definitions

SPECIFY COMMAND AND UNIT

DOA (f) ac, MTA

0	1	1	AC		0	1	1	F		0	1	0	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bits 9-15 of the specified AC are loaded into the combined Command/Transport Select Register. Bits 0-8 are ignored. After the data transfer, the controller's Busy and Done flags are set according to the function specified by F. The contents of the specified AC remain unchanged. The format of the specified AC is as follows:

											COMMAND			UNIT	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0 - 8		Reserved for future use.
9	Parity (NRZI)	This bit may be used to select high speed/density see paragraph 2.3.2.
10 - 12	Command	Select the command for the selected transport as follows: 000 Read 001 Rewind 010 Reserved for future use 011 Space forward 100 Space Reverse 101 Write 110 Write End Of File 111 Erase
13 - 15	Unit	Select transport 0-7 for NRZI or 0-3 for PE.

READ STATUS

DIA (f) ac, MTA

0	1	1		AC		0	0	1		F		0	1	0	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

The contents of the Status Register are placed in bits 0-15 of the specified AC. After the data transfer, the controller's Busy and Done flags are set according to the function specified by F. The format of the specified AC is as follows:

ERR	DATA LATE	REW	ILL	HI DEN	PAR ERR	EOT	EOF	BEG TAPE	9 TRK	BAD TAPE	SEND CLK	lst CHAR	WR LOCK	ODD CHAR	UNIT RDY
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0	Error	One or more of the bits 1, 3, 5, 6, 7, 8, 10 and 14 is 1.
1	Date Late	The data channel failed to respond in time to a data channel request.
2	Rewinding	The selected transport is currently rewinding.
3	Illegal	A Start command was issued to the selected transport when one of the following conditions existed: 1. The transport was not ready. 2. The command was Space Reverse and the tape was at the beginning of tape leader. 3. The command was Write, Write End of File or Erase when the tape was write-protected.
4	High Density	The selected NRZI transport is set to read or Write at 800 BPI. This bit is always 1 for PE transports (1600 BPI).
5	Parity Error	One or more bytes in the record did not have the correct parity, or in NRZI, tapes the LPCC read from the tape after the record did not match the character calculated by the controller.
6	End Of Tape	The transport has reached or passed the End Of Tape mark. Executing either a Space Reverse or a Rewind operation will set this bit to 0.
7	End Of File	The transport has encountered an End of File mark in reading, spacing or after writing an EOF mark.
8	Begin of Tape	The tape is at the beginning of tape mark.

BITS	NAME	FUNCTION
9	9 Track	The selected transport is set to Read or Write a 9 track tape. This bit is always 1 for PE transports.
10	Bad Tape	The Section of tape just processed is of poor quality.
11	Send Clock	Used for maintenance.
12	First Character	Used for maintenance
13	Write Lock	The tape on the selected transport is write-protected.
14	Odd Character	The record just read or written contains an odd number of bytes.
15	Unit Ready	The selected transport is ready.

LOAD MEMORY ADDRESS COUNTER

DOB (f) ac, MTA

0	1	1		AC		1	0	0		F		0	1	0	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

Bits 0-15 of the specified AC are loaded into the Memroy Address Counter. After the data transfer, the controller's Busy and Done flags are set according to the function specified by F. The contents of the specified AC remain unchanged. The format of the specified AC is as follows:

MAINT						MEMORY ADDRESS									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0	Maintenance	When set to 1, this bit places the NRZI subsystem in the maintenance mode of operation. This mode allows the cyclic redundancy check character used on 9 track NRZI tapes to be read into the memory location following the last data word in memory for the record. This bit may optionally be used to expand the memory address to allow direct access to 64K of memory. See paragraph 2.3.3.
1-15	Memory Address	Location of the next word in memory to be used for a data channel transfer.

LOAD WORD COUNTER

DOC (f) ac, MTA

0	1	1		AC			1	1	0		F		0	1	0	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			

Bits 1 -15 of the specified AC are loaded into the controllers word count. Bit 0 is ignored. Bit 1 of the word counter is copied into Bit 0.

							WORD COUNT								
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0 - 15	Word count	Two's complement of number of words to be transferred or records to skipped.

READ MEMORY ADDRESS COUNTER

DIB (f) ac, MTA

0	1	1		AC			0	1	1		F		0	1	0	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			

The contents of the Memory Address Counter are placed in bits 0-15 of the specified AC. After the data transfer, the controller's Busy and Done flags are set according to the function specified by F. When the Memory Address Counter is read after a Read or a Write operation, the contents point to a memory location one greater than the location of the last word transferred. The format of the specified AC is as follows:

							MEMORY ADDRESS								
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

BITS	NAME	FUNCTION
0 - 15	Memory Address	Location of the next word in memory to be used for a data channel transfer.

3.3 HARDWARE OPERATION

The following paragraphs provide a brief description of the major logical sections and busses within the SPECTRA 20. Figure 1 is a block diagram representing this hardware.

3.3.1. The CPU Processor

The CPU processor is a bit slice design using two 2901's. There are two major busses in this processor, CSRC and CDEST. CSRC is an 8 bit data buss providing the 8 bit input source to the two 2901's on their D inputs. The outputs of the 2901's provide the 8 bit destination buss, CDEST. The firmware may select a variety of sources for the CSRC buss and a variety of destinations for the CDEST buss.

The sequencer for the CPU processor consists of three 2911 IC's. These provide the ability to do jumps, conditional jumps, subroutine jumps, and subroutine returns. Up to four levels of subroutines may be nested. Also included in the hardware of the CPU processor is the logic necessary to perform a multiway (vector) jump. The outputs of the 2901's on the CDEST buss of the previous instruction may be used to provide the 8 least significant bits of the target address for the multiway jump. The most significant bits are held high, enabling the multiway jump instruction to jump to a table at the high end of the firmware. This table is a jump table so that the 2911's may recover the current program counter and continue sequencing as before.

The instruction width of the CPU processor is 36 bits, two of which are spare. The instruction is defined as follows:

Bit 35	Spare
Bit 34-31	Instruction type - defines type of jump and whether this instruction includes a flag field.
Bit 30-26	CSRC address - defines one of up to 32 sources.
Bit 25	Spare
Bit 24-22	CDEST address - defines one of up to 8 destinations.
Bit 21-17	2901 control bits I6, I5, I4, I2, and I0.
Bit 16-12	For jump instructions other than multiway jumps, these bits address the condition to be selected. The 2901 control bits I8, I7, I3, and CN are then held low (0) and I1 is held high (1). This enables certain ALU instructions to be performed at the same time as a jump instruction. For instructions other than jump instructions, these bits provide the 2901 control bits I8, I7, I3, I1, and CN directly.
Bit 11-8	For jump instructions, these bits provide the most significant bits of the target address. For instructions other than jump instructions, these bits provide both the A and B register addresses of the 2901's. Since the A and B addresses are identical, the dual port capability of the 2901's is not used.

Bit 7-0 For jump instructions, these bits provide the least significant 8 bits of the target address.
For instructions using the flag field, these bits are used to select the flag.
For instructions using a constant for CSRC, these bits provide that constant.

3.3.2. The DISK Processor

The DISK processor is a bit slice design using two 2901's and is very similar to the CPU processor. The 8 bit source buss is called DSRC and the 8 bit destination buss is called DDEST. The sequencer for the DISK processor consists of three 2911 IC's and is very similar to the CPU processor's sequencer. The major difference between the two sequencers is that the DISK processor does not have the multiway jump facility.

The instruction width of the DISK processor is 32 bits. Eight 1Kx4 PROM's are used. The instruction is defined as follows:

Bit 31-29 Instruction type - defines type of jump and whether this instruction includes a flag field.

Bit 28-26 DSRC address - defines one of 8 sources.

Bit 25-22 DDEST address - defines one of 16 destinations.

Bit 21-16 2901 control bits I6, I5, I4, I2, I0, and CN.

Bit 15-12 For jump instructions, these bits address the condition to be selected. The 2901 control bit I8, I7, and I3 are then held low (0) and I1 is held high (1). This enables certain ALU instructions to be performed at the same time as a jump instruction.
For instructions other than jump instructions, these bits provide the 2901 control bits I8, I7, I3, and I1 directly.

Bit 11-8 For jump instructions, these bits provide the most significant bits of the target address.
For instructions other than jump instructions, these bits provide both the A and B register addresses of the 2901. Since the A and B addresses are identical, the dual port capability of the 2901's is not used.

Bit 7-0 For jump instructions, these bits provide the least significant 8 bits of the target address.
For instructions using the flag field, these bits are used to select the flag.
For instructions using a constant for DSRC, these bits provide that constant.

3.3.3. The Disk Interface

The SMD disk interface is controlled by the DISK processor. The firmware may write directly to the SMD buss lines and tag lines. The data is passed through two 74S299 IC's used as a 16 bit serializer/deserializer shift register. Further registers surrounding this shift register give the firmware a 16 bit word time to move the first two bytes to or from the Sector Buffer. The firmware is synchronized to the SMD interface by a bit counter which sets a word available flip-flop, WRDAV, each time the counter overflows. All controls for the CRC and ECC logic may also be switched at this word available time. It is necessary for the firmware to pre-load these controls in the previous word time. The controls will be synchronized and enabled at the next word available time.

The firmware will normally elect to write a CRC field after each header. The hardware used to do this is a 9401 IC wired to generate the polynomial $X^{16} + X^{15} + X^2 + 1$. This IC is also used when reading the header to check its validity. At the end of the data field, however, four bytes of ECC are written. The polynomial used in this case is $X^{32} + X^{23} + X^{21} + X^{11} + X^2 + 1$. The hardware used to implement this polynomial are several MSI IC's. When reading data from the disk, the firmware may choose to break this polynomial up into its factors and return an ECC pattern identical to the DG 6060 Series. Optionally, the firmware will not factor the polynomial, and any correctable error encountered will be corrected by the firmware in the Sector Buffer before passing the data to the DG computer.

3.3.4. The Mag Tape Interface

The Mag Tape interface is controlled by the CPU processor. The firmware may write directly into two 8 bit registers to enable/disable various tape formatter control signals. Data read from the selected tape unit is buffered through two 67402 FIFO IC's providing 64 bytes of buffering. Data to be written onto the tape is also passed through the FIFO. A 74S280 IC generates parity for each byte stored in the FIFO, and another 74S280 checks parity on each byte read from the FIFO. Mag Tape status may be stored in 74LS373 registers or enabled onto the DG databus. The Mag Tape unit select and formatter select is stored in a 74LS273 IC which provide inputs to a 7416 IC to drive the select lines. All write data and control lines are driven by 7416 IC's. Read data and status signals are received by 74LS240 IC's, with 220/330 ohm resistor dividers used for line termination.

4.0 DIAGNOSTICS

4.1. MICRODIAGNOSTICS AND LEDS

Microdiagnostics are run every time the controller powers up. The CPU processor and the DISK processor each have their own diagnostics. Any failure will cause the LEDs to be lit. The LEDs have the following meaning:

DS5	DS6	DS7	DS8	
Off	Off	Off	Off	No Fault
Off	Off	Off	On	CPU processor failed basic 2901 test.
Off	Off	On	Off	CPU processor failed ALU function test.
Off	Off	On	On	CPU processor failed register address test.
Off	On	Off	Off	CPU processor failed RAM buffer test.
Off	On	Off	On	CPU processor failed MT counter test.
Off	On	On	Off	CPU processor failed MT FIFO test.
Off	On	On	On	CPU processor failed interrupt test.
Any other settings				CPU processor's sequencer failed.

DS4	DS3	DS2	DS1	
Off	Off	Off	Off	No Fault
Off	Off	Off	On	Disk processor failed basic 2901 test.
Off	Off	On	Off	Disk processor failed ALU function test.
Off	Off	On	On	Disk processor failed register address test.
Off	On	Off	Off	Disk processor failed serializer/deserializer test.
Off	On	Off	On	Disk processor failed ECC test.
Off	On	On	Off	Disk processor failed RAM buffer test.
Any other settings				Disk processor's sequencer failed.

N.B.: Since both processors test the RAM buffer, there is some communication between the two processors during diagnostics. For this reason, both processors may be indicating a fault when in fact only one has failed.

4.2. DIAGNOSTIC SOFTWARE

The SPECTRA 20 multifunction disk controller is designed to emulate the Data General 6067 Disk Subsystem, Data General Mag Tape subsystem, and to run with the standard Data General diagnostics:

ZDKP FMTR	(095-000471)	6067 Formatter
ZDKP DIAG	(095-000470)	6067 Diagnostic
ZDKP RELI	(095-000469)	6067 Reliability Program
MAG DIAG	(095-000033)	Magnetic Tape Diagnostic
MAG RELI	(095-000034)	Magnetic Tape Reliability

In standard emulation mode (815 cylinders, 5 heads, and 24 sectors per track), the Disk Formatter and Reliability programs run without modification. The Disk Diagnostic and Mag Tape Diagnostic and Reliability programs require a few patches to ignore those features which the SPECTRA 20 does not emulate, none of which affect operational system software. In expanded emulation mode with different numbers of cylinders, heads, and/or sectors per track, additional changes have to be made to the disk programs in order to take advantage of these different capacities.

4.2.1. DTOS REV. 7

ZDKP FMTR (095-000471-03)

4.2.1.1. To change sectors per track from 24 to 32:

Address	Is	Change to	Comments
113	30	40	;sectors/track
171	30	40	;sectors/track
2525	176400	176000	;-(sectors/track*40)
2536	1400	2000	;sectors/track*40
2537	27	37	;sectors/track-1

80MB disk (815 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (815 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.1.2. To change cylinders from 815 to 823:

Address	Is	Change to	Comments
202	1457	1467	;cylinders

80MB disk (823 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (823 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.1.3. For 160MB disk with 1645 cylinders:

Address	Is	Change to	Comments
202	1457	3155	;cylinders
1167	34170	34172	;load cylinder mask
2606	167400	2401	;JMP @ .+1
2607	123000	370	;
370	-	167400	;AND 3,1
371	-	123000	;ADD 1,0
372	-	34404	;LDA 3,.+4
373	-	163400	;AND 3,0
374	-	2401	;JMP @ .+1
375	-	2610	;
376	-	160377	;mask

160MB disk (1645 cylinders, 5 heads) is referred to as 50MB 6067.

ZDKP FMTR (095-0000471-03) (cont.)

4.2.1.4. To change number of heads or cylinders for other drives:

Address	Is	Change to	Comments
202	1457	CCCC	;cylinders
1200	22	HH-1	;heads-1
		34167	;if CCCC less than 1000
1167	34170	34170	;if CCCC between 1000 & 2000
		34172	;if CCCC greater than 2000

Disk is referred to as 190MB 6061.
CCCC and HH are values taken from the Drive Configuration Table (4.2.3.).

ZDKP DIAG (095-000470-03)

4.2.1.5. Required Changes:

Address	Is	Change to
1511	6246	403
1600	6252	474
1723	6251	6263
1724	60227	6274
3272	16000	12000
3322	16000	12000
3423	6252	516
4113	20216	557
6476	451	401

4.2.1.6. To change sectors per track from 24 to 32:

Address	Is	Change to	Comments
142	177750	177740	;-sectors/track
2367	0	400	;32 sector write
2474	102400	20102	;check head increment
2554	40401	40000	;force illegal sector
2637	10006	10406	;force illegal surface
2640	44006	44406	;
5621	21400	20212	;

80MB disk (815 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (815 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.1.7. To change cylinders from 815 to 823:

Address	Is	Change to	Comments
214	1457	1467	;cylinders

80MB disk (823 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (823 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.1.8. For 160MB disk with 1645 cylinders:

Address	Is	Change to	Comments
214	1457	3155	;cylinders
6655	34211	34212	;load cylinder mask
6023	176400	2401	;JMP @ .+1
6024	151220	332	;
332	-	34212	;LDA 3,212
333	-	173400	;AND 3,2
334	-	176400	;SUB 3,3
335	-	151220	;MOVZR 2,2
336	-	2401	;JMP @ .+1
337	-	6025	;

160MB disk (1645 cylinders, 5 heads) is referred to as 50MB 6067.

4.2.1.9. To change number of heads or cylinders for other drives:

Address	Is	Change to	Comments
214	1457	CCCC	;cylinders
6707	22	HH-1	;heads-1
		34212	;if CCCC less than 1000
6655	34211	34211	;if CCCC between 1000 & 2000
		34212	;if CCCC greater than 2000
212	1777	377	;if CCCC less than 1000

Disk is referred to as 190MB 6061.
CCCC and HH are values taken from the Drive Configuration Table (4.2.3.).

4.2.1.10. To change sectors per track from 24 to 32:

Address	Is	Change to	Comments
116	30	40	;sectors/track
6757	176400	176000	;-(sectors/track*40)
6770	1400	2000	;sectors/track*40
6771	27	37	;sectors/track-1

80MB disk (815 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (815 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.1.11. To change cylinders from 815 to 823:

Address	Is	Change to	Comments
3713	1457	1467	;cylinders

80MB disk (823 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (823 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.1.12. For 160MB disk with 1645 cylinders:

Address	Is	Change to	Comments
3713	1457	3155	;cylinders
3663	34426	34151	;load cylinder mask
7042	167400	2401	;JMP @ .+1
7043	123000	350	;
350	-	167400	;AND 3,1
351	-	123000	;ADD 1,0
352	-	34404	;LDA 3,.+4
353	-	163400	;AND 3,0
354	-	2401	;JMP @ .+1
355	-	2610	;
356	-	160377	;mask

160MB disk (1645 cylinders, 5 heads) is referred to as 50MB 6067.

4.2.1.13. To change number of heads or cylinders for other drives:

Address	Is	Change to	Comments
3713	1457	CCCC	;cylinders
3710	22	HH-1	;heads-1
		34146	;if CCCC less than 1000
3663	34426	34426	;if CCCC between 1000 & 2000
		34151	;if CCCC greater than 2000

Disk is referred to as 190MB 6061.
CCCC and HH are values taken from the Drive Configuration Table (4.2.3.).

4.2.1.14. Additional changes required for Fixed/Removable Cartridge Drives (CDC CMD and Ampex DFR)

ZDKP FMTR (095-000471-03)

Address	Is	Change to
2516	20073	2401
2517	101005	1103

Other changes as in 4.2.1.4.

ZDKP DIAG (095-000470-03)

Address	Is	Change to
2176	32037	37
2177	44037	37
2367	400	0
2403	2400	2000
2474	20102	102400
2537	751	401

Other changes as in 4.2.1.9.

ZDKP RELI (095-000469-03)

No additional changes
Other changes as in 4.2.1.13

MAG DIAG (095-000033-11)

4.2.1.15. Required Changes:

Address	Is	Change to
330	0	2600
745	6275	443
1030	20135	415*
1124	100220	100200
1132	6265	466
1413	34233	415
1456	6274	425
2101	102001	1
2124	102001	1
2244	34060	2401
2245		2625
2600	102	54404
2601	6264	6265
2602	1	6317
2603	6277	2401
2667	6317	6330
2730	6317	6330
2771	6317	6330
3030	20453	464
3547	71	1000
3724	70	200
3756	20137	102400
4024	70	400

*Note: Only if Speed/Density select option is installed. (See 2.3.2.)

MAG RELI (095-000034-15)

4.2.1.16. Required Changes:

Address	Is	Change to
1406	1750	20000
1633	1750	20000
2330	1750	20000
2413	1750	20000
3010	30256	404

4.2.2. DTOS REV. 8

ZDKP FMTR (095-000471-04)

4.2.2.1. To change sectors per track from 24 to 32:

Address	Is	Change to	Comments
1246	27	37	;sectors/track-1
1256	27	37	;sectors/track-1
3013	176400	176000	;-(sectors/track*40)
3024	30	40	;sectors/track
3025	27	37	;sectors/track-1

80MB disk (815 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (815 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.2.2. To change cylinders from 815 to 823:

Address	Is	Change to	Comments
1244	1456	1466	;cylinders-1
1254	1456	1466	;cylinders-1

80MB disk (823 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (823 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.2.3. For 160MB disk with 1645 cylinders:

Address	Is	Change to	Comments
1247	22	4	;heads-1
1250	632	3154	;cylinders-1
1251	777	3777	;mask
1252	27	37	;sectors/track-1
3067	167400	2401	;JMP @ .+1
3070	123000	366	;
366	-	167400	;AND 3,1
367	-	123000	;ADD 1,0
370	-	34404	;LDA 3,.+4
371	-	163400	;AND 3,0
372	-	2401	;JMP @ .+1
373	-	3071	;
374	-	160377	;mask

160MB disk (1645 cylinders, 5 heads) is referred to as 96MB 6060.

ZDKP FMTR (095-0000471-04) (cont.)

4.2.2.4. To change number of heads or cylinders for other drives:

Address	Is	Change to	Comments
1247	22	HH-1	;heads-1
1250	632	CCCC-1	;cylinders-1
		777	;if CCCC less than 1000
1251	777	1777	;if CCCC between 1000 & 2000
		3777	;if CCCC greater than 2000
1252	27	37	;sectors/track-1

Disk is referred to as 96MB 6060.
CCCC and HH are values taken from the Drive Configuration Table (4.2.3.).

ZDKP DIAG (095-000470-04)

4.2.2.5. Required Changes:

Address	Is	Change to
1533	6246	403
1622	6253	504
1756	6252	6264
1757	60227	6275
3650	16000	12000
3700	16000	12000
4004	6253	520
4472	102400	561
7240	451	401

4.2.2.6. To change sectors per track from 24 to 32:

Address	Is	Change to	Comments
7513	27	37	;sectors/track
7523	27	37	;sectors/track
2505	0	10	;32 sector write
2661	102400	20105	;check head increment
3065	40401	40000	;force illegal sector
3150	126400	24105	;force illegal surface
4733	24022	24021	;

80MB disk (815 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (815 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.2.7. To change cylinders from 815 to 823:

Address	Is	Change to	Comments
7511	1456	1466	;cylinders-1
7521	1456	1466	;cylinders-1

80MB disk (823 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (823 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.2.8. For 160MB disk with 1645 cylinders:

Address	Is	Change to	Comments
7514	22	4	;heads-1
7515	632	3154	;cylinders-1
7516	777	3777	;mask
7517	27	37	;sectors-1
6572	176400	2401	;JMP @ .+1
6573	151220	333	;
333	-	34406	;LDA 3,.+6
334	-	173400	;AND 3,2
335	-	176400	;SUB 3,3
336	-	151220	;MOVZR 2,2
337	-	2401	;JMP @ .+1
340	-	6574	;
341	-	1777	;mask

160MB disk (1645 cylinders, 5 heads) is referred to as 96MB 6060.

4.2.2.9. To change number of heads or cylinders for other drives:

Address	Is	Change to	Comments
7514	22	HH-1	;heads-1
7515	632	CCCC-1	;cylinders-1
		777	;if CCCC less than 1000
7516	777	1777	;if CCCC between 1000 & 2000
		3777	;if CCCC greater than 2000
7517	27	37	;sectors/track-1

Disk is referred to as 96MB 6060.
CCCC and HH are values taken from the Drive Configuration Table (4.2.3.).

4.2.2.10. To change sectors per track from 24 to 32:

Address	Is	Change to	Comments
4277	27	37	;sectors/track-1
4307	27	37	;sectors/track-1
7236	176400	176000	;-(sectors/track*40)
7247	30	40	;sectors/track
7250	27	37	;sectors/track-1

80MB disk (815 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (815 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.2.11. To change cylinders from 815 to 823:

Address	Is	Change to	Comments
4275	1456	1466	;cylinders-1
4305	1456	1466	;cylinders-1

80MB disk (823 cylinders, 5 heads) is referred to as 50MB 6067.
300MB disk (823 cylinders, 19 heads) is referred to as 190MB 6061.

4.2.2.12. For 160MB disk with 1645 cylinders:

Address	Is	Change to	Comments
4300	22	4	;heads-1
4301	632	3154	;cylinders-1
4302	777	3777	;mask
4303	27	37	;sectors/track-1
7312	167400	2401	;JMP @ .+1
7313	123000	342	;
342	-	167400	;AND 3,1
343	-	123000	;ADD 1,0
344	-	34404	;LDA 3,.+4
345	-	163400	;AND 3,0
346	-	2401	;JMP @ .+1
347	-	7314	;
350	-	160377	;mask

160MB disk (1645 cylinders, 5 heads) is referred to as 96MB 6060.

4.2.2.13. To change number of heads or cylinders for other drives:

Address	Is	Change to	Comments
4300	22	HH-1	;heads-1
4301	632	CCCC-1	;cylinders-1
		777	;if CCCC less than 1000
4302	777	1777	;if CCCC between 1000 & 2000
		3777	;if CCCC greater than 2000
4303	27	37	;sectors/track-1

Disk is referred to as 96MB 6060.
CCCC and HH are values taken from the Drive Configuration Table (4.2.3.).

4.2.3. DRIVE CONFIGURATION TABLE

	Type	Capac	Cyls	Hds	Secs	CCCC	HH	SS	M,LLLLLL
AMPEX									
	DM940	40MB	411	5	32	633	5	40	1,340
	DM980	80MB	823	5	32	1467	5	40	2,1140
	DM9160	160MB	1645	5	32	3155	5	40	4,2040
	DM9300	300MB	815	19	32	1457	23	40	7,107640
	DM9300A	300MB	823	19	32	1467	23	40	7,121240
	DFR932	16MB R	823	1	32	1467	1	40	0,63340
		16MB F	823	1	32	1467	1	40	0,63340
	DFR964	16MB R	823	1	32	1467	1	40	0,63340
		48MB F	823	3	32	1467	3	40	1,32240
	DFR996	16MB R	823	1	32	1467	1	40	0,63340
		80MB F	823	5	32	1467	5	40	2,1140
CONTROL DATA									
SMD	9760	40MB	411	5	32	633	5	40	1,340
	9762	80MB	823	5	32	1467	5	40	2,1140
	9764	150MB	411	19	32	633	23	40	3,150040
	9766	300MB	823	19	32	1467	23	40	7,121240
CMD	9448-32	16MB R	823	1	32	1467	1	40	0,63340
		16MB F	823	1	32	1467	1	40	0,63340
	9448-64	16MB R	823	1	32	1467	1	40	0,63340
		48MB F	823	3	32	1467	3	40	1,32240
	9448-96	16MB R	823	1	32	1467	1	40	0,63340
		80MB F	823	5	32	1467	5	40	2,1140
MMD	9730-12	12MB	320	2	32	500	2	40	0,50000
	9730-24	24MB	320	4	32	500	4	40	0,120000
	9730-80	80MB	823	5	32	1467	5	40	2,1140
	9730-160	160MB	823	10	32	1467	12	40	4,2300
CENTURY DATA									
	T82	80MB	815	5	32	1457	5	40	1,176540
	T82X	80MB	823	5	32	1467	5	40	2,1140
	T302	300MB	815	19	32	1457	23	40	7,107640
	T302X	300MB	823	19	32	1467	23	40	7,121240
FUJITSU									
	2201	50MB	815	3	32	1457	3	40	1,30640
	2211	80MB	823	5	32	1467	5	40	2,1140
	2282	66MB	823	4	32	1467	4	40	1,115600
	2283	132MB	823	8	32	1467	10	40	3,33400
	2284	165MB	823	10	32	1467	12	40	4,2300
	2311	48MB	589	4	32	1115	4	40	1,23200
	2312	84MB	589	7	32	1115	7	40	2,1540

4.2.3. DRIVE CONFIGURATION TABLE (cont.)

Type	Capac	Cyls	Hds	Secs	CCCC	HH	SS	M,LLLLLL
DASTEK								
4830-1	200MB	823	12	32	1467	14	40	4,151200
4830-2	330MB	823	20	32	1467	24	40	10,4600
4830-3	400MB	823	24	32	1467	30	40	11,122400
KENNEDY								
5300-70	70MB	700	5	32	1274	5	40	1,132600
5380	80MB	823	5	32	1467	5	40	2,1140

5.0 SYSTEM SOFTWARE

5.1. INITIALIZATION

The SPECTRA 20 multifunction controller in standard emulation mode is designed to run RDOS V6.62 without modifications. In order to take advantage of the increased capacities of many SMD compatible disk drives, it is necessary to make some minor parameter changes in DKINIT. The procedure is as follows, with the required values taken from the Drive Configuration Table (see 4.2.3.):

(1) Execute DKINIT either from MT0:4 or from a running RDOS disk.

(2) Halt the CPU and make the following parameter changes:

Address	Is	Change to	Comments
20557	1	M	# Blocks
20560	77010	LLLLLL	
20561	1457	CCCC	Cylinders
20562	170	HH*SS	Sectors/cylinder
31564	5	HH	Heads
31565	30	SS	Sectors/track
31566	1	M	# Blocks-6
31567	77002	LLLLLL-6	

(3) Continue with the RDOS build.

INTERFACES

Disk

The disk interface is industry standard SMD compatible allowing attachment of up to two drives. The SPECTRA 20 provides an SMD compatible flat cable connector set with pin assignment and signals defined on the following pages.

Tape

The tape interface is compatible with the Pertec industry standard embedded formatter. This interface consists of two 50 pin connectors with pin assignments and signals defined on the following pages.

"A" CABLE

CONTROLLER			DRIVE LO, HI	
Unit Select Tag			22, 52	
Unit Select 2^0			23, 54	
Unit Select 2^1			24, 54	
Unit Select 2^3			27, 57	
Tag 1	2*		1, 31	
Tag 2	2*		2, 32	
Tag 3	2*		3, 33	
Bit 0	2*		4, 34	
Bit 1	2*		5, 35	
Bit 2	2*		6, 36	
Bit 3	2*		7, 37	
Bit 4	2*		8, 38	
Bit 5	2*		9, 39	
Bit 6	2*		10, 40	
Bit 7	2*		11, 41	
Bit 8	2*		12, 42	
Bit 9	2*		13, 43	
Open Cable Detector			14, 44	
Index	2*		18, 48	
Sector	2*		25, 55	
Fault	2*		15, 45	
Seek Error	2*		16, 46	
On Cylinder	2*		17, 47	
Unit Ready	2*		19, 49	
Address Mark Found	2*		20, 50	
Write Protected	2*		28, 58	
Power Sequence Pick			29	(one twisted
Power Sequence Hold			59	pair)
Busy	2*	1**	21, 51	
Bit 10	2*	3**	30, 60	

NOTE: 60 Position, 28 Awg., 30 twisted pair, flat cable, 100 ft. max.
1** Dual Channel units Only. 2* Gated by unit selected.
3* Bit 10 used for cylinder 1024 Bit for drives so equipped.

"B" CABLE

CONTROLLER	DRIVE LO, HI
Write Data	8, 20
Ground	7
Write Clock	6, 19
Ground	18
Servo Clock	2, 14
Ground	1
Read Data	3, 16
Ground	15
Read Clock	5, 17
Ground	4
Seek End	10, 23
Unit Selected	22, 9
Ground	21
Reserved for Index	12, 24
Ground	11
Reserved for Index	13, 26
Ground	25

NOTES:

1. 26 conductor shielded flat cable
   Maximum length - 50 ft.

2. No signals gated by Unit Selected.

TAPE
INTERFACE PLUG CONNECTIONS

P-1

Live Pin	Ground Pin	Signal	Signal Name
2	1	Formatter Busy	FBY
4	3	Last Word	LWD
6	5	Write Data 4	W4
8	7	Initiate Command	GO
10	9	Write Data Ø	WØ
12	11	Write Data 1	W1
14	13	Reserved	
16	15	Reserved	
18	17	Reverse	REV
20	19	Rewind	REW
22	21	Write Data Parity	WP
24	23	Write Data 7	W7
26	25	Write Data 3	W3
28	27	Write Data 6	W6
30	29	Write Data 2	W2
32	31	Write Data 5	W5
34	33	Write	WRT
36	35	Reserved	
38	37	Edit	EDIT
40	39	Erase	ERASE
42	41	Write Filemark	WFM
44	43	Reserved	
46	45	Transport Address Ø	TADØ
48	47	Read Data 2	R2
50	49	Read Data 3	R3

TAPE

P-2

Live Pin	Ground Pin	Signal	Signal Name
1	—	Read Data Parity	RP
2	—	Read Data Ø	RØ
3	—	Read Data 1	R1
4	—	Load Point	LDP
6	5	Read Data 4	R4
8	7	Read Data 7	R7
10	9	Read Data 6	R6
12	11	Hard Error	HER
14	13	Filemark	FMK
16	15	Identification 1	IDENT
18	19	Formatter Enable	FEN
20	19	Read Data 5	R5
22	21	End Of Tape	EOT
24	23	Rewind/Unload	RWU
26	25	Reserved	
28	27	Ready	RDY
30	29	Rewinding	RWD
32	31	File Protect	FPT
34	33	Read Strobe	RSTR
36	35	Write Strobe	WSTR
38	37	Data Busy	DBY
40	39	Hi Speed Select	SPEED
42	41	Corrected Error	CER
44	43	On Line	ONL
46	45	Transport Address 1	TAD1
48	47	Formatter Address	FAD
50	49	High Speed Select	HISP

APPENDEX B
TROUBLESHOOTING CHECKLIST

The following checklist should be consulted prior to installation, and during installation if problems occur.

General

1. Is the drive grounded properly to the computer chassis? A braided ground strap should be connected between the first disk drive and the computer chassis. Also ground straps should be connected between multiple disk drives.

2. Are the drive and controller/CPU plugged into a common AC power source? If not they should be.

3. Check for proper voltages: primarily +5 vdc and -5 vdc or -15 vdc if applicable. DC voltage should be measured on the PCB to ensure it is set at 5 volts $\pm$ 5 % (4.7.5 to 5.25). If voltage is low and cannot be adjusted to specification, try unloading the supply in twin supply chassis by reassigning PCB's to different slots. This mostly applies to DEC systems, not DG, or PE.

4. If you have another disk drive, tape drive, or CPU run tests using any or all to verify results. This is to ensure the particular drive or CPU is not the cause of the problem, either due to configuration or fault.

5. Check to see that an appropriate burst rate (or throttle control) is set in the controller. Refer to switch settings earlier in this manual.

6. Try to cut test down to an absolute minimum: run on 1 cylinder and head, etc. If you cannot run the diagnostic or OS in expanded mode, try it in the standard mode.

Controller

1. Check all switch settings, read the installation section and check them again! It is easy to set one switch wrong.

2. Ensure the NPG jump (CA1 to CB1) is out on the slot being used (DEC). On DG systems, ensure the INTP and DCHP signals are jumpered properly on the slot used. On P-E systems, ensure RACKO TACKO is jumpered properly, and SNSO is wired from the SELECH to the slot being used; on systems with a "remote bus" jumper 124-1 to 229-1.

3. Check to see if the cables are plugged in properly; on S12, S14, S20, and S21 products the arrowhead on the cable connector mates with the arrowhead on the PCB header. The S11 product must have the cables put on opposite to this, or "backwards," with the arrowheads on opposite ends from each other. When switching from S11 to an S12 this is sometimes overlooked. Also check the cables for opens or shorts if suspected.

4. Are the cables supplied by Spectra Logic? If not double check the termination into the connector for not frayed wires, shorts, etc. and that the shield is attached to ground.

5. On P-E systems, if the disk subsystems is running excessively slow, check the throttle switches and the "optional protocol" is selected.

Drive

1. Check the sectors per track setting for 32 sectors/track; CDC ships drives with 64 sectors/tracks.

2. Is "Index and Sector" supplied in the "A" cable, or both "A" and "B"? The S11, S14, and S20 require these signals be in the "A" cable. The S12 and S21 will use Index and Sector in either the "A" or "B" cable; providing switch for RPS is set appropriately. Some drives may have a PCB part number indicating these signals are in the "A" cable, but it may be jumpered incorrectly. Also, if the drive is a CDC SMD drive, check the jumper for gating Index and Sector on the "A" cable; important on multiple drive installation.

3. Is the drive set for hard sectoring, i.e. a fixed number of sectors/track, v.s. soft sectoring (using Address Marks)? Spectra Logic controllers do not use Address Marks and only run with hard sectoring: typically 24, 32, or 33 sectors/track.

4. Are the interface cables at the drive end connected properly (pin 1 to pin 1) and plugged into the proper A or B port? Some drives may have both A and B port connectors installed even though it is not a dual port drive; PCB's not installed for the option.

5. What is the disk drive's history—has it been working on another controller/system? Try to use a known good drive. If the drive has been used on a different controller manufacturer's product, double check that Index and Sector are in the "A" cable and gated properly. If the disk (pack or media) was previously formatted by a controller other than Spectra Logic, it should be reformatted. The S12 and S21 are format compatible with a DEC RM02, so reformatting is not necessary.

6. Is the drive a "flat cable" or "round cable" drive? If it is a "round cable" version, check with Spectra Logic.

MAGNETIC TAPE INTERFACE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

UNIT NO
STATUS
WRITE DATA
READ DATA
COMMAND
CONTROL

MT UNIT & COMMAND 273 (7)
BUFFER 244 (7)
MT STATUS 1 240 (10)
MT STATUS 2 240 (10)
LATCH 373 (10)
LATCH 373 (10)
MT WRITE DATA (9)
FIFO 64x9 2x67402 (9)
BUFFER 244 (9)
MT READ DATA 240 (9)
BUFFER 374 (9)
MT COMMAND 273 (10)
MT CONTROL 273 (10)
DRIVE STATUS 2x3450 (21) → DRIVE STATUS
MT WORD COUNT 2x374 (7)
DMA DATA IN REGS 2x374 (7)
DMA DATA IN BUFFER 374 (7)
COUNTER 4x569 (10)
CONSTANT FROM FIRMWARE
BUFFER 244 (17)
OPTION SWITCH (18)
SER/DES IN 2x374 (19)
SER/DES 2x299 (19)
SER/DES OUT 2x374 (19)
DK CYLINDER 2x374 (8)
OPTION SWITCH (14)
CSB DIN 374 (15)
DSB DIN 374 (15)
DISK ALU 2x2901 (18)
DSRC
DDEST
SMD HI 174 (22)
DRIVER 3453 (23) → BUS 8-10
DG DIN
CONSTANT FROM FIRMWARE
BUFFER 244 (12)
CSRC
CPU ALU 2x2901 (14)
C.DEST
CSB DOUT 374 (15)
DSB DOUT 374 (15)
SMD LO 273 (22)
DRIVER 3453 (23) → BUS Ø-7
DK DRIVE & COMMAND 273 (8)
MUX 4x257 (8)
SECTOR BUFFER 2K x 8 4x2149 (15)
UNIT SELECT 174 (22)
DRIVER 3453 (23) → UNIT SELECT Ø-3
DK SURF. SEC & COUNT 5x197 (8)
BUFFER 2x244 (8)
DMA DATA OUT REGS 2x374 (7)
DMA DATA OUT BUFFER 374 (7)
DK PORT NO 175 (5)
CSB ADDRESS 3x569 (15)
DSB ADDRESS 3x569 (15)
CLOCK CONTROL 174 (11)
DRIVERS 3453s (23) → TAGS, WRITE DATA, WRITE CLOCK
DK ADDRESS COUNTER 4x197 (6)
BUFFER 2x244 (6)
DK XFER STATUS 2x244 (6)
HARDWARE STATUS BITS
XFER STATUS REG 273 (5)
DRIVE STATUS FILE 16x4 4x670 (7)
RD/WR CONTROL 273 (9)
RCVRS 3450s (23) → UNIT SELECTED, READ DATA, READ CLOCK, SERVO CLOCK
MT ADDRESS COUNTER 4x197 (6)
BUFFER 2x244 (6)
MT STATUS REG 273 (5)
MT STATUS 2x244 (5)
HARDWARE STATUS BITS
ECC PATTERN 2x244 (20)
ECC BUFFERS 4x257 (20)
ECC LOGIC 4x473 (20)
16
16
DG DOUT
32
DEVICE SELECT LOGIC 2x257 (3)
DG TRANCEIVERS 4x26S12 (6)
DATA GENERAL INTERFACE

SMD INTERFACE

TOLERANCES UNLESS OTHERWISE SPECIFIED			SPECTRA LOGIC	
FRACTIONS	DEC	ANGLES	SPECTRA 20 DATAFLOW BLOCK DIAGRAM	
±	±	±		
APPROVALS	DATE			
DRAWN SK/B	10/9/80		SCALE	SIZE D
CHECKED			DO NOT SCALE DRAWING	SHEET 1 OF 1