IBM - 9020

DATA PROCESSING SYSTEM REFERENCE DATA

STANDARD INSTRUCTION SET

NAME	MNEMONIC	OPERAND	CODE	FORMAT
Add(c)	AR	R1,R2	1A	RR
Add(c,4)	A	R1,D2(X2,B2)	5A	RX
Add Halfword(c,2)	AH	R1,D2(X2,B2)	4A	RX
Add Logical(c)	ALR	R1,R2	1E	RR
Add Logical(c,4)	AL	R1,D2(X2,B2)	5E	RX
AND(c)	NR	R1,R2	14	RR
AND(c,4)	N	R1,D2(X2,B2)	54	RX
AND(c)	NI	D1(B1),I2	94	SI
AND(c)	NC	D1(L,B1),D2(B2)	D4	SS
Branch and Link	BALR	R1,R2	05	RR
Branch and Link (2)	BAL	R1,D2(X2,B2)	45	RX
Branch on Condition	BCR	M1,R2	07	RR
Branch on Condition (2)	BC	M1,D2(X2,B2)	47	RX
Branch on Count	BCTR	R1,R2	06	RR
Branch on Count(2)	BCT	R1,D2(X2,B2)	46	RX
Branch on Index High(2)	BXH	R1,R3,D2(B2)		RS
Branch on Index Low or Equal(2)	BXLE	R1,R3,D2(B2)	87	RS
Compare(c)	CR	R1,R2	19	RR
Compare(c,4)	C	R1,D2(X2,B2)	59	RX
Compare Halfword(c,2)	CH	R1,D2(X2,B2)	49	RX
Compare Logical(c)	CLR	R1,R2	15	RR
Compare Logical(c,4)	CL	R1,D2(X2,B2)	55	RX
Compare Logical(c)	CLC	D1(L,B1),D2(B2)	D5	SS
Compare Logical(c)	CLI	D1(B1),I2	95	SI
Convert to Binary (8)	CVB	R1,D2(X2,B2)	4F	RX
Convert to Decimal(8)	CVD	R1,D2(X2,B2)	4E	RX
Diagnose(p,8)	DIAG	D1(B1)	83	SI
Divide(e)	DR	R1,R2	ID	RR
Divide(e,4)	D	R1,D2(X2,B2)	5D	RX
Exclusive OR(c)	XR	R1,R2	17	RR
Exclusive OR(c,4)	X	R1,D2(X2,B2)	57	RX
Exclusive OR(c)	XI	D1(B1),I2	97	SI
Exclusive OR(c)	XC	D1(L,B1),D2(B2)	D7	SS
Execute(2)	EX	R1,D2(X2,B2)	44	RX
Halt I/O(c,p)	HIO	D1(B1)	9E	SI
Insert Character	IC	R1,D2(X2,B2)	43	RX
Load	LR	R1,R2	18	RR
Load(4)	L	R1,D2(X2,B2)	58	RX
Load Address	LA	R1,D2(X2,B2)	41	RX
Load and Test(c)	LTR	R1,R2	12	RR
Load Complement(c)	LCR	R1,R2	13	RR
Load Halfword(2)	LH	R1,D2(X2,B2)	48	RX
Load Multiple(4)	LM	R1,R3,D2(B2)	98	RS
Load Negative(c)	LNR	R1,R2	11	RR
Load Positive(c)	LPR	R1,R2	10	RR
Load PSW(n,p)	LPSW	D1(B1)	82	SI
Move	MVI	D1(B1),I2	92	SI
Move	MVC	D1(L,B1),D2(B2)	D2	SS
Move Numerics	MVN	D1(L,B1),D2(B2)	D1	SS
Move with Offset	MVO	D1(L1,B1),D2(L2,B2)	F1	SS
Move Zones	MVZ	D1(L,B1),D2(B2)	D3	SS
Multiply(e)	MR	R1,R2	1C	RR
Multiply(e,4)	M	R1,D2(X2,B2)	5C	RX
Multiply Halfword(2)	MH	R1,D2(X2,B2)	4C	RX
OR(c)	OR	R1,R2	16	RR
OR(c,4)	O	R1,D2(X2,B2)	56	RX
OR(c)	OI	D1(B1),I2	96	SI
OR(c)	OC	D1(L,B1),D2(B2)	D6	SS
Pack	PACK	D1(L1,B1),D2(L2,B2)	F2	SS
Set PCI(c,p)	SPCI	D1(B1)	9B	SI
Set Program Mask(n)	SPM	R1	04	RR
Set System Mask(p,2)	SSM	D1(B1)	80	SI
Shift Left Double(c)	SLDA	R1,D2(B2)	8F	RS
Shift Left Single(c)	SLA	R1,D2(B2)	8B	RS
Shift Left Double Logical	SLDL	R1,D2(B2)	8D	RS
Shift Left Single Logical	SLL	R1,D2(B2)	89	RS
Shift Right Double(c)	SRDA	R1,D2(B2)	8E	RS
Shift Right Single(c)	SRA	R1,D2(B2)	8A	RS

(Continued)

Shift Right Double Logical	SRDL	R1,D2(B2)	8C	RS
Shift Right Single Logical	SRL	R1,D2(B2)	88	RS
Start I/O(c,p)	SIO	D1(B1)	9C	SI
Store(4)	ST	R1,D2(X2,B2)	50	RX
Store Character	STC	R1,D2(X2,B2)	42	RX
Store Halfword(2)	STH	R1,D2(X2,B2)	40	RX
Store Multiple(4)	STM	R1,R3,D2(B2)	90	RS
Subtract(c)	SR	R1,R2	1B	RR
Subtract(c,4)	S	R1,D2(X2,B2)	5B	RX
Subtract Halfword(c,2)	SH	R1,D2(X2,B2)	4B	RX
Subtract Logical(c)	SLR	R1,R2	1F	RR
Subtract Logical(c,4)	SL	R1,D2(X2,B2)	5F	RX
Supervisor Call(n,★)	SVC	I	0A	RR
Test Channel(c,p)	TCH	D1(B1)	9F	SI
Test I/O(c,p)	TIO	D1(B1)	9D	SI
Test Under Mask(c)	TM	D1(B1),I2	91	SI
Translate	TR	D1(L,B1),D2(B2)	DC	SS
Translate and Test(c)	TRT	D1(L,B1),D2(B2)	DD	SS
Unpack	UNPK	D1(L1,B1),D2(L2,B2)	F3	SS

DECIMAL FEATURE INSTRUCTIONS

Add Decimal(c)	AP	D1(L1,B1),D2(L2,B2)	FA	SS
Compare Decimal(c)	CP	D1(L1,B1),D2(L2,B2)	F9	SS
Divide Decimal	DP	D1(L1,B1),D2(L2,B2)	FD	SS
Edit(c)	ED	D1(L,B1),D2(B2)	DE	SS
Edit and Mark(c)	EDMK	D1(L,B1),D2(B2)	DF	SS
Multiply Decimal	MP	D1(L1,B1),D2(L2,B2)	FC	SS
Subtract Decimal(c)	SP	D1(L1,B1),D2(L2,B2)	FB	SS
Zero and Add(c)	ZAP	D1(L1,B1),D2(L2,B2)	F8	SS

DIRECT CONTROL FEATURE INSTRUCTIONS

Read Direct(p)	RDD	D1(B1),I2	85	SI
Write Direct(c,p)	WRD	D1(B1),I2	84	SI

PROTECTION FEATURE INSTRUCTIONS

Insert Storage Key(p)	ISK	R1,R2	09	RR
Set Storage Key(p)	SSK	R1,R2	08	RR

FLOATING-POINT FEATURE INSTRUCTIONS

Add Normalized (Long)(c,e)	ADR	R1,R2	2A	RR
Add Normalized (Long)(c,e,8)	AD	R1,D2(X2,B2)	6A	RX
Add Normalized (Short)(c,e)	AER	R1,R2	3A	RR
Add Normalized (Short)(c,e,4)	AE	R1,D2(X2,B2)	7A	RX
Add Unnormalized (Long)(c,e)	AWR	R1,R2	2E	RR
Add Unnormalized (Long)(c,e,8)	AW	R1,D2(X2,B2)	6E	RX
Add Unnormalized (Short)(c,e)	AUR	R1,R2	3E	RR
Add Unnormalized (Short)(c,e,8)	AU	R1,D2(X2,B2)	7E	RX
Compare (Long)(c,e)	CDR	R1,R2	29	RR
Compare (Long)(c,e,8)	CD	R1,D2(X2,B2)	69	RX
Compare (Short)(c,e)	CER	R1,R2	39	RR
Compare (Short)(c,e,4)	CE	R1,D2(X2,B2)	79	RX
Divide (Long)(e)	DDR	R1,R2	2D	RR
Divide (Long)(e,8)	DD	R1,D2(X2,B2)	6D	RX
Divide (Short)(e)	DER	R1,R2	3D	RR
Divide (Short)(e,4)	DE	R1,D2(X2,B2)	7D	RX
Halve (Long)(e)	HDR	R1,R2	24	RR
Halve (Short)(e)	HER	R1,R2	34	RR
Load and Test (Long)(c,e)	LTDR	R1,R2	22	RR
Load and Test (Short)(c,e)	LTER	R1,R2	32	RR
Load Complement (Long)(c,e)	LCDR	R1,R2	23	RR
Load Complement (Short)(c,e)	LCER	R1,R2	33	RR
Load (Long)(e)	LDR	R1,R2	28	RR
Load (Long)(e,8)	LD	R1,D2(X2,B2)	68	RX
Load Negative (Long)(c,e)	LNDR	R1,R2	21	RR
Load Negative (Short)(c,e)	LNER	R1,R2	31	RR

Notes for Panels 1-3

c—Condition Code is set
e—Op$_1$ = Even Reg
n—New Condition Code
p—Priviledged Instruction
*—Special Requirements
2—Halfword Boundary
4—Fullword Boundary
8—Doubleword Boundary
★—SVC operand field used as an Immediate Byte

FLOATING-POINT FEATURE INSTRUCTIONS

(Continued)

Load Positive (Long)(c,e)	LPDR	R1,R2	20	RR
Load Positive (Short)(c,e)	LPER	R1,R2	30	RR
Load (Short)(e)	LER	R1,R2	38	RR
Load (Short)(e,4)	LE	R1,D2(X2,B2)	78	RX
Multiply (Long)(e)	MDR	R1,R2	2C	RR
Multiply (Long)(e,8)	MD	R1,D2(X2,B2)	6C	RX
Multiply (Short)(e)	MER	R1,R2	3C	RR
Multiply (Short)(e,4)	ME	R1,D2(X2,B2)	7C	RX
Store (Long)	STD	R1,D2(X2,B2)	60	RX
Store (Short)	STE	R1,D2(X2,B2)	70	RX
Subtract Normalized (Long)(c,e)	SDR	R1,R2	2B	RR
Subtract Normalized (Long)(c,e,8)	SD	R1,D2(X2,B2)	6B	RX
Subtract Normalized (Short)(c,e)	SER	R1,R2	3B	RR
Subtract Normalized (Short)(c,e,4)	SE	R1,D2(X2,B2)	7B	RX
Subtract Unnormalized (Long)(c,e)	SWR	R1,R2	2F	RR
Subtract Unnormalized (Long)(c,e,8)	SW	R1,D2(X2,B2)	6F	RX
Subtract Unnormalized (Short)(c,e)	SUR	R1,R2	3F	RR
Subtract Unnormalized (Short)(c,e,4)	SU	R1,D2(X2,B2)	7F	RX

SPECIAL 9020 INSTRUCTION SET

Delay	DLY	I	0B	RR
Insert Address Translator	IATR	R1,R2	0E	RR
Load Data Address (IOCE)	LDA	R1,D2(B2)	09	RS
Load Identity	LI	R1	0C	RR
Load PSBA(p,4)	LPSB	D1(B1)	A1	SI
Move Word(4)	MVW	D1(L,B1),D2(B2)	D8	SS
Set Configuration(c,e,p)	SCON	R1,R2	01	RR
Set ATR (c,p)	SATR	R1,R2	0D	RR
Start I/O Processor(c,p,8)	SIOP	D1(B1),I2	9A	SI
Store PSBA(p,4)	SPSB	D1(B1)	A0	SI
Test and Set(c,p)	TS	D1(B1)	93	SI

DISPLAY INSTRUCTIONS — D/E System Only

Load Chain(c,4,*)	LC	R1,D2(X2,B2)	52	RX
Convert and Sort Symbols (c,*)	CSS	R1,R2	02	RR
Convert Weather Lines(*)	CVWL	R1,R2	03	RR
Repack Symbols(c,*)	RPSB	R1,R2	0F	RR

EXTENDED MNEMONIC INSTRUCTION CODES

EXTENDED CODE		MACHINE INSTRUCTION		MEANING
GENERAL				
B	D2(X2,B2)	BC	15,D2(X2,B2)	Branch Unconditionally
BR	R2	BCR	15,R2	Branch Unconditionally (RR)
NOP	D2(X2,B2)	BC	0,D2(X2,B2)	No Operation
NOPR	R2	BCR	0,R2	No Operation (RR)
AFTER COMPARE INSTRUCTIONS (A:B) **				
BE	D2(X2,B2)	BC	8,D2(X2,B2)	Branch on A Equal B
BH	D2(X2,B2)	BC	2,D2(X2,B2)	Branch on A High
BHE	D2(X2,B2)	BC	10,D2(X2,B2)	Branch on A High or Equal
BL	D2(X2,B2)	BC	4,D2(X2,B2)	Branch on A Low
BLE	D2(X2,B2)	BC	12,D2(X2,B2)	Branch on A Low or Equal
BNE	D2(X2,B2)	BC	7,D2(X2,B2)	Branch on A Not Equal B
BNH	D2(X2,B2)	BC	13,D2(X2,B2)	Branch on A Not High
BNL	D2(X2,B2)	BC	11,D2(X2,B2)	Branch on A Not Low
AFTER ARITHMETIC INSTRUCTIONS **				
BM	D2(X2,B2)	BC	4,D2(X2,B2)	Branch on Minus
BNM	D2(X2,B2)	BC	11,D2(X2,B2)	Branch on Not Minus
BNP	D2(X2,B2)	BC	13,D2(X2,B2)	Branch on Not Plus
BNZ	D2(X2,B2)	BC	7,D2(X2,B2)	Branch on Not Zero
BO	D2(X2,B2)	BC	1,D2(X2,B2)	Branch on Overflow
BP	D2(X2,B2)	BC	2,D2(X2,B2)	Branch on Plus
BV	D2(X2,B2)	BC	1,D2(X2,B2)	Branch on Overflow
BZ	D2(X2,B2)	BC	8,D2(X2,B2)	Branch on Zero
AFTER TEST UNDER MASK INSTRUCTIONS **				
BALL	D2(X2,B2)	BC	1,D2(X2,B2)	Branch if ALL Ones
BNO	D2(X2,B2)	BC	14,D2(X2,B2)	Branch if Not ALL Ones
BNON	D2(X2,B2)	BC	8,D2(X2,B2)	Branch if NO Ones
BO	D2(X2,B2)	BC	1,D2(X2,B2)	Branch if Ones
BSOM	D2(X2,B2)	BC	4,D2(X2,B2)	Branch if Some Ones
BZ	D2(X2,B2)	BC	8,D2(X2,B2)	Branch if Zeros

** RR Format instructions can be generated by adding a "R" to the mnemonic, ie., BER.

CONDITION CODE SETTING

CC =	0	1	2	3
Mask =	8	4	2	1

FLOATING-POINT ARITHMETIC

Add Normalized S/L	zero	< zero	> zero	overflow
Add Unnormalized S/L	zero	< zero	> zero	overflow
Compare S/L(A:B)	equal	A low	A high	--
Load and Test S/L	zero	< zero	> zero	--
Load Complement S/L	zero	< zero	> zero	--
Load Negative S/L	zero	< zero	--	--
Load Positive S/L	zero	--	> zero	--
Subtract Normalized S/L	zero	< zero	> zero	overflow
Subtract Unnormalized S/L	zero	< zero	> zero	overflow

FIXED-POINT ARITHMETIC

Add H/F	zero	< zero	> zero	overflow
Add Logical	zero, no carry	not zero, no carry	zero, carry	not zero, carry
Compare H/F (A:B)	equal	A low	A high	--
Load and Test	zero	< zero	> zero	--
Load Complement	zero	< zero	> zero	overflow
Load Negative	zero	< zero	--	--
Load Positive	zero	--	> zero	overflow
Shift Left Double	zero	< zero	> zero	overflow
Shift Left Single	zero	< zero	> zero	overflow
Shift Right Double	zero	< zero	> zero	--
Shift Right Single	zero	< zero	> zero	--
Subtract H/F	zero	< zero	> zero	overflow
Subtract Logical	--	not zero, no carry	zero, carry	not zero, carry

DECIMAL ARITHMETIC

Add Decimal	zero	< zero	> zero	overflow
Compare Decimal (A:B)	equal	A low	A high	--
Subtract Decimal	zero	< zero	> zero	overflow
Zero and Add	zero	< zero	> zero	overflow

LOGICAL OPERATIONS

AND	zero	not zero	--	--
Compare Logical (A:B)	equal	A low	A high	--
Edit	zero	< zero	> zero	--
Edit and Mark	zero	< zero	> zero	--
Exclusive OR	zero	not zero	--	--
OR	zero	not zero	--	--
Test Under Mask	zero	mixed	--	one
Translate and Test	zero	incomplete	complete	--

INPUT/OUTPUT OPERATIONS

Start I/O	Operation Initiated	CSW Stored	Chan./ Subchan. Busy	Not Operational
Test I/O	Device Available	CSW Stored	Chan./ Subchan. Busy	Not Operational
Halt I/O	Ch. End Interrupt Pending	CSW Stored	Burst Operation Terminated	Not Operational
Test Channel	Channel Available	Interrupt Pending	Channel Operating Burst mode	Not Operational
Set Program Control Interrupt	Subchan. Idle	CSW Stored	PCI Flag Set. I/O Interrupt Pending.	Not Operational

CNOP ALIGNMENT

DOUBLE WORD							
WORD				WORD			
HALF WORD		HALF WORD		HALF WORD		HALF WORD	
BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE
0,4 0,8		2,4 2,8		0,4 4,8		2,4 6,8	

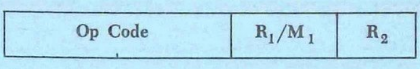
Standard Instructions

Floating-Point Feature Instructions

Decimal	Hexadecimal	Mnemonic	Graphic Symbols EBCDIC	Punched Card Code	8-bit Code
0	00			12-0-9-8-1	0000 0000
1	01	SCON		12-9-1	0000 0001
2	02	CSS*		12-9-2	0000 0010
3	03	CVWL*		12-9-3	0000 0011
4	04	SPM	PF	12-9-4	0000 0100
5	05	BALR	HT	12-9-5	0000 0101
6	06	BCTR	LC	12-9-6	0000 0110
7	07	BCR	DEL	12-9-7	0000 0111
8	08	SSK		12-9-8	0000 1000
9	09	ISK		12-9-8-1	0000 1001
10	0A	SVC		12-9-8-2	0000 1010
11	0B	DLY		12-9-8-3	0000 1011
12	0C	LI		12-9-8-4	0000 1100
13	0D	SATR		12-9-8-5	0000 1101
14	0E	IATR		12-9-8-6	0000 1110
15	0F	RPSB*		12-9-8-7	0000 1111
16	10	LPR		12-11-9-8-1	0001 0000
17	11	LNR		11-9-1	0001 0001
18	12	LTR		11-9-2	0001 0010
19	13	LCR		11-9-3	0001 0011
20	14	NR	RES	11-9-4	0001 0100
21	15	CLR	NL	11-9-5	0001 0101
22	16	OR	BS	11-9-6	0001 0110
23	17	XR	IL	11-9-7	0001 0111
24	18	LR		11-9-8	0001 1000
25	19	CR		11-9-8-1	0001 1001
26	1A	AR		11-9-8-2	0001 1010
27	1B	SR		11-9-8-3	0001 1011
28	1C	MR		11-9-8-4	0001 1100
29	1D	DR		11-9-8-5	0001 1101
30	1E	ALR		11-9-8-6	0001 1110
31	1F	SLR		11-9-8-7	0001 1111
32	20	LPDR		11-0-9-8-1	0010 0000
33	21	LNDR		0-9-1	0010 0001
34	22	LTDR		0-9-2	0010 0010
35	23	LCDR		0-9-3	0010 0011
36	24	HDR	BYP	0-9-4	0010 0100
37	25		LF	0-9-5	0010 0101
38	26		EOB	0-9-6	0010 0110
39	27		PRE	0-9-7	0010 0111
40	28	LDR		0-9-8	0010 1000
41	29	CDR		0-9-8-1	0010 1001
42	2A	ADR	SM	0-9-8-2	0010 1010
43	2B	SDR		0-9-8-3	0010 1011
44	2C	MDR		0-9-8-4	0010 1100
45	2D	DDR		0-9-8-5	0010 1101
46	2E	AWR		0-9-8-6	0010 1110
47	2F	SWR		0-9-8-7	0010 1111
48	30	LPER		12-11-0-9-8-1	0011 0000
49	31	LNER		9-1	0011 0001
50	32	LTER		9-2	0011 0010
51	33	LCER		9-3	0011 0011
52	34	HER	PN	9-4	0011 0100
53	35		RS	9-5	0011 0101
54	36		UC	9-6	0011 0110
55	37		EOT	9-7	0011 0111
56	38	LER		9-8	0011 1000
57	39	CER		9-8-1	0011 1001
58	3A	AER		9-8-2	0011 1010
59	3B	SER		9-8-3	0011 1011
60	3C	MER		9-8-4	0011 1100
61	3D	DER		9-8-5	0011 1101
62	3E	AUR		9-8-6	0011 1110
63	3F	SUR		9-8-7	0011 1111

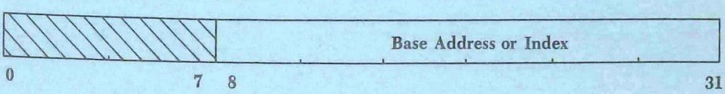
* Display instructions — D/E system only

RR Format



R1,R2 — Meaningful for all RR instructions except SPM and SVC

BASE AND INDEX REGISTERS



Standard Instructions

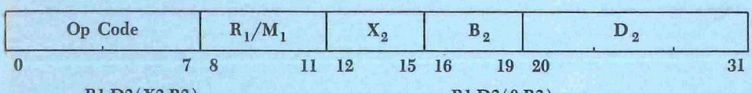
Decimal	Hexadecimal	Mnemonic	Graphic Symbols EBCDIC	Punched Card Code	8-bit Code
64	40	STH	BLANK	No Punches	0100 0000
65	41	LA		12-0-9-1	0100 0001
66	42	STC		12-0-9-2	0100 0010
67	43	IC		12-0-9-3	0100 0011
68	44	EX		12-0-9-4	0100 0100
69	45	BAL		12-0-9-5	0100 0101
70	46	BCT		12-0-9-6	0100 0110
71	47	BC		12-0-9-7	0100 0111
72	48	LH		12-0-9-8	0100 1000
73	49	CH		12-8-1	0100 1001
74	4A	AH	¢	12-8-2	0100 1010
75	4B	SH	.	12-8-3	0100 1011
76	4C	MH	<	12-8-4	0100 1100
77	4D		(	12-8-5	0100 1101
78	4E	CVD	+	12-8-6	0100 1110
79	4F	CVB	|	12-8-7	0100 1111
80	50	ST	&	12	0101 0000
81	51			12-11-9-1	0101 0001
82	52	LC*		12-11-9-2	0101 0010
83	53			12-11-9-3	0101 0011
84	54	N		12-11-9-4	0101 0100
85	55	CL		12-11-9-5	0101 0101
86	56	O		12-11-9-6	0101 0110
87	57	X		12-11-9-7	0101 0111
88	58	L		12-11-9-8	0101 1000
89	59	C		11-8-1	0101 1001
90	5A	A	!	11-8-2	0101 1010
91	5B	S	$	11-8-3	0101 1011
92	5C	M	*	11-8-4	0101 1100
93	5D	D	)	11-8-5	0101 1101
94	5E	AL	;	11-8-6	0101 1110
95	5F	SL	¬	11-8-7	0101 1111
96	60	STD	-	11	0110 0000
97	61		/	0-1	0110 0001
98	62			11-0-9-2	0110 0010
99	63			11-0-9-3	0110 0011
100	64			11-0-9-4	0110 0100
101	65			11-0-9-5	0110 0101
102	66			11-0-9-6	0110 0110
103	67			11-0-9-7	0110 0111

Floating-Point Feature Instructions

Decimal	Hexadecimal	Mnemonic	Graphic Symbols EBCDIC	Punched Card Code	8-bit Code
104	68	LD		11-0-9-8	0110 1000
105	69	CD		0-8-1	0110 1001
106	6A	AD		12-11	0110 1010
107	6B	SD	,	0-8-3	0110 1011
108	6C	MD	%	0-8-4	0110 1100
109	6D	DD	_	0-8-5	0110 1101
110	6E	AW	>	0-8-6	0110 1110
111	6F	SW	?	0-8-7	0110 1111
112	70	STE		12-11-0	0111 0000
113	71			12-11-0-9-1	0111 0001
114	72			12-11-0-9-2	0111 0010
115	73			12-11-0-9-3	0111 0011
116	74			12-11-0-9-4	0111 0100
117	75			12-11-0-9-5	0111 0101
118	76			12-11-0-9-6	0111 0110
119	77			12-11-0-9-7	0111 0111
120	78	LE		12-11-0-9-8	0111 1000
121	79	CE		8-1	0111 1001
122	7A	AE	:	8-2	0111 1010
123	7B	SE	#	8-3	0111 1011
124	7C	ME	@	8-4	0111 1100
125	7D	DE	'	8-5	0111 1101
126	7E	AU	=	8-6	0111 1110
127	7F	SU	"	8-7	0111 1111

* Display instructions — D/E system only

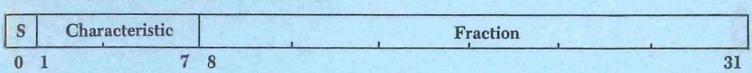
RX Format



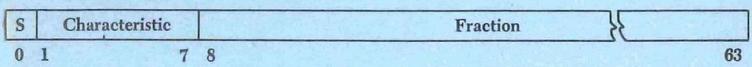
R1,D2(X2,B2)
R1,S2(X2)

R1,D2(0,B2)
R1,S2

SHORT FLOATING-POINT NUMBER

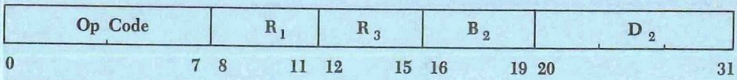


LONG FLOATING-POINT NUMBER



	Decimal	Hexadecimal	Mnemonic	Graphic Symbols EBCDIC	Punched Card Code	8-bit Code
Standard Instructions	128	80	SSM		12-0-8-1	1000 0000
	129	81		a	12-0-1	1000 0001
	130	82	LPSW	b	12-0-2	1000 0010
	131	83	DIAG	c	12-0-3	1000 0011
	132	84	WRD	d	12-0-4	1000 0100
	133	85	RDD	e	12-0-5	1000 0101
	134	86	BXH #	f	12-0-6	1000 0110
	135	87	BXLE #	g	12-0-7	1000 0111
	136	88	SRL #	h	12-0-8	1000 1000
	137	89	SLL #	i	12-0-9	1000 1001
	138	8A	SRA #		12-0-8-2	1000 1010
	139	8B	SLA #		12-0-8-3	1000 1011
	140	8C	SRDL #		12-0-8-4	1000 1100
	141	8D	SLDL #		12-0-8-5	1000 1101
	142	8E	SRDA #		12-0-8-6	1000 1110
	143	8F	SLDA #		12-0-8-7	1000 1111
	144	90	STM #		12-11-8-1	1001 0000
	145	91	TM	j	12-11-1	1001 0001
	146	92	MVI	k	12-11-2	1001 0010
	147	93	TS	l	12-11-3	1001 0011
	148	94	NI	m	12-11-4	1001 0100
	149	95	CLI	n	12-11-5	1001 0101
	150	96	OI	o	12-11-6	1001 0110
	151	97	XI	p	12-11-7	1001 0111
	152	98	LM #	q	12-11-8	1001 1000
	153	99	LDA #	r	12-11-9	1001 1001
	154	9A	SIOP		12-11-8-2	1001 1010
	155	9B	SPCI		12-11-8-3	1001 1011
	156	9C	SIO		12-11-8-4	1001 1100
	157	9D	TIO		12-11-8-5	1001 1101
	158	9E	HIO		12-11-8-6	1001 1110
	159	9F	TCH		12-11-8-7	1001 1111
	160	A0	SPSB		11-0-8-1	1010 0000
	161	A1	LPSB		11-0-1	1010 0001
	162	A2		s	11-0-2	1010 0010
Floating-Point Feature Instructions	163	A3		t	11-0-3	1010 0011
	164	A4		u	11-0-4	1010 0100
	165	A5		v	11-0-5	1010 0101
	166	A6		w	11-0-6	1010 0110
	167	A7		x	11-0-7	1010 0111
	168	A8		y	11-0-8	1010 1000
	169	A9		z	11-0-9	1010 1001
	170	AA			11-0-8-2	1010 1010
	171	AB			11-0-8-3	1010 1011
	172	AC			11-0-8-4	1010 1100
	173	AD			11-0-8-5	1010 1101
	174	AE			11-0-8-6	1010 1110
	175	AF			11-0-8-7	1010 1111
	176	B0			12-11-0-8-1	1011 0000
	177	B1			12-11-0-1	1011 0001
	178	B2			12-11-0-2	1011 0010
	179	B3			12-11-0-3	1011 0011
	180	B4			12-11-0-4	1011 0100
	181	B5			12-11-0-5	1011 0101
	182	B6			12-11-0-6	1011 0110
	183	B7			12-11-0-7	1011 0111
	184	B8			12-11-0-8	1011 1000
	185	B9			12-11-0-9	1011 1001
	186	BA			12-11-0-8-2	1011 1010
	187	BB			12-11-0-8-3	1011 1011
	188	BC			12-11-0-8-4	1011 1100
	189	BD			12-11-0-8-5	1011 1101
	190	BE			12-11-0-8-6	1011 1110
	191	BF			12-11-0-8-7	1011 1111

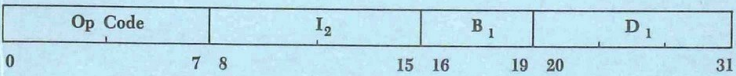
RS Format



R1,R3,D2(B2) RXH, BXLE, LDA, LM, STM
R1,R3,S2

R1,D2(B2) Shift instructions
R1,S2

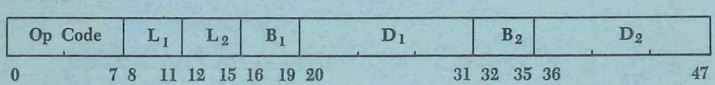
SI Format



D1(B1) LPSW, SSM, HIO, SIO
S1 SIOP, TIO, TCH, TS
D1(B1),I2
S1,I2 All other SI Instructions

Decimal	Hexadecimal	Mnemonic	Graphic Symbols EBCDIC	Punched Card Code	8-bit Code
192	C0			12-0	1100 0000
193	C1		A	12-1	1100 0001
194	C2		B	12-2	1100 0010
195	C3		C	12-3	1100 0011
196	C4		D	12-4	1100 0100
197	C5		E	12-5	1100 0101
198	C6		F	12-6	1100 0110
199	C7		G	12-7	1100 0111
200	C8		H	12-8	1100 1000
201	C9		I	12-9	1100 1001
202	CA			12-0-9-8-2	1100 1010
203	CB			12-0-9-8-3	1100 1011
204	CC			12-0-9-8-4	1100 1100
205	CD			12-0-9-8-5	1100 1101
206	CE			12-0-9-8-6	1100 1110
207	CF			12-0-9-8-7	1100 1111
208	D0			11-0	1101 0000
209	D1	MVN	J	11-1	1101 0001
210	D2	MVC	K	11-2	1101 0010
211	D3	MVZ	L	11-3	1101 0011
212	D4	NC	M	11-4	1101 0100
213	D5	CLC	N	11-5	1101 0101
214	D6	OC	O	11-6	1101 0110
215	D7	XC	P	11-7	1101 0111
216	D8	MVW	Q	11-8	1101 1000
217	D9		R	11-9	1101 1001
218	DA			12-11-9-8-2	1101 1010
219	DB			12-11-9-8-3	1101 1011
220	DC	TR		12-11-9-8-4	1101 1100
221	DD	TRT		12-11-9-8-5	1101 1101
222	DE	ED		12-11-9-8-6	1101 1110
223	DF	EDMK		12-11-9-8-7	1101 1111
224	E0			0-8-2	1110 0000
225	E1			11-0-9-1	1110 0001
226	E2		S	0-2	1110 0010
227	E3		T	0-3	1110 0011
228	E4		U	0-4	1110 0100
229	E5		V	0-5	1110 0101
230	E6		W	0-6	1110 0110
231	E7		X	0-7	1110 0111
232	E8		Y	0-8	1110 1000
233	E9		Z	0-9	1110 1001
234	EA			11-0-9-8-2	1110 1010
235	EB			11-0-9-8-3	1110 1011
236	EC			11-0-9-8-4	1110 1100
237	ED			11-0-9-8-5	1110 1101
238	EE			11-0-9-8-6	1110 1110
239	EF			11-0-9-8-7	1110 1111
240	F0		0	0	1111 0000
241	F1	MVO	1	1	1111 0001
242	F2	PACK	2	2	1111 0010
243	F3	UNPK	3	3	1111 0011
244	F4		4	4	1111 0100
245	F5		5	5	1111 0101
246	F6		6	6	1111 0110
247	F7		7	7	1111 0111
248	F8	ZAP	8	8	1111 1000
249	F9	CP	9	9	1111 1001
250	FA	AP		12-11-0-9-8-2	1111 1010
251	FB	SP		12-11-0-9-8-3	1111 1011
252	FC	MP		12-11-0-9-8-4	1111 1100
253	FD	DP		12-11-0-9-8-5	1111 1101
254	FE			12-11-0-9-8-6	1111 1110
255	FF			12-11-0-9-8-7	1111 1111

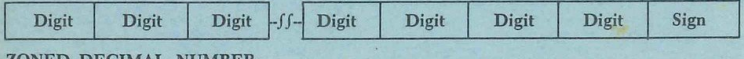
SS Format



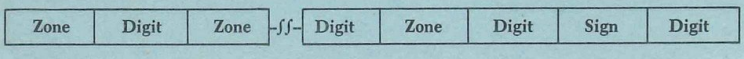
D1(L1,B1),D2(L2,B2) PACK, UNPK, MV0, AP,
S1(L1),S2(L2) CP, DP, MP, SP, ZAP

D1(L,B1),D2(B2) NC, OC, XC, CLC, MVC, MVN, MVW,
S1(L),S2 MVZ, TR, TRT, ED, EDMK

PACKED DECIMAL NUMBER



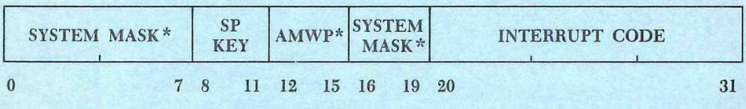
ZONED DECIMAL NUMBER

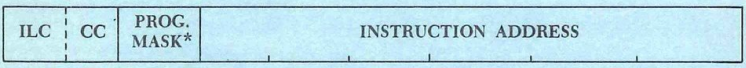


PREFERENTIAL STORAGE ASSIGNMENT

ADDRESS DEC	ADDRESS HEX	ADDRESS BINARY	LENGTH	PURPOSE
0	0	0000 0000	double-word	Initial program loading PSW
8	8	0000 1000	double-word	Initial program loading CCW1
16	10	0001 0000	double-word	Inital program loading CCW2
24	18	0001 1000	double-word	External old PSW
32	20	0010 0000	double-word	Supervsor call old PSW
40	28	0010 1000	double-word	Program old PSW
48	30	0011 0000	double-word	Machine-check old PSW
56	38	0011 1000	double-word	Input/output old PSW
64	40	0100 0000	double-word	Channel status word
72	48	0100 1000	word	Channel address word
76	4C	0100 1100	word	Unused
80	50	0101 0000	word	Timer (uses bytes 50,51,52)
84	54	0101 0100	word	Unused
88	58	0101 1000	double-word	External new PSW
96	60	0110 0000	double-word	Supervisor call new PSW
104	68	0110 1000	double-word	Program new PSW
112	70	0111 0000	double-word	Machine-check new PSW
120	78	0111 1000	double-word	Input/output new PSW
128	80	1000 0000	512 Bytes	Diagnostic logout area

PROGRAM STATUS WORD





0	Multiplexor Channel 0 Mask	16	Selector Channel 7 Mask
1	Selector Channel 1 Mask	17	Multiplexor Channel 8 Mask
2	Selector Channel 2 Mask	18	Selector Channel 9 Mask
3	Selector Channel 3 Mask	19	Selector Channel A Mask
4	Multiplexor Channel 4 Mask	20-31	Interrupt Codes — See Page 10
5	Selector Channel 5 Mask	32-33	Instruction Length Code (ILC)
6	Selector Channel 6 Mask	34-35	Condition Code (CC)
7	External Interrupt Mask	36	Fixed Point Overflow Mask
12	ASCII Mode (A)	37	Decimal Overflow Mask
13	Machine Check Mask (M)	38	Exponent Underflow Mask
14	Wait State (W)	39	Significance
15	Problem State (P)		

*A one bit permits interrupts.
A zero bit prevents interrupts.

NOTE: SYSTEM 360 PSW must have System Mask Bits 16 thru 19 equal to zero while Bits 0 thru 3 identify Channels 0 thru 3 of the IOCE being used.

NOTES

CODES FOR INTERRUPTS

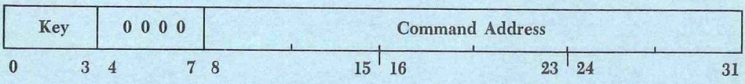
INTERRUPT SOURCE	PSW BITS 20-31	HEX	MASK BITS
I/O (OLD PSW 56; NEW PSW 120)			
Multiplexor Channel 0	0000aaaaaaaa	0--	0
Selector Channel 1	0001aaaaaaaa	1--	1
Selector Channel 2	0010aaaaaaaa	2--	2
Selector Channel 3	0011aaaaaaaa	3--	3
Multiplexor Channel 4	0100aaaaaaaa	4--	4
Selector Channel 5	0101aaaaaaaa	5--	5
Selector Channel 6	0110aaaaaaaa	6--	6
Selector Channel 7	0111aaaaaaaa	7--	16
Multiplexor Channel 8	1000aaaaaaaa	8--	17
Selector Channel 9	1001aaaaaaaa	9--	18
Selector Channel A	1010aaaaaaaa	A--	19
PROGRAM (OLD PSW 40; NEW PSW 104)			
Operation	000000000001	001	
Privileged Operation	000000000010	002	
Execute	000000000011	003	
Protection	000000000100	004	
Addressing	000000000101	005	
Specification	000000000110	006	
Data	000000000111	007	
Fixed Point Overflow	000000001000	008	36
Fixed Point Divide	000000001001	009	
Decimal Overflow	000000001010	00A	37
Decimal Divide	000000001011	00B	
Exponent Overflow	000000001100	00C	
Exponent Underflow	000000001101	00D	38
Significance	000000001110	00E	39
Floating Point Divide	000000001111	00F	
IOCE-3 PSA Lockout	000000010000	010	
IOCE-2 PSA Lockout	000000100000	020	
IOCE-1 PSA Lockout	000001000000	040	
SE Stopped	000010000000	080	
SUPERVISOR CALL (OLD PSW 32; NEW PSW 96)			
Instruction Bits	0000iiiiiiii		
EXTERNAL (OLD PSW 24; NEW PSW 88)			
DAR	----------1	--1	7
PIR	---------1-	--2	7
CE-4 Write Direct	--------1--	--4	7
CE-4 Read Direct	-------1---	--8	7
CE-3 Write Direct	------1----	-1-	7
CE-3 Read Direct	-----1-----	-2-	7
Interrupt Switch	----1------	-4-	7
Timer	---1-------	-8-	7
CE-2 Write Direct	--1--------	1--	7
CE-2 Read Direct	-1---------	2--	7
CE-1 Write Direct	1----------	4--	7
CE-1 Read Direct		8--	7
MACHINE CHECK (OLD PSW 48; NEW PSW 112)			
CE Malfunction	000000000000	000	13
IOCE-1 Malfunction	000000000001	001	13
IOCE-2 Malfunction	000000000010	002	13
IOCE-3 Malfunction	000000000011	003	13
Read Direct Timeout	000000000100	004	13

Legend

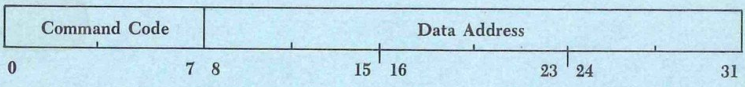
a = Unit Address Bits
i = Bits of I Field of Supervisor Call Instruction

NOTES

CHANNEL ADDRESS WORD



CHANNEL COMMAND WORD

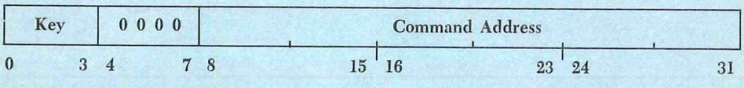


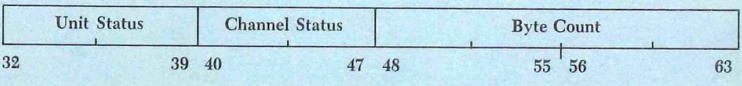
FLAG BIT ASSIGNMENTS

Bit 32 causes the address portion of the next CCW to be used. (CD)
Bit 33 causes the command code and data address in the next CCW to be used. (CC)
Bit 34 causes a possible incorrect length indication to be suppressed. (SILI)
Bit 35 suppresses the transfer of information to main storage. (SKIP)
Bit 36 causes an interruption as Program Control Interrupt. (PCI)

If Bits 32 and 33 are used together, Bit 32 takes precedence.

CHANNEL STATUS WORD





32 Attention	38 Unit Check	43 Protection check
33 Status modifier	39 Unit exception	44 Channel data check
34 Control unit end	40 Program-controlled interruption	45 Channel control check
35 Busy		46 Interface control check
36 Channel end	41 Incorrect length	47 Chaining check
37 Device end	42 Program check	

Count: Bits 48-63 form the residual count for the last CCW used.

Command Address: Bits 8-31 contain the address of the last CCW + 8.

DIRECT ACCESS DEVICES

	Command for CCW	MT Off HEX	MT Off DEC	MT On* HEX	MT On* DEC	Count
Control	Noop	03	03			Nonzero
	Recalibrate	13	19			Nonzero
	Seek	07	7			6
	Seek Cylinder	0B	11			6
	Seek Head	1B	27			6
	Sense I/O	04	4			6
	Set File Mask	1F	31			1
	Transfer In Channel	08	8			Nonzero
Search*	Home Address Equal	39	57	B9	185	4
	Identifier Equal	31	49	B1	177	5
	Identifier High	51	81	D1	209	5
	Identifier Equal or High	71	113	F1	241	5
	Key Equal	29	41	A9	169	KL
	Key High	49	73	C9	201	KL
	Key Equal or High	69	105	E9	233	KL
Read*	Home Address	1A	26	9A	154	5
	Count	12	18	92	146	8
	Record 0	16	22	96	150	DL
	Data	06	6	86	134	DL
	Key and Data	0E	14	8E	142	DL
	Count, Key and Data	1E	30	9E	158	DL
	IPL	02	2			DL
Write	Home Address	19	25			5
	Record 0	15	21			8+KL+DL of RO
	Erase	11	17			8+KL+DL
	Count, Key and Data	1D	29			8+KL+DL
	Special Count, Key and Data	01	1			8+KL+DL
	Data	05	5			DL
	Key and Data	0D	13			KL+DL

*MT On = MT Off except, during Search and Read bit 0 = 1 in MT On

KL = Key Length, DL = Data Length, RO = Record 0

DEVICE	COMMAND FOR CCW	8-BIT-CODE 0 1 2 3 4 5 6 7	HEX	DEC
1052	Read	1 0 0 0 1 0 1 0	8A	138
	Write, Auto Carriage Return	1 0 0 0 1 0 0 1	89	137
	Write, No Auto Carriage Return	1 0 0 0 0 0 0 1	81	129
	No Op	0 0 0 0 0 0 1 1	03	03
	Sense	0 0 0 0 0 1 0 0	04	04
	Transfer in Channel	0 0 0 0 1 0 0 0	08	08
2540	Read, Feed, Select Stacker SS Type AA	S S 0 0 0 0 1 0	-2	
	Read Type AB	1 1 0 0 0 0 1 0	C2	194
	Feed, Select Stacker SS Type BA	S S 1 0 0 0 1 1	-3	
	Sense	0 0 0 0 0 1 0 0	04	04
	Punch, Feed, Select Stacker SS * Type BB	S S 0 0 0 0 0 1	-1	
	No Op	0 0 0 0 0 0 1 1	03	03
	Transfer in Channel	0 0 0 0 1 0 0 0	08	08
1403	Write, No Space	0 0 0 0 0 0 0 1	01	01
	Write, Space 1 after Print	0 0 0 0 1 0 0 1	09	09
	Write, Space 2 after Print	0 0 0 1 0 0 0 1	11	17
	Write, Space 3 after Print	0 0 0 1 1 0 0 1	19	25
	Write, Skip to Channel N after Print	1 C H A N 0 0 1		
	Sense	0 0 0 0 0 1 0 0	04	04
	Transfer in Channel	0 0 0 0 1 0 0 0	08	08
Carriage Control	Space 1 Line Immediately	0 0 0 0 1 0 1 1	0B	11
	Space 2 Lines Immediately	0 0 0 1 0 0 1 1	13	19
	Space 3 Lines Immediately	0 0 0 1 1 0 1 1	1B	27
	Skip to Channel N Immediately	1 C C C C 0 1 1		
	No Op	0 0 0 0 0 0 1 1	03	03
	Transfer in Channel	0 0 0 0 1 0 0 0	08	08
2400	Transfer in Channel	0 0 0 0 1 0 0 0	08	08
	Sense	0 0 0 0 0 1 0 0	04	04
	Read Backward	0 0 0 0 1 1 0 0	0C	12
	Write	0 0 0 0 0 0 0 1	01	01
	Read	0 0 0 0 0 0 1 0	02	02
	Control	0 0 C C C 1 1 1		
	Mode Set	X X M M M 0 1 1		
7265-03 SC	Read Sense Switches	0 0 0 0 0 0 1 0	02	02
	Write Mode Indicator	0 0 0 0 0 1 0 1	05	05
	Write Conf Register	M M M M 1 0 0 1	-9	
	Control Bell	0 0 0 0 0 1 1 1	07	07
	Control Buzzer	0 0 0 0 1 0 1 1	0B	11

SS	Stacker
00	R1
01	R2
10	RP3

* SS=11 Invalid for Punch

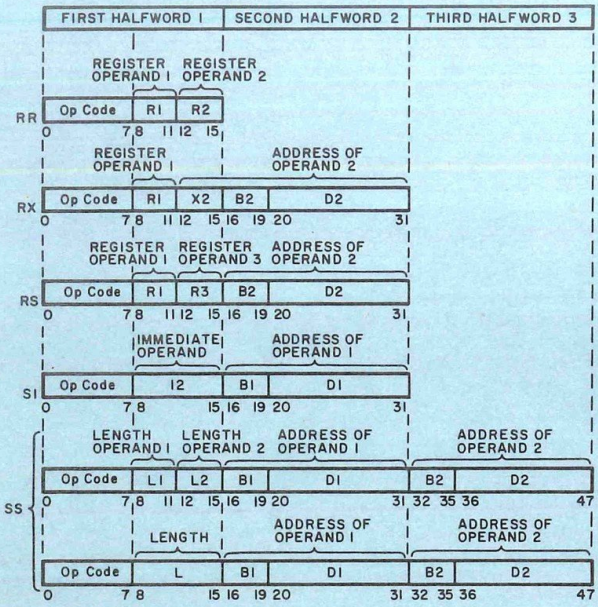
C	C	C	C	Channel
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6

C	C	C	C	Channel
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12

C	C	C	Cntrl Codes	Hex	Dec
0	0	0	REW	07	07
0	0	1	RUN	0F	15
0	1	0	ERG	17	23
0	1	1	WTM	1F	31
1	0	0	BSR	27	39
1	0	1	BSF	2F	47
1	1	0	FSR	37	55
1	1	1	FSF	3F	63

M	M	M	Mode	Hex	Dec
0	0	0	CONF	03	03
0	0	1	IF R	0B	11
0	1	0	RST	13	19
0	1	1	TIE	1B	27

M	M	M	M	Conf Reg
0	0	0	1	1
0	0	1	0	2
0	1	0	0	3
1	0	0	0	4



FIELDS IN CONTROL STATEMENTS

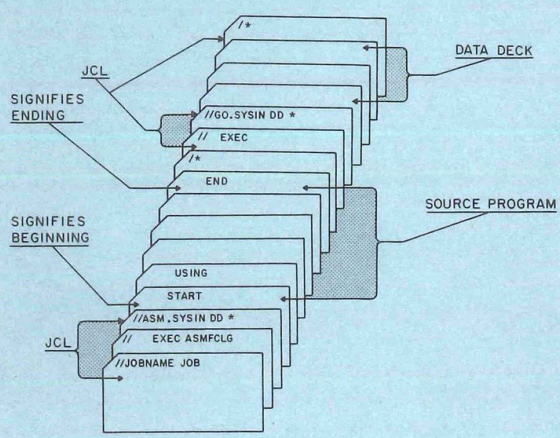
Statement	Columns 1 and 2	Fields
Job	//	name operation(JOB) operand[1] comments[1]
Execute	//	name[1] operation(EXEC) operand comments[1]
Data Definition	//	name[1] operation(DD) operand comments[1]
PROC(Cataloged)	//	name[1] operation(PROC) operand comments[1]
PROC(in-stream)	//	name operation(PROC) operand[1] comments[2]
Procedure end	//	name[1] operation(PEND) comments[1]
Command	//	operation(command) operand comments[1]
Delimiter	/*	comments[1]
Null	//	
Statement	**Columns 1,2,3**	**Field**
Comment	//*	comments

[1]Optional

[2]Optional — If operand(s) are not coded, comments cannot be coded. If operand(s) are coded, comments are optional.

Spaces — used as Delineators

JOB STREAM



Environment Required — Simplex

One 2314 SCU Min
64 K Storage Min
1052 IOT PAM or Switchable
I/O Set Print/Punch/HSP
Tapes — as required by program

IPL Reply Message:

IEA218I MOD=9020X OS/PCP Y System ID **IDENT**
IEE007A READY
X = A, D, or E
Y = IBM level of OS/PCP
IDENT = 6 character IDENT of utility PCP system

Enter Date:

t date=yy.ddd,clock=hh.mm.ss
- yy — Year
- ddd — Julian Date
- hh — Hours
- mm — Minutes
- ss — Seconds

Enter Display Jobnames & Time (both optional):

d jobnames,t

Vary printer/reader/punch online:

v cuu,online
- cuu — chan & unit address

Start SYSOUT Writer:

s wtr,cuu
- cuu — Printer Address

Start Punch:

s wtr,cuu,,b
- cuu — Punch Address
- b — Class B writer

Start SYSIN Reader:

s rdr,cuu
- cuu — Reader Address

Start Command:

s

Reply Message:

r 00, 'PN'
- 'PN' — Specifies Universal Character Set (UCS)

SUMMARY OF CONSTANTS (OS and DOS Assemblers)

TYPE	IMPLIED LENGTH, BYTES	ALIGNMENT	FORMAT	TRUNCATION/ PADDING
C	—	byte	characters	right
X	—	byte	hexadecimal digits	left
B	—	byte	binary digits	left
F	4	word	fixed-point binary	left
H	2	halfword	fixed-point binary	left
E	4	word	short floating-point	right
D	8	doubleword	long floating-point	right
L*	16	doubleword	extended floating-point	right
P	—	byte	packed decimal	left
Z	—	byte	zoned decimal	left
A	4	word	value of address	left
Y	2	halfword	value of address	left
S	2	halfword	address in base-displacement form	—
V	4	word	externally defined address value	left
Q*	4	word	symbol naming a DXD or DSECT	left

*Assembler F only

Function	*Mnemonic*	*Meaning*
Data definition	DC	Define constant
	DS	Define storage
	CCW	Define channel command word
Program	START	Start assembly
sectioning	CSECT	Identify control section
and linking	DSECT	Identify dummy section
	DXD*	Define external dummy section
	CXD*	Cumulative length of external dummy section
	COM	Identify blank common control section
	ENTRY	Identify entry-point symbol
	EXTRN	Identify external symbol
	WXTRN	Identify weak external symbol
Base register	USING	Use base address register
assignment	DROP	Drop base address register
Control of listings	TITLE	Identify assembly output
	EJECT	Start new page
	SPACE	Space listing
	PRINT	Print optional data
Program control	ICTL	Input format control
	ISEQ	Input sequence checking
	PUNCH	Punch a card
	REPRO	Reproduce following card
	ORG	Set location counter
	EQU	Equate symbol
	OPSYN	Equate operation code
	LTORG	Begin literal pool
	CNOP	Conditional no operation
	COPY	Copy predefined source coding
	END	End assembly
Macro definition	MACRO	Macro definition header
	MNOTE	Request for error message
	MEXIT	Macro definition exit
	MEND	Macro definition trailer
Conditional	ACTR	Conditional assembly loop counter
assembly	AGO	Unconditional branch
	AIF	Conditional branch
	ANOP	Assembly no operation
	GBLA	Define global SETA symbol
	GBLB	Define global SETB symbol
	GBLC	Define global SETC symbol
	LCLA	Define local SETA symbol
	LCLB	Define local SETB symbol
	LCLC	Define local SETC symbol
	SETA	Set arithmetic variable symbol
	SETB	Set binary variable symbol
	SETC	Set character variable symbol

*Assembler F Only

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE		BYTE		BYTE		BYTE		BYTE		BYTE	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

Hexadecimal-decimal fraction conversion

X	0.X	0.0X	0.00X
1	0.0625	0.00390625	0.000244140625
2	0.1250	0.00781250	0.000488281250
3	0.1875	0.01171875	0.000732421875
4	0.2500	0.01562500	0.000976562500
5	0.3125	0.01953125	0.001220703125
6	0.3750	0.02343750	0.001464843750
7	0.4375	0.02734375	0.001708984375
8	0.5000	0.03125000	0.001953125000
9	0.5625	0.03515625	0.002197265625
A	0.6250	0.03906250	0.002441406250
B	0.6875	0.04296875	0.002685546875
C	0.7500	0.04687500	0.002929687500
D	0.8125	0.05078125	0.003173828125
E	0.8750	0.05468750	0.003417968750
F	0.9375	0.05859375	0.003662109375

POWERS OF 2

2^n	n
256	8
512	9
1 024	10
2 048	11
4 096	12
8 192	13
16 384	14
32 768	15
65 536	16
131 072	17
262 144	18
524 288	19
1 048 576	20
2 097 152	21
4 194 304	22
8 388 608	23
16 777 216	24

$2^0 = 16^0$
$2^4 = 16^1$
$2^8 = 16^2$
$2^{12} = 16^3$
$2^{16} = 16^4$
$2^{20} = 16^5$
$2^{24} = 16^6$
$2^{28} = 16^7$
$2^{32} = 16^8$
$2^{36} = 16^9$
$2^{40} = 16^{10}$
$2^{44} = 16^{11}$
$2^{48} = 16^{12}$
$2^{52} = 16^{13}$
$2^{56} = 16^{14}$
$2^{60} = 16^{15}$

POWERS OF 16

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

FAA ACADEMY
DATA PROCESSING TRAINING SECTION

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