HEWLETT hp PACKARD

2100A computer

installation and maintenance manual

HEWLETT hp PACKARD

INSTALLATION AND MAINTENANCE MANUAL

MODEL 2100A COMPUTER

SERIAL NUMBERS COVERED

This manual applies directly to Model 2100A Computers having serial numbers prefixed 1136, 1140, 1145 through 1148, 1150, 1202, 1203, 1215, and 1217. Computers with higher prefix numbers will be covered in manual updating supplements.

OPTIONS COVERED

This manual covers options 001 and 015 as well as the basic computer.

ACCESSORIES COVERED

This manual covers the following accessory kits:

12884A, 12884A-001, and 12884A-002 Memory (4K Increments) Accessory Kits

12885A, 12885A-001, 12885A-002, 12885A-003, and 12885A-004 Memory (8K Increments) Accessory Kits

12895A Direct Memory Access Accessory Kit

12899A Operator Panel Accessory Kit

12900A Maintenance Accessory Kit

12901A Floating-Point Hardware Accessory Kit

Field installation of the above accessory kits is covered in separate manuals.

02100-90002

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GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION.

1-2. This Installation and Maintenance Manual, part no. 02100-90002, is one in a set of five manuals that document the Hewlett-Packard 2100A Computer (figure 1-1). The other manuals in the series are: the Reference Manual, part no. 02100-90001, the Diagrams Manual, part no. 02100-90003, the Illustrated Parts Breakdown Manual, part no. 02100-90004, and the power supply Operating and Service Manual, part no. 5951-3038. The computer is documented in the five manuals as follows:

a. This Installation and Maintenance Manual contains instructions for installation, maintenance, troubleshooting, and repair except as covered in the power supply manual.

b. The Reference manual contains specifications, operating instructions, and programming information for the computer.

c. The Diagrams Manual provides interconnecting information and schematic diagrams for all assemblies of the computer except the power supply.

d. The IPB manual contains replaceable parts ordering information, replaceable parts lists, exploded views, part location diagrams, and numerical lists of parts for all assemblies of the computer except the power supply.

e. The power supply manual contains all the information necessary to troubleshoot and repair the power supply. This includes installation instructions, schematic diagrams, and replaceable parts information.

1-3. SCOPE

1-4. This manual is intended for use by maintenance personnel who are familiar with the circuit theory and maintenance procedures of the 2100A. A thorough understanding of the information presented in the Reference Manual for the 2100A is essential to using and understanding the material presented in this manual.

1-5. The material contained in this manual includes theory of operation, testing, troubleshooting, and repair instructions for four of the five major functional sections

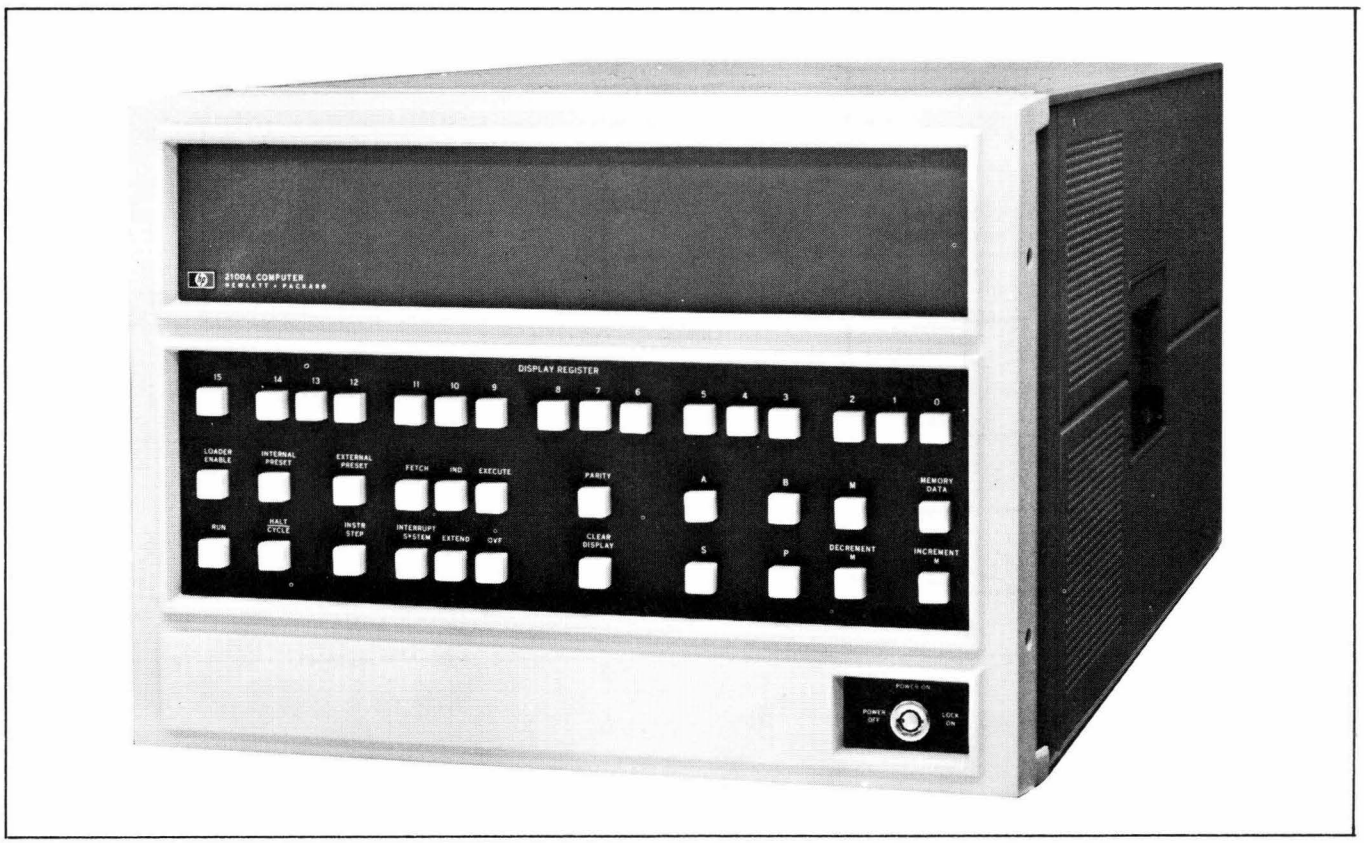

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Figure 1-1. Hewlett-Packard 2100A Computer

of the computer. These four sections are control, arithmetic, memory, and input/output (see figure 1-2).

1-6. The sections of this manual contain the following information:

a. Section I, General Information. Section I contains information for users who require knowledge of the physical makeup of the computer and an understanding of its maintenance features. Included are a description of the various electronic assemblies which comprise the computer, an explanation of the controls and indicators, a description of identification numbers used in the computer, a description of standard accessory equipment supplied with the computer, a description of the accessories and options available, an explanation of the principle built-in maintenance features, and a list of recommended servicing equipment.

b. Section II, Installation. Section II describes unpacking procedures, provides primary power data, explains initial inspection procedures, and presents instructions for installing the computer.

c. Section III, Theory of Operation. Section III describes the circuit theory of the control, arithmetic, memory, input/output, and power supply sections of the computer and its central processor accessories and options.

d. Section IV, Troubleshooting. Section IV gives procedures for fault isolation and testing. The results of these tests form the basis for fault-localizing procedures, which use the diagrams presented in the Diagrams Manual.

e. Section V, Maintenance. Section V provides preventive maintenance instructions, adjustment information, and parts removal and replacement instructions.

f. Updating Supplements. If required, updating supplements are included with this manual. These make the manual applicable to computers with serial numbers prefixed higher than those listed on the title page of this manual.

1-7. GENERAL DESCRIPTION.

1-8. COMPUTER ASSEMBLIES.

1-9. The major electronic assemblies that make up the computer are listed in table 1-1 and are shown in figures 1-3, 1-4, and 1-5. The following paragraphs describe these assemblies.

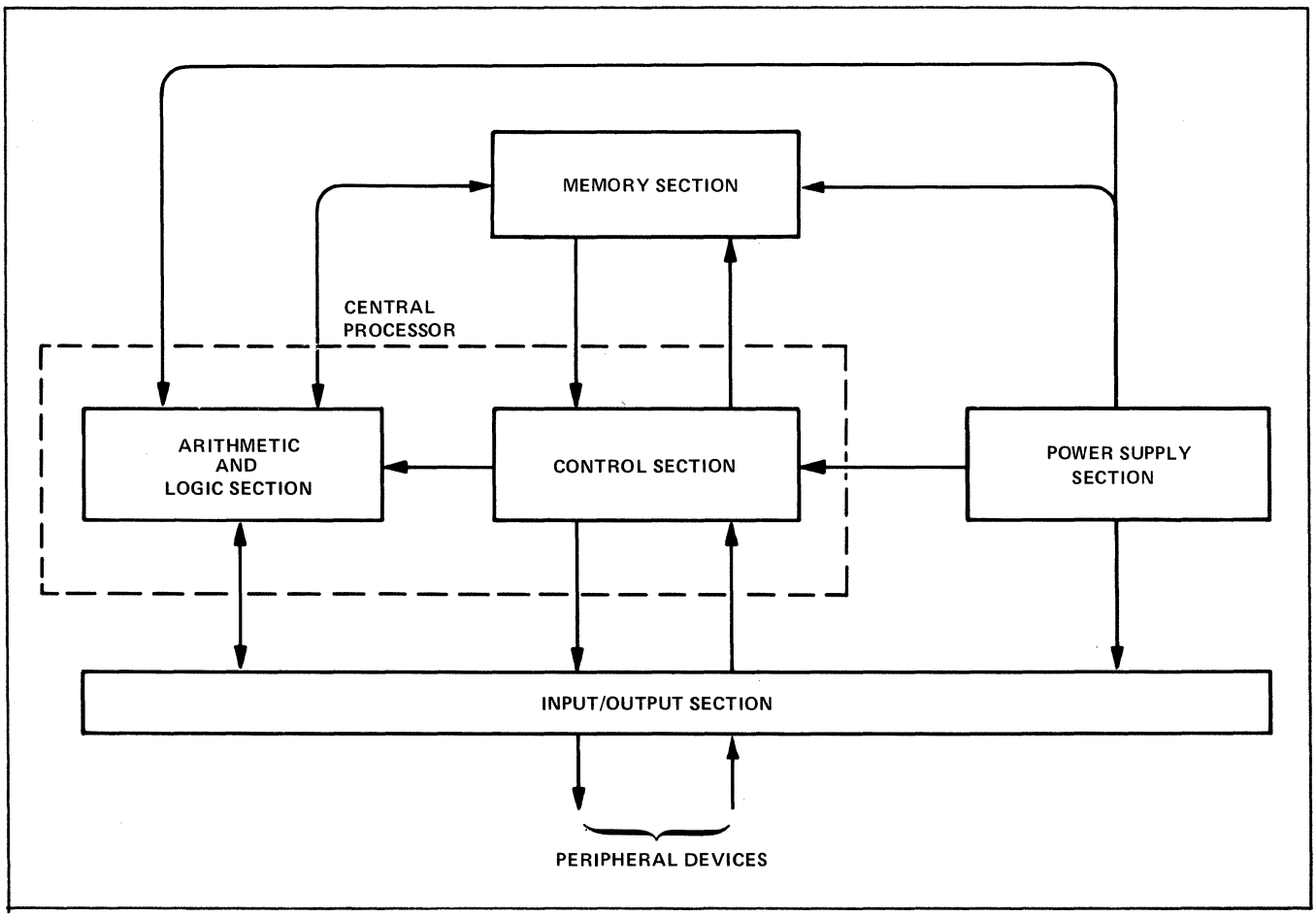

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Figure 1-2. Major Functional Sections of the 2100A Computer

Table 1-1. Major Electronic Assemblies*

REFERENCE DESIGNATION	PART NUMBER	QTY	NOMENCLATURE
A1	02100-60014	1	Timing and Control Card
A2	02100-60002	1	ROM Control Card
A3	02100-60004	1	Microinstruction Decoder 1 Card
A4	02100-60022 or 02100-60091	1	Microinstruction Decoder 2 Card
A5	02100-60001	1	Arithmetic/Logic Card
A6	02100-60003	1	Instruction Register Decoder Card
A7	02100-60024	1	I/O Control Card
A8	02100-60007	1	I/O Buffer Card
A9	12895-60001	1	Direct Memory Access (DMA) Card**
A16	02100-60060	1	I/O Terminator Card***
A24	02100-60015	1	Operator Panel
A25	02100-60053	1	Power Supply Assembly
A26	(no number)	1	Plenum Chamber Assembly

Notes:

*For assemblies contained in the memory accessory kits, refer to paragraph 1-19.
**Direct Memory Access is an accessory to the computer and not part of the basic configuration.
***I/O Terminator Card must be removed from the computer when the eighth I/O interface card is installed.

1-10. CIRCUIT CARDS. As the term is used with the 2100A Computer, a circuit card is an assembly consisting of electronic components mounted on an insulating card. An etched-foil pattern on the card makes connections between the components. The entire unit, referred to as a card, plugs into a connector on the computer. A similar unit which is permanently wired to other assemblies is referred to as a board.

1-11. The computer logic circuits are made up entirely of cards which plug into fixed connectors in the card cage. In some cases, a second connector, on the end of a flexible cable, fits on the top end of the card. Each card is assigned a reference designation beginning with the letter "A" followed by a number indicating the card cage slot in which the card is installed. Each card also has a part number. If more than one card of a given type is used, each of the cards has the same part number but a different reference designation.

1-12. Cards with reference designations A1 through A6 contain control section and arithmetic section circuits. Cards A7 through A23 contain I/O section circuits. Cards A101 through A112 contain the memory section circuits.

1-13. The cards shown in figure 1-3 are those required for the basic computer configuration. For accessory features, additional cards may be installed in the card cage.

1-14. OPERATOR PANEL. The operator panel assembly, reference designation A24, contains the computer operating controls and provides a visual indication of computer operating conditions and displays the contents of the principle computer registers. The controls are push-button type with internal indicating lamps.

1-15. POWER SUPPLY SECTION. The power supply section is located at the rear of the computer cabinet. Access to this part of the computer is gained by removing the top panel of the computer cabinet. The power supply section consists of plenum chamber assembly A26 and power supply assembly A25. The plenum chamber houses a line filter, line fuses, and two cooling fans. The computer operating voltages are also connected to test points mounted on the back panel of the plenum chamber. The function of the plenum chamber is to provide air pressure for cooling the memory section and to prevent dust from entering the memory section through the exhaust ports.

1-16. The power supply assembly, comprised of 12 subassemblies, furnishes the seven regulated dc voltages required by the computer and any optional plug-in cards installed in the computer card cage. All optional units external to the computer cabinet furnish their own ac and dc voltages derived from a separate connection to the primary ac power line. Table 1-2 lists the power supply currents available to the I/O section for I/O interface card operation.

1-17. BACKPLANE ASSEMBLY. The backplane assembly is located beneath the card cage and contains the circuit card connectors and interconnecting wiring for the plug-in cards (A1 through A23, and A101 through A112). (See figure 1-5.)

1-18. PROCESSOR ACCESSORIES.

1-19. MEMORY SIZES. Memory sizes available for the 2100A Computer are 4K, 8K, 12K, 16K, 24K, and 32K (K = 1024_{10} words). Eight accessory kits permit any of the above memory sizes to be configured at time of

Table 1-2. Power Supply Currents Available for I/O Interface Cards

SUPPLY VOLTAGE	CURRENT AVAILABLE DEPENDING ON MEMORY SIZE (AMPERES)					
	4K	8K	12K	16K	24K	32K
+30	0.1	0.1	0.1	0.1	0.1	0.1
+12	3.0	3.0	3.0	3.0	3.0	3.0
+4.85	23.6	23.6	22.7	22.7	21.6	20.8
-2	10.9	10.9	10.1	10.1	9.3	8.5
-12	3.0	3.0	3.0	3.0	3.0	3.0

NOTE: The currents specified are available with the DMA accessory kit installed.

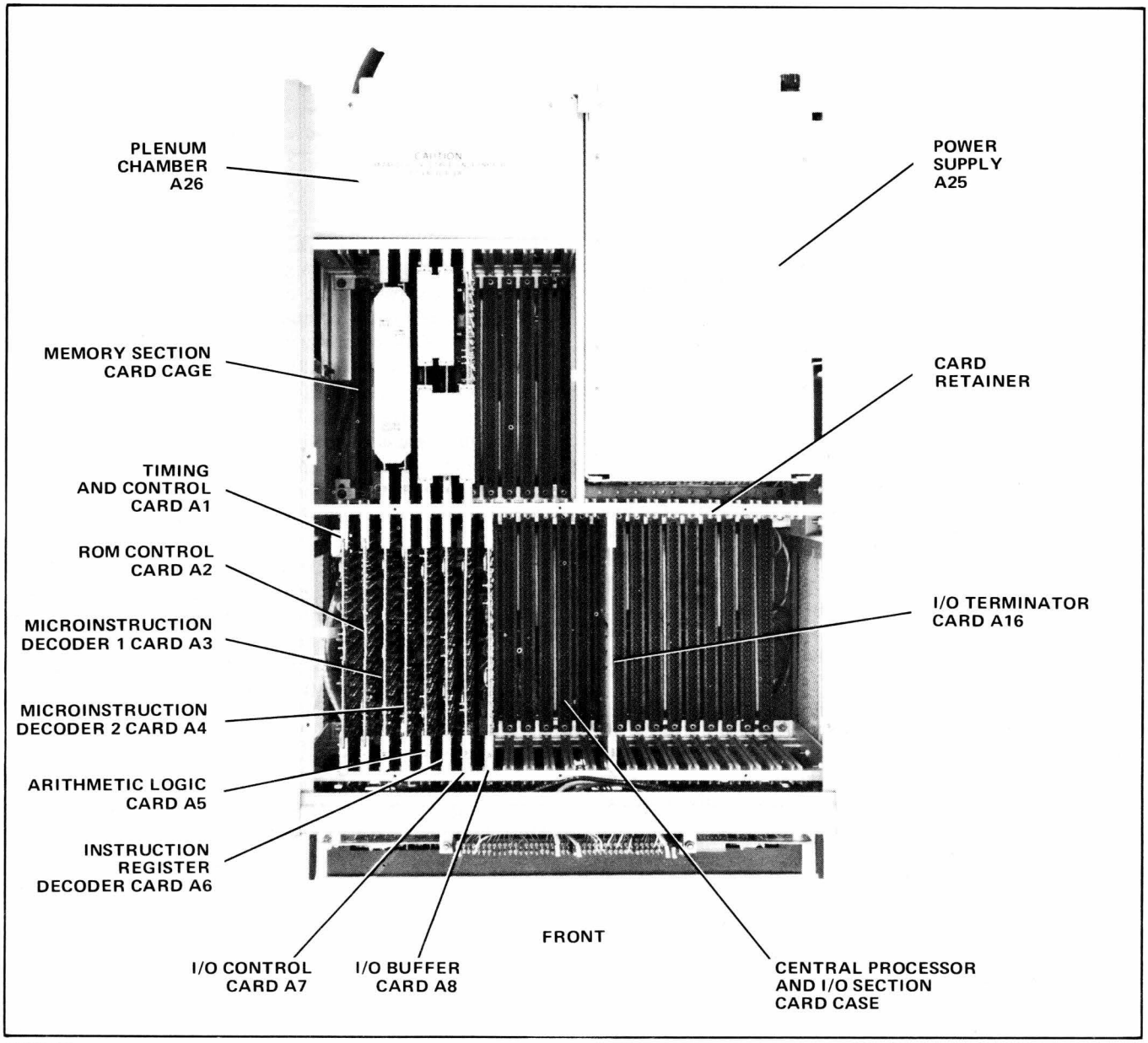

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Figure 1-3. 2100A Computer, Top View (Panel Removed)

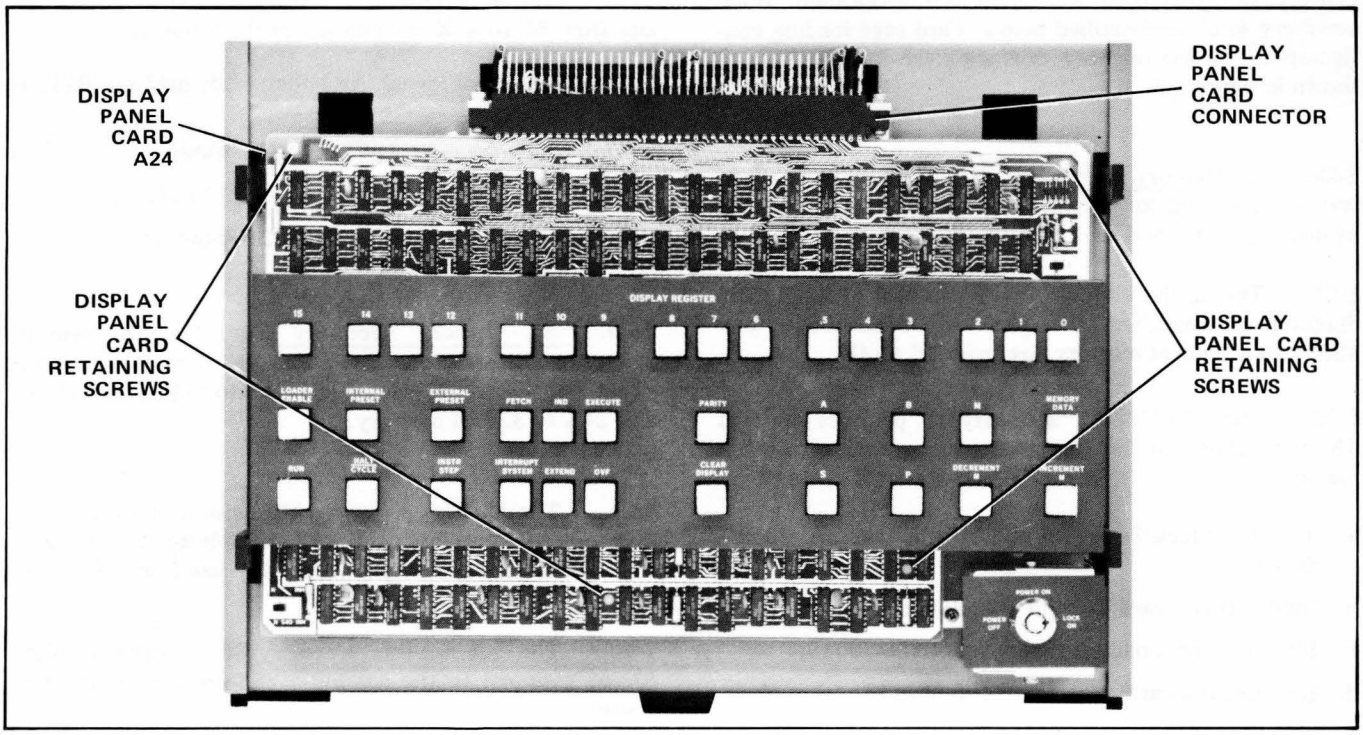

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Figure 1-4. 2100A Computer, Front View (Front Cover Removed)

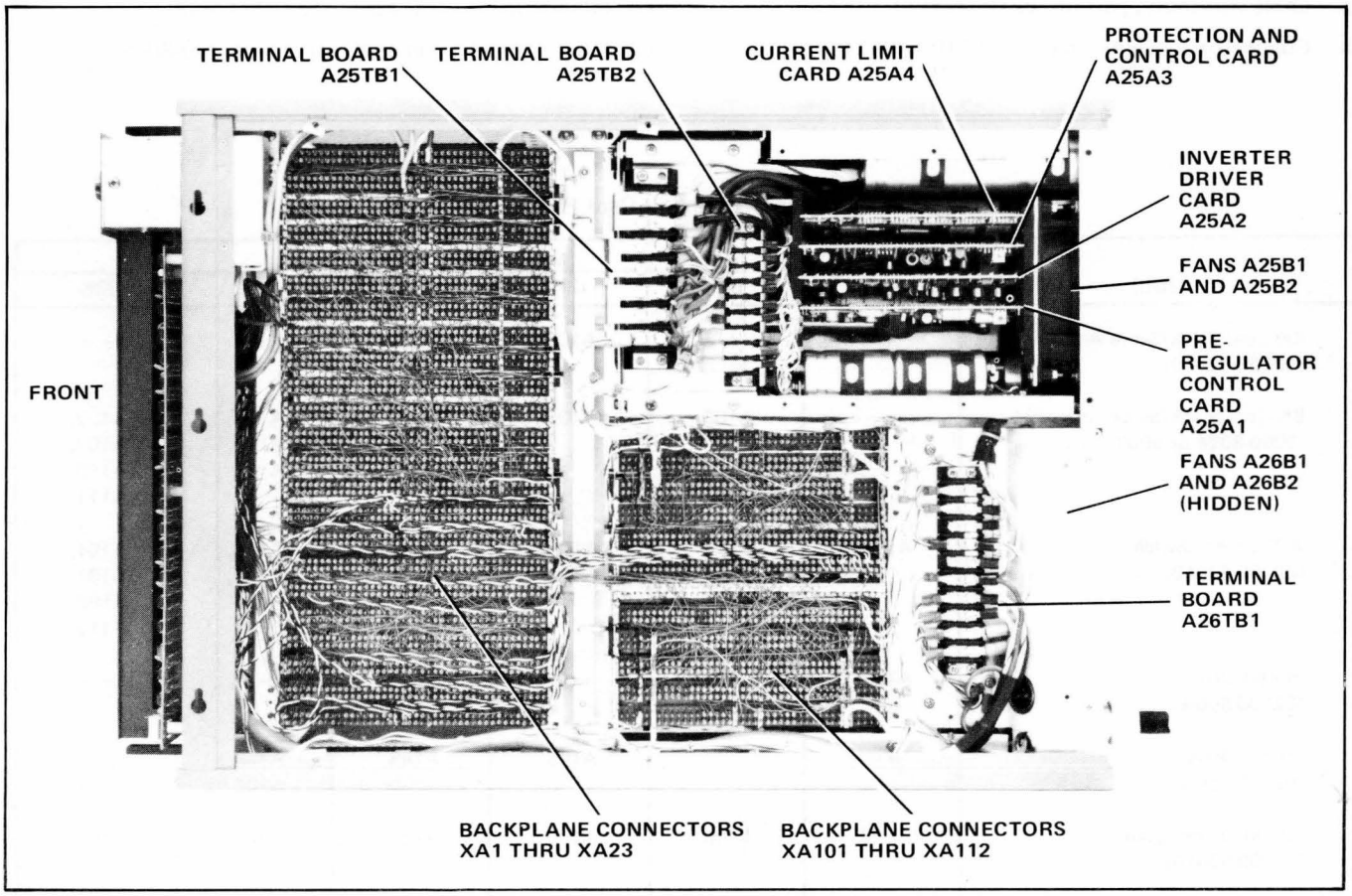

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Figure 1-5. 2100A Computer, Bottom View (Panel Removed)

delivery, or updated to a different size in the field. These accessory kits are described below. Card cage loading configurations for the memory sizes are given in table 1-3 and shown in figure 1-6.

1-20. 4K Memory Accessory Kits. The 4K memory accessory kits are used for the first 4K of memory, reducing 8K of memory to 4K, and for expanding 8K of memory to 12K.

1-21. The 12884A accessory kit consists of a 4K Core Stack/Sense Amplifier card, part no. 02100-60040. The 12884A kit reduces memory size from 8K to 4K.

1-22. The 12884A-001 accessory kit provides the first 4K of memory to the computer and consists of the following:

a. 4K Core Stack/Sense Amplifier card, part no. 02100-60040.

b. Inhibit Driver card, part no. 02100-60008.

c. Inhibit Driver Load card, part no. 02100-60010.

d. Data Control card, part no. 02100-60011.

e. X-Y Driver/Switch card, part no. 02100-60012.

f. Cable Assembly, part no. 02100-60028.

g. Cable Assembly, part no. 02100-60029.

h. Connector Assembly, part no. 02100-60054.

1-23. The 12884A-002 accessory kit expands memory size from 8K to 12K and consists of the following:

a. 4K Core Stack/Sense Amplifier card, part no. 02100-60040.

b. Inhibit Driver card, part no. 02100-60009.

c. X-Y Driver/Switch card, part no. 02100-60012.

d. Connector Assembly, part no. 02100-60052.

1-24. 8K Memory Accessory Kits. The 8K memory accessory kits are used for the first 8K of memory and for expanding 4K to 8K, 4K to 12K, 8K to 16K, 16K to 24K, and 24K to 32K of memory.

1-25. The 12885A accessory kit consists of an 8K Core Stack/Sense Amplifier card, part no. 5060-8324 or 5060-8331. The 12885A kit expands memory size from 4K to 8K.

1-26. The 12885A-001 accessory kit provides the first 8K of memory to the computer and consists of the following:

a. 8K Core Stack/Sense Amplifier card, part no. 5060-8324 or 5060-8331.

b. Inhibit Driver card, part no. 02100-60008.

c. Inhibit Driver Load card, part no. 02100-60010.

Table 1-3. Memory Section Card Part Numbers

CARD	MEMORY SIZE					
	4K	8K	12K	16K	24K	32K
4K Core Stack/Sense Amplifier (02100-60040)	A103	--	A102	--	--	--
8K Core Stack/Sense Amplifier (5060-8324 or 5060-8331)	--	A103	A103	A102, A103	A102, A103, A110	A102, A103, A110, A111
X-Y Driver/Switch (02100-60012)	A104	A104	A101, A104	A101, A104	A101, A104, A109	A101, A104, A109, A112
Inhibit Driver (02100-60008)	A105	A105	--	--	--	--
Inhibit Driver (02100-60009)	--	--	A105	A105	A105, A108	A105, A108
Inhibit Driver Load (02100-60010)	A106	A106	A106	A106	A106	A106
Data Control (02100-60011)	A107	A107	A107	A107	A107	A107

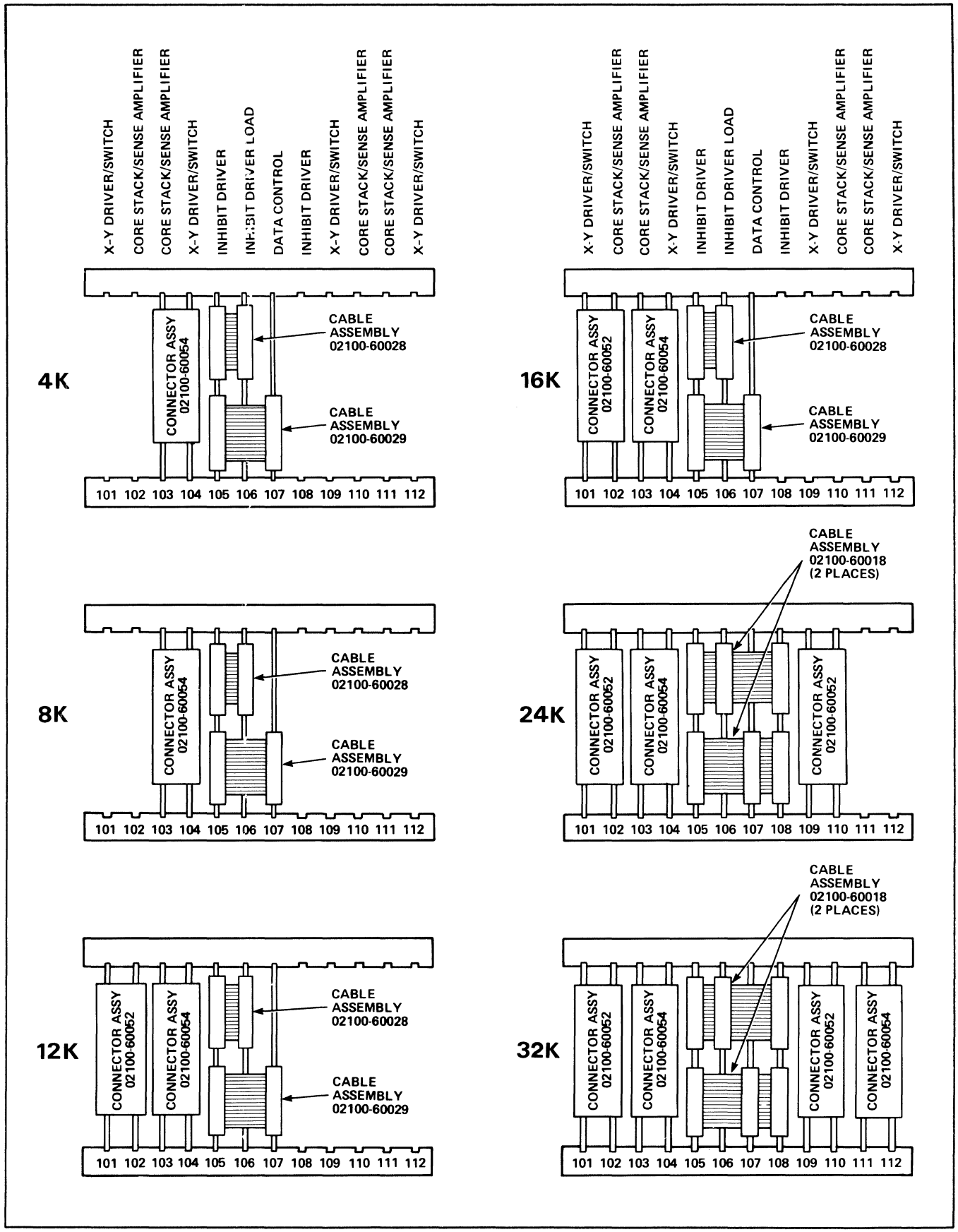

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Figure 1-6. Memory Section Card Cage Loading Configurations

d. Data Control card, part no. 02100-60011.

e. X-Y Driver/Switch card, part no. 02100-60012.

f. Cable Assembly, part no. 02100-60028.

g. Cable Assembly, part no. 02100-60029.

h. Connector Assembly, part no. 02100-60054.

1-27. The 12885A-002 accessory kit expands memory size from 4K to 12K or from 8K to 16K and consists of the following:

a. 8K Core Stack/Sense Amplifier card, part no. 5060-8324 or 5060-8331.

b. Inhibit Driver card, part no. 02100-60009.

c. X-Y Driver/Switch card, part no. 02100-60012.

d. Connector Assembly, part no. 02100-60052.

1-28. The 12885A-003 accessory kit expands memory size from 16K to 24K and consists of the following:

a. 8K Core Stack/Sense Amplifier card, part no. 5060-8324 or 5060-8331.

b. Inhibit Driver card, part no. 02100-60009.

c. X-Y Driver/Switch card, part no. 02100-60012.

d. Two Cable Assemblies, part no. 02100-60018.

e. Connector Assembly, part no. 02100-60052.

1-29. The 12885A-004 accessory kit expands memory size from 24K to 32K and consists of the following:

a. 8K Core Stack/Sense Amplifier card, part no. 5060-8324 or 5060-8331.

b. X-Y Driver/Switch card, part no. 02100-60012.

c. Connector Assembly, part no. 02100-60054.

1-30. DIRECT MEMORY ACCESSS ACCESSORY KIT (12895A). Direct memory access (DMA) enables the computer to transfer data directly between memory and external devices at a maximum rate of 1,020,400 16-bit words per second in block lengths of 1 to 32,568 words. The DMA system consists of two separate, independent, high-priority control channels. Either or both DMA channels may be switched under program control between computer memory and any external device normally serviced through the I/O system of the computer mainframe.

1-31. Any pair of devices can be run simultaneously on channel 1 (DMA 1) and channel 2 (DMA 2) provided that their combined transfer rate does not exceed 1,020,400 words per second. The computer can access memory at a rate equal to the difference between the maximum transfer rate and the amount which is actually being used by DMA 1 and DMA 2.

1-32. The 2100A DMA transfers on a full-word basis (no character packing/unpacking). DMA in the computer mainframe can be extended to the 2155A Input/Output Extender by using the 12896A DMA Extension Kit. (Refer to the 2155A Input/Output Extender Operating and Service Manual, part no. 02155-90002, for further details.)

1-33. Priority is resolved each memory cycle using the following scheme (highest to lowest priority): DMA 1, DMA 2, central processor.

1-34. The DMA accessory kit is field installable and contains one Direct Memory Access (DMA) card, part no. 12895-60001, which plugs into card cage slot 9 of the computer mainframe.

1-35. OPERATOR PANEL ACCESSORY KIT (12899A). The operator panel accessory kit is a maintenance aid for troubleshooting when the computer is configured with the controller panel, option 001. The operator panel contained in the accessory kit is identical to the operator panel mounted in the basic configuration of the 2100A Computer (refer to paragraph 1-13). The operator panel in the kit replaces the controller panel for troubleshooting.

1-36. PROCESSOR OPTIONS.

1-37. CONTROLLER PANEL (OPTION 001). The controller panel contains the minimum controls and indicators required for operating the computer in controller applications. For a description of the controls and indicators, refer to paragraph 1-41.

1-38. Jumpers (links) and a jumper configuration table, which can be viewed by removing the cover from the front of the controller panel, permit configuring the controller panel to match the computer memory size and the type of loader to be used (paper tape reader or disc memory device). (Figure 1-7 shows the jumper configuration table as it appears on the controller panel card.) Links W1 through W4 are soldered in place, as required, for specifying the correct loader starting address. This is accomplished automatically when the links correspond to the computer memory size. Link W5 specifies the type of loading device to be used.

1-39. 230-VOLT OPERATION (OPTION 015). Movable jumpers located under the plenum chamber assembly permit operation from a 230-volt source. The jumpers are placed in the appropriate position and the ac power cable fitted with a NEMA type 6-15P connector before shipment to the customer.

1-40. INPUT/OUTPUT ACCESSORIES.

1-41. Input/output accessories, such as multiplexed I/O (12894A), 2155A Input/Output Extender, and general and special purpose interface cards, are covered in separate manuals which are provided with the accessory. For information concerning these accessories, contact the nearest Hewlett-Packard Sales and Service Office.

1-42. PANEL CONTROLS AND INDICATORS.

1-43. The locations of various controls and indicators on the operator panel and controller panel are shown in figures 1-8 and 1-9. The function of each control and indicator is given in tables 1-4 and 1-5.

1-44. SPECIFICATIONS.

1-45. See table 1-6 for computer specifications.

1-46. IDENTIFICATION.

1-47. COMPUTER MODEL NUMBER.

1-48. The computer model number (2100A) is marked above the serial number on the identification label (13, figure 1-11) on the back of the computer. The model number is also marked on the front of the computer.

1-49. COMPUTER SERIAL NUMBER.

1-50. The computer is identified by a 9-digit one-letter (0000A00000) serial number marked on the identification label on the rear of the computer. The first four digits are a serial-number prefix used to indicate design changes. If the serial-number prefix on the computer does not agree with the prefix number on the title page of this manual, refer to the manual-change information contained in a supplement accompanying this manual. The letter designates the country in which the computer was manufactured ("A" indicates the United States). The remaining five digits are a sequential suffix number that changes with each computer.

1-51. OPTION NUMBERS.

1-52. On the option label at the rear of the computer, (14, figure 1-11), is marked the identifying number of each factory-installed optional feature. When optional features are supplied for installation in the field, the installation instructions require that the appropriate option number be marked in the same place as for a factory-installed option.

1-53. For a definition of option numbers, request the nearest Hewlett-Packard Sales and Service Office to furnish a list of optional features for the 2100A. (Sales and Service Offices are listed at the back of this manual.)

1-54. ASSEMBLY PART NUMBERS.

1-55. The majority of the electronic assemblies in the computer are plug-in circuit cards. Two typical cards of the type installed in the card cage are shown in figure 1-10. In the illustration, the part number is in the upper left corner of each card. Also shown in the illustration are the identifying numbers and letters of the card pins, and the means used for identifying integrated circuits (microcircuits) mounted on the card.

1-56. Assemblies other than circuit cards usually are not marked with their part number. Part numbers for these assemblies are found in the Illustrated Parts Breakdown (IPB) Manual, where all electronic assemblies are identified by their location in the computer.

1-57. CIRCUIT-CARD REVISION CODES.

1-58. Marked beneath the part number on each circuit card is a revision code (see figure 1-10). The first character of the code is a letter which identifies the etched-foil pattern on the card. The next four digits, referred to as a date code, identify the electrical characteristics of the card with components mounted. The date code is followed by a 1- or 2-digit number which identifies the Hewlett-Packard division which manufactured the assembly. The entire revision code is either stamped on the card with marking ink, or as part of the etched-foil pattern. If both a stamped and an etched code are used, the stamped revision code identifies the card with components mounted, and the etched revision code identifies the card without components.

1-59. POWER SUPPLY DATE CODE.

1-60. The power supply date code is marked on the power supply date code label at the rear of the computer. The date code, consisting of four digits, identifies the electrical configuration of the power supply assembly and is used to indicate design changes. If the date code marked on the label does not agree with the power supply date code on the title page of the power supply manual, refer to the manual change information contained in a supplement accompanying that manual.

1-61. DOCUMENTATION OF EQUIPMENT IMPROVEMENTS.

1-62. When factory changes are made in the design and construction of the computer, manuals issued with the computer cover these changes by means of an updating supplement. The factory may request that changes be made to the computer after delivery to the field. When instructions are issued for making such a change, updating supplements or change sheets are issued for all manuals affected by the change.

1-63. MAINTENANCE ACCESSORIES AND SERVICE ITEMS.

1-64. Maintenance accessories and service items for the 2100A Computer consist of a 12900A Maintenance Accessory Kit, a rack mounting kit, and five manuals. The maintenance accessory kit, available at extra cost, contains special tools and maintenance aids to facilitate maintenance of the computer. The rack mounting kit and the five manuals are furnished with the computer and need not be ordered separately. A description of the maintenance kit, rack mounting kit, and manuals is given in paragraphs 1-64 through 1-73.

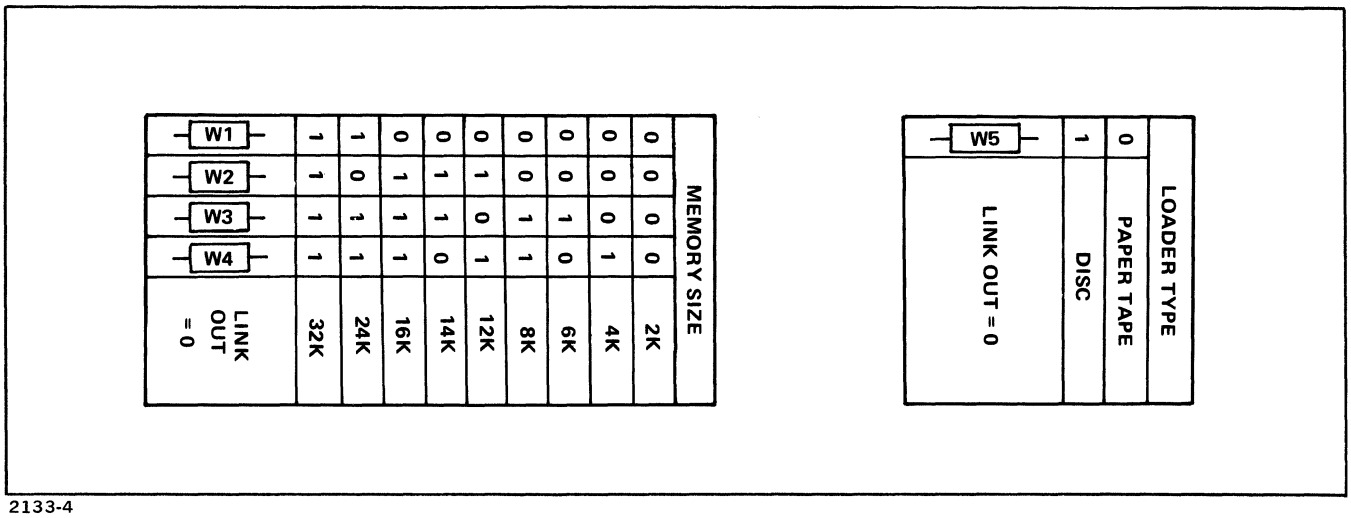

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Figure 1-7. Controller Panel Card Jumper Configurations

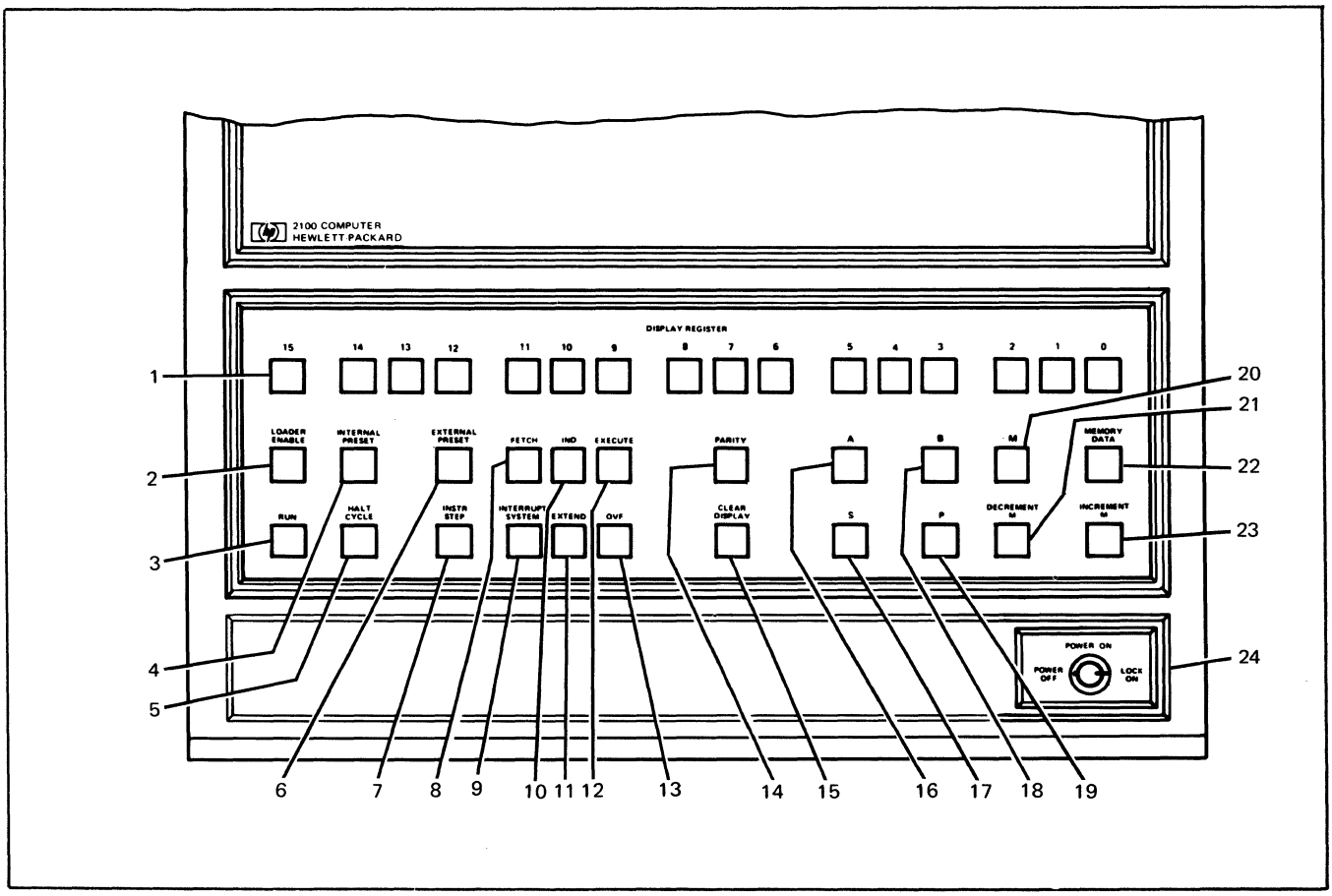

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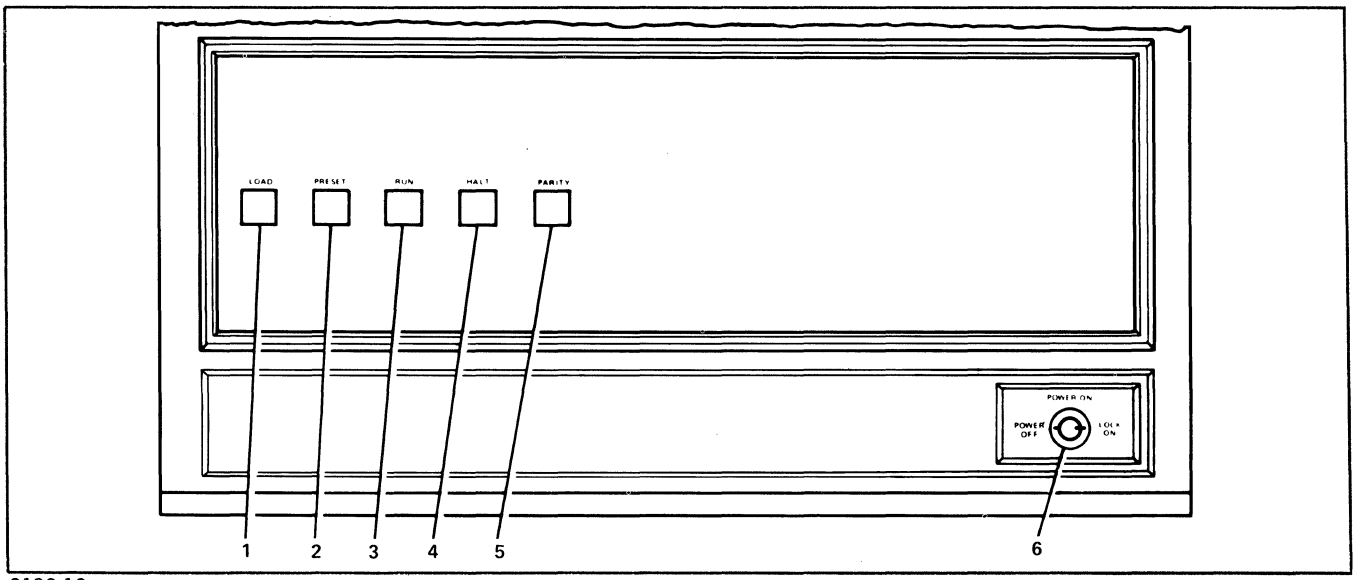
Figure 1-8. Operator Panel Controls and Indicators

Table 1-4. Operator Panel Controls and Indicators

FIGURE 1-8, INDEX NO.	NAME	FUNCTION
1	DISPLAY REGISTER	Displays the contents of the register selected by switches A, B, M, S, P, and MEMORY DATA. The contents of the selected register may be modified by pressing the appropriate switches. The computer halts with the Memory Data Register contents, or A- or B-register contents (if addressed), in the DISPLAY REGISTER.
2	LOADER ENABLE	Used to access the upper 64 memory locations (binary loader). If LOADER ENABLE is on when RUN is pressed, the binary loader is accessible. After a programmed or manual halt, the LOADER ENABLE switch is cleared and the binary loader is protected.
3	RUN (operation mode)	Used to start the computer and disable the control panel except for the HALT/CYCLE, DISPLAY REGISTER, and CLEAR DISPLAY switches. Indicator is lit when the computer is in the run mode.
4	INTERNAL PRESET	Used to preset the processor to the fetch phase, disable memory protect, clear parity error indication, clear flag 0, and clear the overflow bit.
5	HALT/CYCLE (operation mode)	In run mode: Used to halt the computer at the end of the current phase and enable the panel controls. In halt mode: Used to advance program execution by single phase increments each time HALT/CYCLE switch is pressed. Indicator is lit when computer is in halt mode and goes out momentarily when operated as single cycle.
6	EXTERNAL PRESET	Used to clear all control bits and set all flag bits at I/O addresses 6 and above. Indicator lights when control bit 4 is cleared or when EXTERNAL PRESET switch is pressed. If the computer is in the automatic restart mode, the lamp will remain lit unless extinguished by the automatic restart program or by pressing the EXTERNAL PRESET switch.
7	INSTR STEP (operation mode)	Used to advance the program execution by single instruction steps.
8	FETCH	Indicates the computer is in the fetch phase.
9	INTERRUPT SYSTEM	Indicates the state (enabled/disabled) of the interrupt system. Indicator on means interrupt system enabled. The state of the interrupt system toggles each time the INTERRUPT SYSTEM switch is pressed.
10	IND	Indicates the computer is in the indirect phase.
11	EXTEND	Indicates the state of the Extend bit. Each time the EXTEND switch is pressed, the state of the Extend bit toggles.
12	EXECUTE	Indicates the computer is in the execute phase.
13	OVF	Indicates the state of the Overflow bit. Each time the OVF switch is pressed, the state of the Overflow bit toggles.
14	PARITY	Indicates that a parity error has been detected.
15	CLEAR DISPLAY	Used to clear the DISPLAY REGISTER, if desired, while modifying its contents.
16	A (register select)	Used to display the contents of the A-register on the DISPLAY REGISTER. The contents of the A-register may be modified by altering the DISPLAY REGISTER and pressing any other register select switch or operation mode switch.
17	S (register select)	Used to display the contents of the switch (S-) register on the DISPLAY REGISTER. The contents of the S-register may be modified by altering the DISPLAY REGISTER and pressing any other register select switch or operation mode switch.
18	B (register select)	Used to display the contents of the B-register on the DISPLAY REGISTER. The contents of the B-register may be modified by altering the DISPLAY REGISTER and pressing any other register select switch or operation mode switch.

Table 1-4. Operator Panel Controls and Indicators (Continued)

FIGURE 1-8, INDEX NO.	NAME	FUNCTION
19	P (register select)	Used to display the program counter (P-) register on the DISPLAY REGISTER. The contents of the program counter register may be modified by altering the DISPLAY REGISTER and pressing any other register select switch or operation mode switch. Pressing the P switch also sets the computer to the fetch phase.
20	M (register select)	Used to display the contents of the memory address (M-) register on the DISPLAY REGISTER. The contents of the M-register may be modified by altering the DISPLAY REGISTER and pressing any other register select switch or operation mode switch.
21	DECREMENT M	Decrements the contents of the memory address register by one and updates the DISPLAY REGISTER when the memory address register or memory data register has been selected.
22	MEMORY DATA (register select)	Used to display the contents of the memory data (T-) register on the DISPLAY REGISTER. The contents of the memory data register may be modified by altering the DISPLAY REGISTER and pressing any other register select switch or operation mode switch. After a programmed or manual halt, the memory data register is automatically selected.
23	INCREMENT M	Increments the contents of the memory address register by one and updates the DISPLAY REGISTER when the memory address register or memory data register has been selected.
24	POWER	A three-position, key-operated switch to control primary power and front panel controls. POWER OFF: Key removable; primary power not applied to power supply. POWER ON: Key not removable; primary power applied to power supply; front panel controls are enabled. LOCK ON: Key removable; primary power applied to power supply; front panel controls are disabled.



2133-12

Figure 1-9. Controller Panel Controls and Indicators

Table 1-5. Controller Panel Controls and Indicators

FIGURE 1-9, INDEX NO.	NAME	FUNCTION
1	LOAD	Used to load a program from a tape reader or disc memory device. When pressed in the halt mode, loads the P-register with the loader starting address, enables the loader, and sets the computer in the run mode. The indicator lights when the loader area is being accessed. A programmed or manual halt resets the loader enable and the indicator is extinguished.
2	PRESET	Used to preset the computer to the fetch phase. When pressed in the halt mode, disables memory protect, clears parity error indication, turns off the I/O interrupt system, clears control bits and sets flag bits. In addition, presets the processor to the fetch phase and clears the A-, B-, and P-registers, and the overflow bit. The indicator lights when control 4 is cleared, or when switch is pressed. Also, indicator lights if a power failure occurred with auto-restart enabled and HLT instruction is located in trap cell 4 (memory location 4). The indicator can be extinguished by pressing the switch.
3	HALT	Used to halt the computer at the end of the current phase and enable the other panel controls. Indicator lights when computer is halted.
4	RUN	Used to set the computer to the run mode in the current phase. Other panel controls, except for HALT switch, are disabled. Indicator lights when computer is in run mode.
5	PARITY	Indicator lights when parity error has been detected. In halt mode, parity error indication can be cleared by pressing PRESET.
6	POWER	A three-position, key-operated switch to control primary power and front panel controls. POWER OFF: Key removable; primary power not applied to power supply. POWER ON: Key not removable; primary power applied to power supply; front panel controls are enabled. LOCK ON: Key removable; primary power applied to power supply; front panel controls and disabled.

1-65. MAINTENANCE ACCESSORY KIT.

1-66. The maintenance accessory kit contains two card extenders, three extension cables, a memory current sense cable, and a light bulb extractor.

1-67. CARD EXTENDERS. Two card extenders allow circuit cards in the card cage and power supply to be extended for troubleshooting. Card Extender, part no. 02116-63216 extends the card cage cards, and Card Extender, part no. 02100-60049, extends the power supply cards.

1-68. EXTENSION CABLES. Three types of extension cables are supplied with the kit. The extension cables allow cards that have a cable plugged onto their 48-pin connector, or their two 50-pin connectors, to be used with a card extender. Two Extension Cables, part no. 02100-60066, permit extension of the inhibit driver, inhibit driver load, or data control cards in the memory section. Extension Cable, part no. 02116-63251, permits extension of the X-Y driver/switch or the core stack/sense amplifier cards in the memory section. Extension Cable, part no. 02115-6047, permits extension of the interface cards in the I/O section.

1-69. MEMORY CURRENT SENSE CABLE. The Memory Current Sense Cable, part no. 02100-60067, permits monitoring individual X and Y driver/switch currents between the X-Y driver/switch card and the core stack/sense amplifier card with a current probe.

1-70. LIGHT BULB EXTRACTOR. The light bulb extractor, part no. 8710-1079, eases replacement of the indicator lamps on the operator panel and the controller panel.

1-71. RACK MOUNTING KIT.

1-72. The Rack Mounting Kit, part no. 5060-8744, allows the computer to be installed in a standard 19-inch equipment rack. Instructions for installing the rack mounting kit onto the computer are included in the kit.

Table 1-6. Specifications

POWER REQUIREMENTS

LINE VOLTAGE: 115V ac (±10 percent), single phase, 12A, or
230V ac (±10 percent), single phase, 6A

LINE FREQUENCY: 47.5 to 66 Hz (See paragraph 2-27.)

POWER CONSUMPTION: 800 watts (1400 volt-amperes), maximum

POWER CABLE

LENGTH: 10 feet (304,8 centimeters)

CONNECTOR: NEMA Type 5-15P (for 115V ac operation), or
NEMA Type 6-15P (for 230V ac operation)

DC SUPPLY VOLTAGES AND CURRENTS (COMPLETELY UNLOADED)

+30V, 0.1A
+20V, 6A
+12V, 3A
+4.85V, 50A
-2V, 23A
-12V, 3A
-20V, 0.5A

ENVIRONMENTAL LIMITS

AMBIENT TEMPERATURE RANGE

Operating: 0° to 55°C (32° to 131°F)
Non-operating: -40° to 75°C (-40° to 167°F)

RELATIVE HUMIDITY: 50 to 95 percent at 25° to 40°C (77° to 104°F) without condensation

ALTITUDE:

Operating: 15,000 feet (4572 meters)
Non-operating: 25,000 feet (7620 meters)

VENTILATION

AIR FLOW: 400 cubic feet (11,3268 cubic meters) per minute

HEAT DISSIPATION: 2300 BTUs (579,6 kilocalories) per hour, maximum

WEIGHT AND DIMENSIONS

WEIGHT: 115 pounds (52,21 kilograms) with 32K and all I/O slots filled.

HEIGHT: 12 inches (304,8 millimeters) for rack mounting
12.5 inches (317,5 millimeters) with stand-alone feet

WIDTH: 16.75 inches (425,5 millimeters)

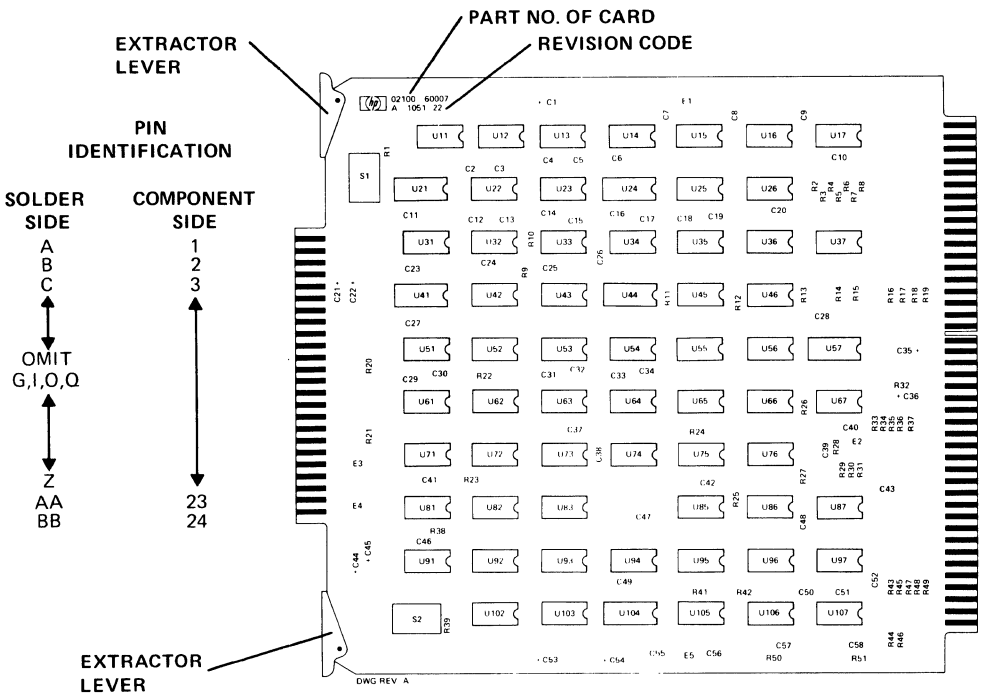
DEPTH: 26 inches (660,4 millimeters)

CLEARANCE REQUIREMENTS

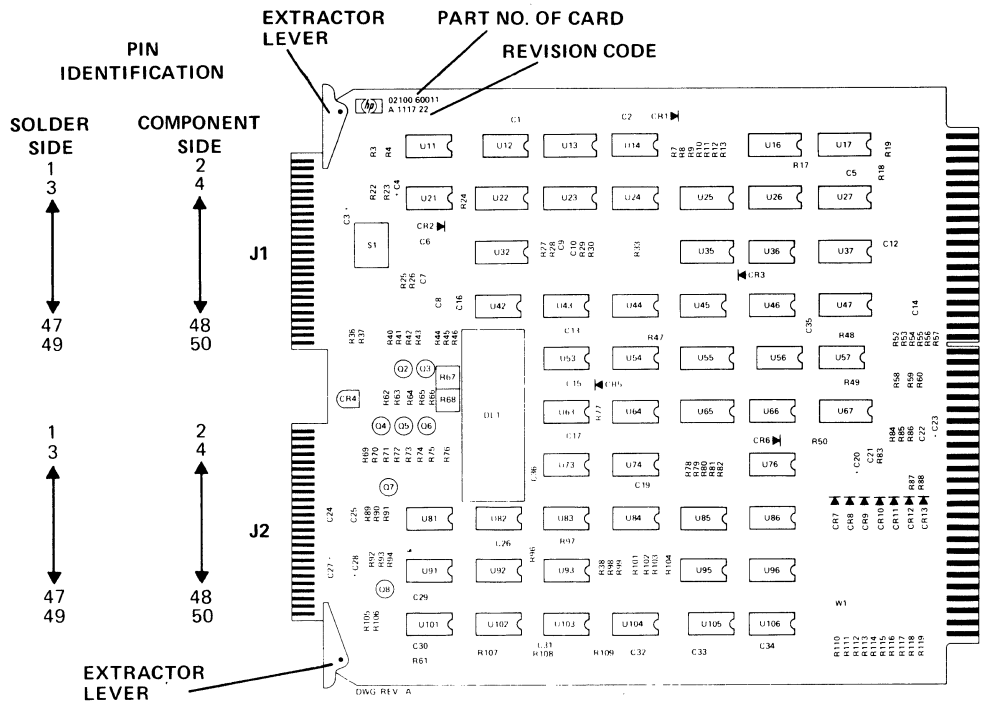
RECOMMENDED CABLE CLEARANCE AT REAR: 5 inches (127 millimeters), minimum

RECOMMENDED AIR EXHAUST CLEARANCE AT TOP: 3 inches (76,2 millimeters), minimum

RECOMMENDED AIR EXHAUST CLEARANCE AT SIDES: 2 inches (50,8 millimeters), minimum



A. ONE 48-PIN EDGE-CONNECTOR



B. TWO 50-PIN EDGE CONNECTORS

NOTE: INTEGRATED CIRCUITS ARE NUMBERED IN ROW AND COLUMN ORDER.

2133-1

Figure 1-10. Particulars of Typical Printed-Circuit Cards

1-73. MANUALS.

1-74. The five manuals furnished with the 2100A Computer are listed below:

a. 2100A Computer Reference Manual, part no. 02100-90001.

b. 2100A Computer Installation and Maintenance Manual, part no. 02100-90002.

c. 2100A Computer Diagrams Manual, part no. 02100-90003.

d. 2100A Computer Illustrated Parts Breakdown Manual, part no. 02100-90004.

e. Power Supply Operating and Service Manual, part no. 5951-3038.

1-75. MAINTENANCE FEATURES.

1-76. Major computer maintenance features for adjusting and servicing are shown in figure 1-11. The function of each feature is given in table 1-7.

1-77. RECOMMENDED MAINTENANCE TOOLS, PARTS, MATERIALS, AND EQUIPMENT.

1-78. TOOLS.

1-79. A standard electronics tool kit will provide the tools required for normal servicing of the computer. The kit should include a 30-watt soldering iron for removing and installing integrated circuits, and a rubber bulb with suction tube for withdrawing molten solder. Also recommended is a torque wrench, capable of indicating 15 pound-inches, and 3/8-inch, 7/16-inch, 1/2-inch, 9/16-inch, and 11/16-inch sockets. The torque wrench is used when replacing stud diodes in the power supply (over-torquing can damage the anodized washers).

1-80. If changes are made to the backplane wiring, wire wrapping tools are required to connect and disconnect the solderless wrapped connections on the backplane terminals. Suitable types of wire wrapping tools are listed in table 1-8. The tool part numbers listed in the table specify the proper size for the computer backplane terminals and wires. The manual wrapping tool (straight shaft) listed in table 1-8 is appropriate for use only when a few wire connections are to be wrapped at infrequent intervals. The manual wrapping tool with the pistol grip is appropriate when wiring changes are made frequently. Power-operated wire wrapping tools for more extensive wiring changes are available from the manufacturers listed.

1-81. In addition to the wiring tools, the following tool is required if a contact in a backplane connector must be replaced: A-MP TERMI-TWIST Contact Replacement Tool, Amp part no. 69514-1, for 0.031 x 0.062 inch wiring post.

1-82. The A-MP tool may be obtained from Amp Incorporated, Harrisburg, Pennsylvania. However, this tool is rarely required and it may be preferable to have backplane wiring work done by Hewlett-Packard service personnel. Hewlett-Packard Sales and Service Offices are listed at the back of this manual.

1-83. PARTS AND MATERIALS.

1-84. Spare parts that may be required for the computer are listed in the Illustrated Parts Breakdown (IPB) Manual and the power supply Operating and Service Manual. Part numbers and ordering information are included.

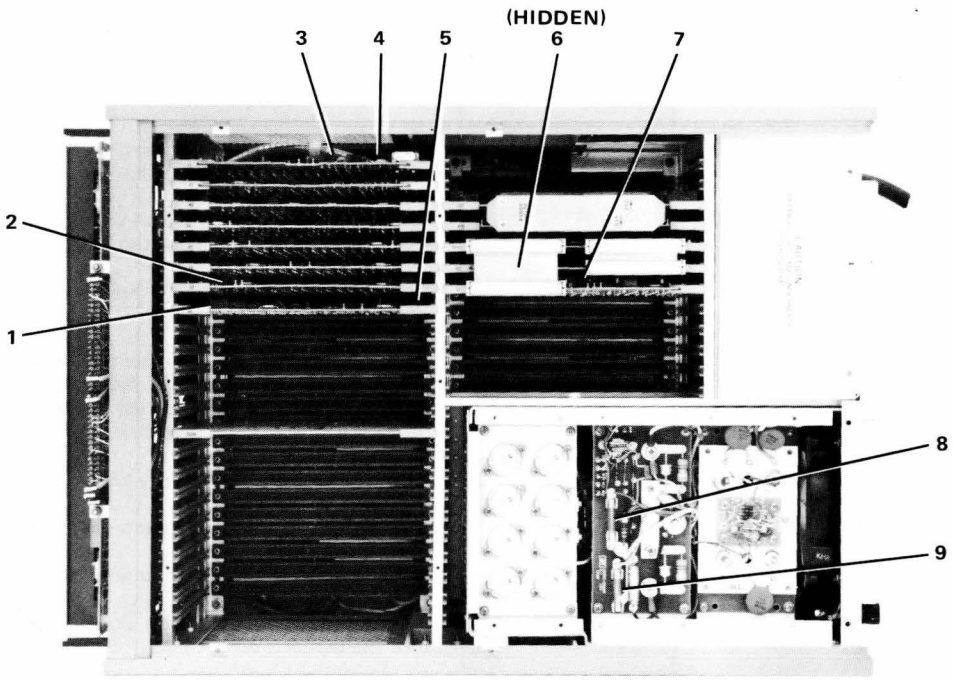
1-85. Materials and chemicals normally used for electronics service work must be available to the serviceman. These must include heat-conductive silicon compound (Wakefield 120 Thermal Joint Compound, HP part no. 6040-0239, or equivalent. When ordering the above compound, specify a 2-ounce jar.)

1-86. SERVICING EQUIPMENT.

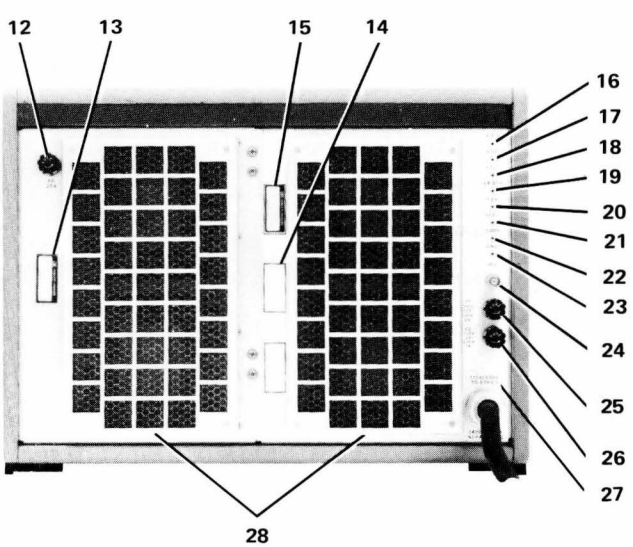
1-87. Equipment recommended for maintenance, troubleshooting, and repair of the computer is listed in table 1-9. Equipment equivalent to that specified may be substituted.

1-88. FIELD OFFICE ASSISTANCE.

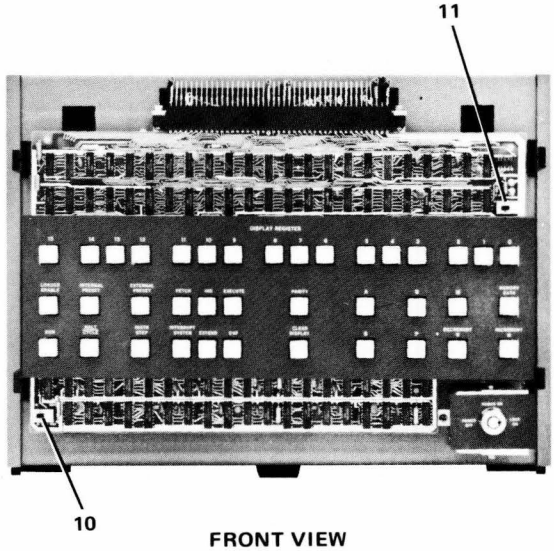
1-89. Should servicing assistance be required, contact the nearest Hewlett-Packard Sales and Service Office. These offices are listed at the back of this manual.



TOP VIEW
(TOP COVER AND POWER SUPPLY COVER REMOVED)



REAR VIEW



FRONT VIEW
(COVER REMOVED)

2133-14B

Figure 1-11. Maintenance Features of the 2100A Computer

Table 1-7. Computer Maintenance Features

FIGURE 1-11, INDEX NO.	NAME	REFERENCE DESIGNATION	FUNCTION
1	Diagnostic Switch	A8S1	(For use during special testing by HP service personnel.)
2	Auto-Restart Switch	A7S1	Permits power fail with automatic restart or power fail without automatic restart.
3	Phase Loop Switch	A1S1	Causes the computer to remain in the phase existing at the time the switch is set to loop position.
4	Instruction Loop Switch	A1S2	Causes the computer to loop on the instruction existing when the switch is set to loop position.
5	Parity Error Switch	A8S2	Permits selection of either a halt or interrupt when parity error is detected.
6	Loader Protect Switch	A107S1	Allows protection of the upper 64 memory locations when the switch is set to protect position. Overrides LOADER ENABLE switch on the operator panel when the switch is set to the "not" protect position.
7	Parity Bit Indicator	A107CR4	Indicates the state of the parity bit.
8	250 VDC, 2.5A Fuse	A25A5F1	160-volt protection for inverter assembly A25A8.
9	250 VDC, 2.5A Fuse	A25A5F2	160-volt protection for inverter assembly A25A8.
10	Memory Test Switch	A24S40	Prevents altering the contents of the DISPLAY REGISTER after the switch is set to inhibit position.
11	Operation Loop Switch	A24S39	Allows looping of an operation selected by pressing and holding one of the operator panel operation switches.
12	250 VDC, 0.25A Fuse	A25F1	+30 volt protection for I/O card slots.
13	Date Code Label	–	Provides a date code which identifies the electrical characteristics of the power supply assembly and determines technical manual effectivity.
14	Option Label	–	Identifies the optional features installed in the computer.
15	Identification Label	–	Identifies computer model number and serial number to determine technical manual effectivity.
16	+30V Test Point	A26TP1	+30 volt supply test point.
17	+20V Test Point	A26TP2	+20 volt supply test point.
18	+12V Test Point	A26TP3	+12 volt supply test point.
19	+4.85V Test Point	A26TP4	+4.85 volt supply test point.
20	-2V Test Point	A26TP5	-2 volt supply test point.
21	-12V Test Point	A26TP6	-12 volt supply test point.
22	-20V Test Point	A26TP7	-20 volt supply test point.
23	GND Test Point	A26TP8	Ground-return test point.
24	IPU connector	A26J1	Provides connection of internal power-up signal to another computer, if desired.
25	250 VAC, 12A Fuse (115V operation) 250 VAC, 6A Fuse (230V operation)	A26F1	Line voltage protection for pre-regulator assembly A25A7.

Table 1-7. Computer Maintenance Features (Continued)

FIGURE 1-11, INDEX NO.	NAME	REFERENCE DESIGNATION	FUNCTION
26	250 VAC, 2A Fuse (115V operation) 250 VAC, 1A Fuse (230V operation)	A26F2	Line voltage protection for pre-regulator control card A25A1.
27	Power Specification Label	–	Specifies power line frequency for which power failure circuits are adjusted.
28	Air Filters	–	Filters cooling air.

Table 1-8. Backplane Wiring Tools, Bits, and Sleeves

TYPE	MANUFACTURER'S PART NO.	MANUFACTURER
Manual Wrapping Tool (Straight Shaft Handle Only)	2682	Ostby and Barton 487 Jefferson Blvd. Warwick, R. I. 02886
Manual Wrapping Bit and Sleeve Assembly (For Straight Shaft Handle)	26509HW	Ostby and Barton 487 Jefferson Blvd. Warwick, R. I. 02886
Manual Unwrapping Bit and Sleeve Assembly (For Straight Shaft Handle)	20260	Ostby and Barton 487 Jefferson Blvd. Warwick, R. I. 02886
Wrapping Tool (Pistol Grip Model)	Model 963	Standard Pneumatic P. O. Box 745 Whittier, Cal. 90608
	Model 14H-IC	Gardner-Denver Co. Grand Haven, Mich. 49417
Wrapping Bit (For Pistol Grip Model)	OB-26509	Standard Pneumatic P. O. Box 745 Whittier, Cal. 90608
	37006	Gardner-Denver Co. Grand Haven, Mich. 49417
Wrapping Sleeve (For Pistol Grip Model)	OB-40200	Standard Pneumatic P. O. Box 745 Whittier, Cal. 90608
	17611-2	Gardner-Denver Co. Grand Haven, Mich. 49417

Table 1-9. Recommended Servicing Devices

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED HP MODEL
Dual-trace oscilloscope	Rise time: ≤10 ns. Vertical deflection: 1 volt/division and 10 volts/division (including attenuator probe, if used). Horizontal sweep speed: 0.1 microsecond/division to 1 second/division.	HP 180A Oscilloscope with 10004A Probe and the following plug-in units: HP 1801A Dual Channel Vertical Amplifier HP 1820A Time Base or HP 1821A Time Base and Delay Generator.
Digital voltmeter	At least 4-digit readout. Minimum input resistance: 10 megohms. Full-scale ranges: 9.999 and 99.99V dc.	HP 3439A Digital Voltmeter with HP 3441A Range Selector
AC voltmeter	Expanded-scale or digital-readout type, capable of reading the ac voltage supplied to the computer to ±1%. Voltage range must be at least 100-115 volts (for a 115-volt computer), or 200-230 volts (for a 230-volt computer).	HP3445A AC/DC Range Unit. (Also performs functions of HP 3441A Range Selector listed above. Requires HP 3439A Digital Voltmeter.)
Multimeter	Accuracy: ±3% of full scale. Full-scale ranges: 100 mV to 300V (dc and ac), 10 ohms center-scale to 10 megohms center-scale.	HP 427A
Logic probe	Indication: logic true >+1.4 volts.	HP 10525A
Variable auto-transformer	Capable of reducing computer input line-voltage to 98 volts rms (196 volts for a 230-volt computer), and able to furnish the power required by the computer (up to 1400 volt-amperes depending on the accessory features installed).	None
Centigrade thermometer	General-purpose type, accurate to ±1°C.	HP 0440-0004
High-pressure air source	25-50 psi pressure	None
Vacuum cleaner	Must have flexible hose with small nozzle, vacuum port for hose, and pressure port for hose.	None
IC test clip	None	None

NOTES:

1. The logic probe is optional. Operating voltage for the probe can be obtained from terminals 4 and 5 of A25TB1 located beneath the power supply assembly using the alligator clip on the adaptor supplied with the probe. Use care not to cause a short.

2. Ambient-temperature and humidity specifications of test equipment must suit the computer environment.

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. This section presents instructions for installing the 2100A Computer. Included are procedures for initial inspection, installation, and performance testing. Also described are claims procedures and methods of repacking the computer for shipment.

2-3. The I/O options described in the customer's order will be installed at the factory before the computer is shipped. The installation instructions for options installed in the field are shipped as part of the kit.

2-4. INSPECTION OF SHIPMENT.

2-5. The computer and its accessories may be shipped in more than one container. When the shipment is received, check the carrier's papers to ensure that all the containers have been received.

2-6. If damage to a shipping carton is evident, or if a carton is water-stained, ask the carrier's agent to be present when the carton is opened.

2-7. When ready to unpack the shipment, open the cartons and find the envelope marked "CUSTOMER RECORDS". One of the items in this envelope is a list of the equipment shipped. Check this against the original ordering papers sent to Hewlett-Packard Co., to ensure that all items correspond.

2-8. Unpack the cartons and examine each item for external damage. Look for broken controls, dented corners, bent panels, scratches, broken circuit cards, bent connector pins, and loose or broken electrical components. Also check the rigid foam-plastic cushioning material (if used) for signs of deformation which could indicate rough handling during transit.

2-9. Remove the top panel of the computer, and check for loose parts inside the computer and other signs of damage.

2-10. If the above examination reveals damage to the computer or its accessories, follow the damage-claim procedure described in paragraph 2-47. Retain the shipping containers and packing materials for examination in the settlement of claims, or for future use.

2-11. PHYSICAL INVENTORY.

2-12. MANUALS.

2-13. Check to ensure that all manuals listed in the "CUSTOMER RECORDS" envelope have been received.

2-14. EQUIPMENT.

2-15. Check the model number marked on the front panel of the computer to ensure that a 2100A has been received.

2-16. Check the model number marked on the back of the computer (figure 1-11, item 15) to ensure that a 2100A is indicated. Also check the serial number on the back of the computer and the serial number given in the "CUSTOMER RECORDS" envelope to ensure that the numbers conform. Compare the list of option numbers marked on the back of the computer to be sure that it includes all optional features listed in the "CUSTOMER RECORDS" envelope.

2-17. Check to ensure that each equipment item listed in the "CUSTOMER RECORDS" envelope has been received. In the case of certain optional features, it may be necessary to refer to the Operating and Service Manual for the option to determine how to identify it. If an option consists of more than one physical unit, make sure that all parts have been received.

2-18. PROGRAM TAPES.

2-19. Check the punched tapes received with the shipment to ensure that all tapes listed in the "CUSTOMER RECORDS" envelope have been received.

2-20. INSTALLATION PROCEDURE.

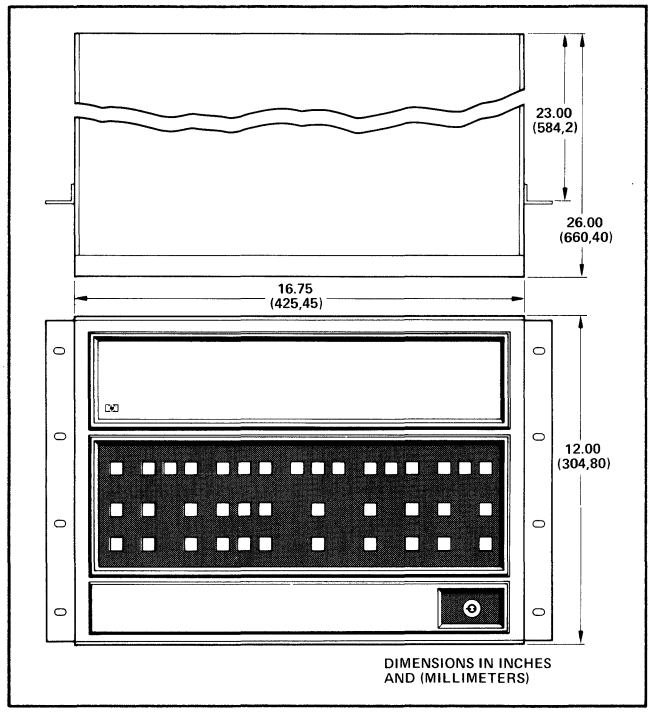
2-21. MANUAL UPDATING.

2-22. Before installing the computer, perform any updating that may be required for the Reference Manual, Installation and Maintenance Manual, Diagrams Manual, Illustrated Parts Breakdown Manual and power supply Operating and Service Manual. Check the first four digits of the computer serial number marked on the back of the computer (figure 1-11 item 15). If the computer serial-number prefix is higher than that stated on the manual title pages, one or more updating supplements are furnished with the manuals. Follow the updating instructions given in the supplements.

2-23. ENVIRONMENTAL REQUIREMENTS.

2-24. The computer must be installed in a location where the ambient temperature is between 0° and 55°C (32° and 131°F) when the computer is operating. When the computer is turned off, the permissible temperature range is between -40° and 75°C (-40° and 167°F).

2-25. Dimensional clearance requirements are shown in figure 2-1. To maintain proper cooling, there must be at least two inches of clear space at the sides of the computer. Clearance at the back must be at least five inches to permit passage of intake air and to prevent sharp bends in cables entering the computer.



2133-6

Figure 2-1. Computer Dimensions

2-26. POWER REQUIREMENTS.

2-27. The computer operates from a power source supplying an ac voltage of 115 or 230 volts rms ±10 percent, single phase. The required power frequency is 47.5 to 66 Hz. However, the power fail circuits in the power supply are line-frequency sensitive and must be adjusted to operate at the line frequency available. A label located at the rear of the computer (figure 1-11 item 27) specifies the line frequency for which the power fail circuits were adjusted before shipment from the factory. If the available line frequency is different from that marked on the label, the power fail circuits will require readjustment (refer to the power supply Operating and Service Manual). Power consumption for all voltages and frequencies is 800 watts maximum. Note that optional features not within the computer cabinet, and which make separate connection to the power line, have their own power specifications. The power they require is additional to that consumed by the computer.

2-28. Movable jumpers in the computer and the proper ac power cable permit use of the 2100A on either 115- or 230-volt power lines. The computer is shipped with the proper ac power cable and with these jumpers conneted in accordance with the customer's order. However, before the computer is connected to the power line, the jumpers must be checked as follows to ensure that they are correctly connected:

a. Make sure that the computer power cable is not plugged into a voltage source.

b. Remove the computer bottom panel and the plenum chamber bottom cover to expose terminal board A26TB1. This terminal board is mounted beneath the plenum chamber.

c. Check the jumpers on the terminal board to ensure that they are properly connected. (See figure 2-2.)

d. Replace the bottom cover and panel.

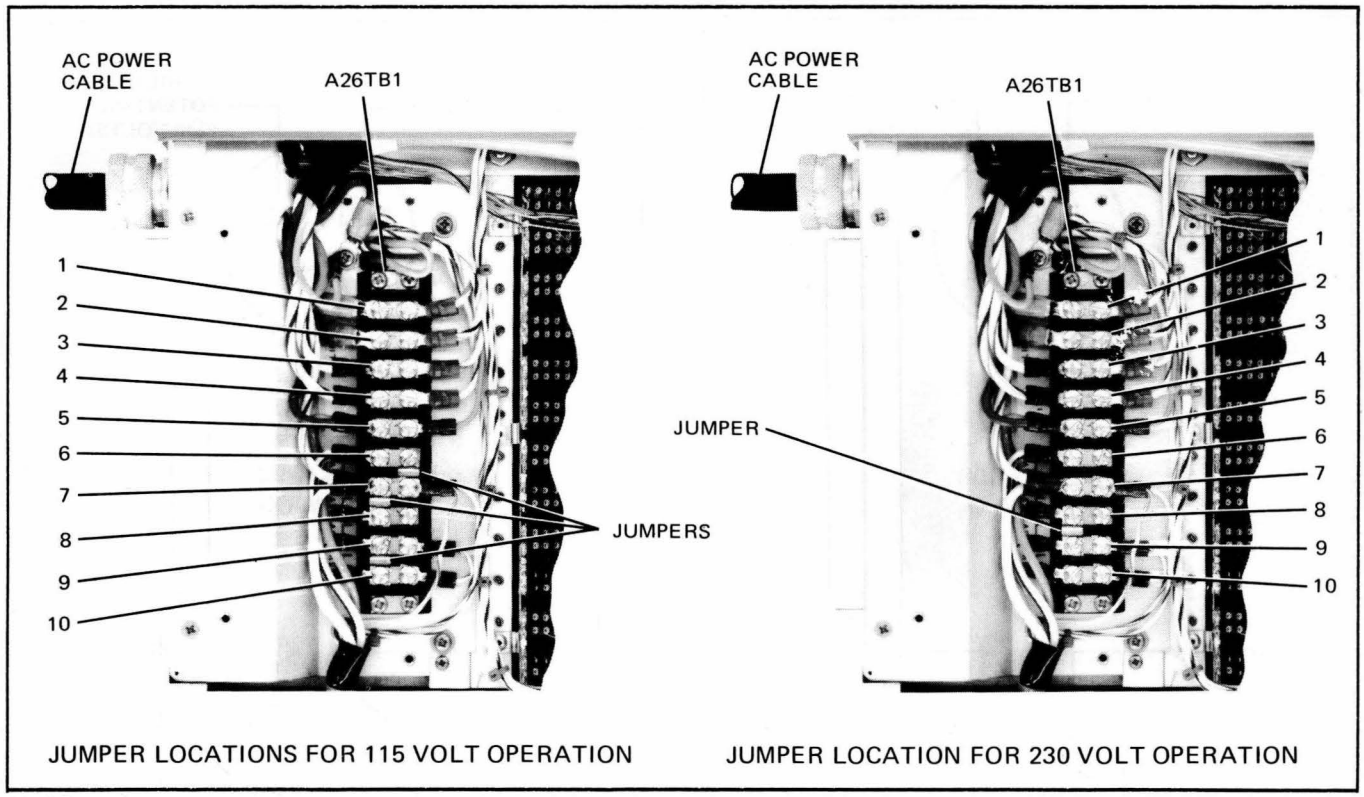
2-29. AC POWER OUTLET AND EXTERNAL GROUND.

2-30. The ac outlet which will supply power to the computer must be checked to ensure that it furnishes the voltage for which the computer is connected. Furthermore, the ac outlet and its associated wiring and fuses (or circuit breakers) must be capable of carrying at least 12 amperes for a 115-volt operation, or 6 amperes for a 230-volt operation.

2-31. If the computer is shipped for 115-volt operation, the ac power cable will fit a NEMA (National Electrical Manufacturers Association) type 5-15R or 5-20R female power outlet (figure 2-3). If the computer is shipped for 230-volt operation, the ac power cable will fit a NEMA type 6-15R or 6-20R female power outlet (figure 2-4). If the computer is to be installed in a building, make sure the local electrical codes permit use of these types of electrical outlets for the line voltage and load current used by the computer. (The 5-15R or 5-20R connector must never be used for 230-volt operation.) If necessary, change the plug on the ac power cable to fit an acceptable type of outlet, as described in paragraph 2-36.

2-32. Check at the ac outlet with a voltmeter to be sure the required voltage is supplied, and that it is single-phase. If the computer is connected for 115-volt operation, the voltage must be 103.5 to 126.5 volts ac (rms). For 230-volt operation, the voltage must be 207 to 253 volts ac (rms). Bear in mind that the electrical load imposed by the computer and its optional features may reduce the line voltage below the no-load value.

2-33. If the voltage is in the correct range, check the ac outlet to ensure that it is correctly wired with respect to high-potential ac voltage, ac neutral, and earth ground. Use a low impedance voltmeter, 20,000 ohms per volt or less, for making these measurements. If the outlet is improperly



2153-7

Figure 2-2. Jumper Locations for 115-Volt and 230-Volt Operation

wired, correction must be made by a qualified electrician, and local electrical codes must be observed if the installation is in a building.

2-34. If the electrical system has only two wires (that is, if there is no separate earth ground wire), the computer will operate with the earth ground lead in the ac power cable unconnected. However, for safety reasons, it is strongly recommended that attachment be made to a good earth ground. This connection must be made through the earth ground wire in the ac power cable used by the computer.

2-35. For installation in a ship, airplane, motor vehicle, or train, the earth ground wire in the computer ac power cable must be connected to the hull or metal frame of the vehicle.

2-36. AC POWER CABLE.

WARNING

If the plug connector at the end of the ac power cable is changed, the replacement connector must be correctly wired to the cable. If the replacement connector is incorrectly wired, fuses A26F1 and A26F2 in the computer will not remove voltage from some of the computer ac circuits when the fuse blows. The resulting high voltage at exposed terminals inside the computer presents a hazard to the serviceman. A similar situation applies when an extension cable is used.

2-37. Check the 10-foot (3-meter) ac power cable to be sure it is long enough to connect the computer to the ac outlet to be used. If a longer cable length is required, 20 feet (7 meters) maximum, the ac power cable must be cut to a 1- to 2-foot length, fitted with a proper connector, and an extension cable added. Also, make sure the connector on the extension cable fits the ac outlet. Any added cabling must have three conductors. Wire insulation on the extension cable must safely withstand at least 230 volts, and the size of each conductor must be as large as the following:

a. For a cable 10 to 15 feet (204,8 to 457,2 cm) in length:

(1) No. 12 American Wire Gauge (AWG).
(2) No. 14 British Standard Wire Gauge (SWG).
(3) No. 20 Metric Wire Gauge.

b. For a cable 15 to 20 feet (457,2 to 609,6 cm) in length:

(1) No. 10 AWG.
(2) No. 12 SWG.
(3) No. 25 Metric Wire Gauge.

2-38. If an extension cable is used, or if the connector at the end of ac power cable has been replaced, make sure that fuses A26F1 and A26F2 remain on the high-potential side of the power line. This is done as follows: (Read the entire procedure before starting.)

a. Ensure that the key-operated power switch at the front of the computer is set to OFF. Plug the extension cable,

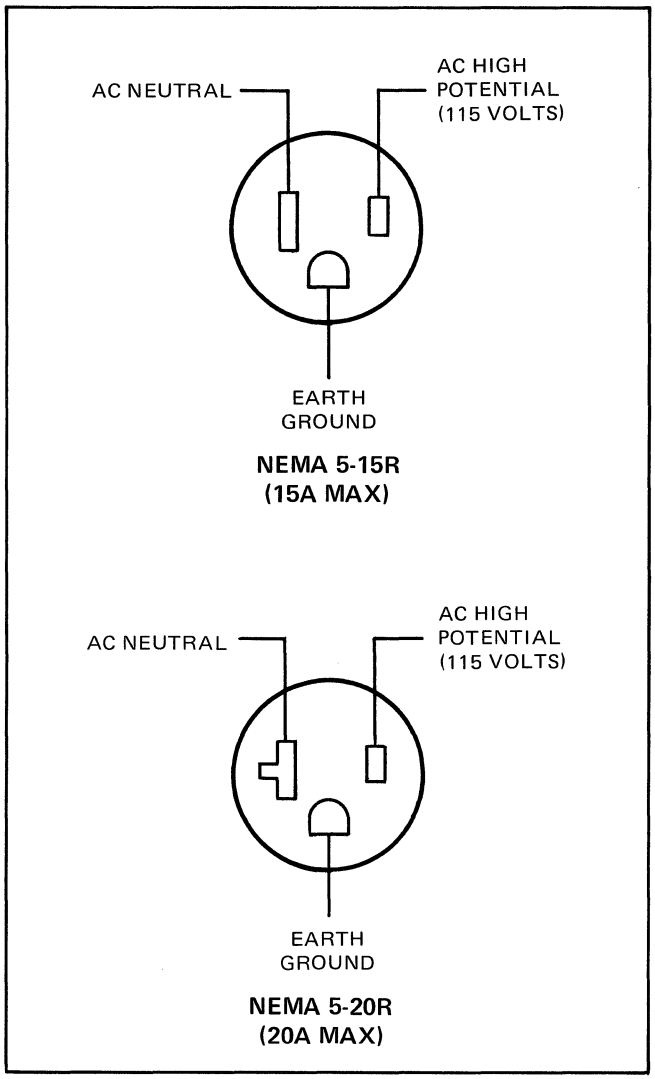


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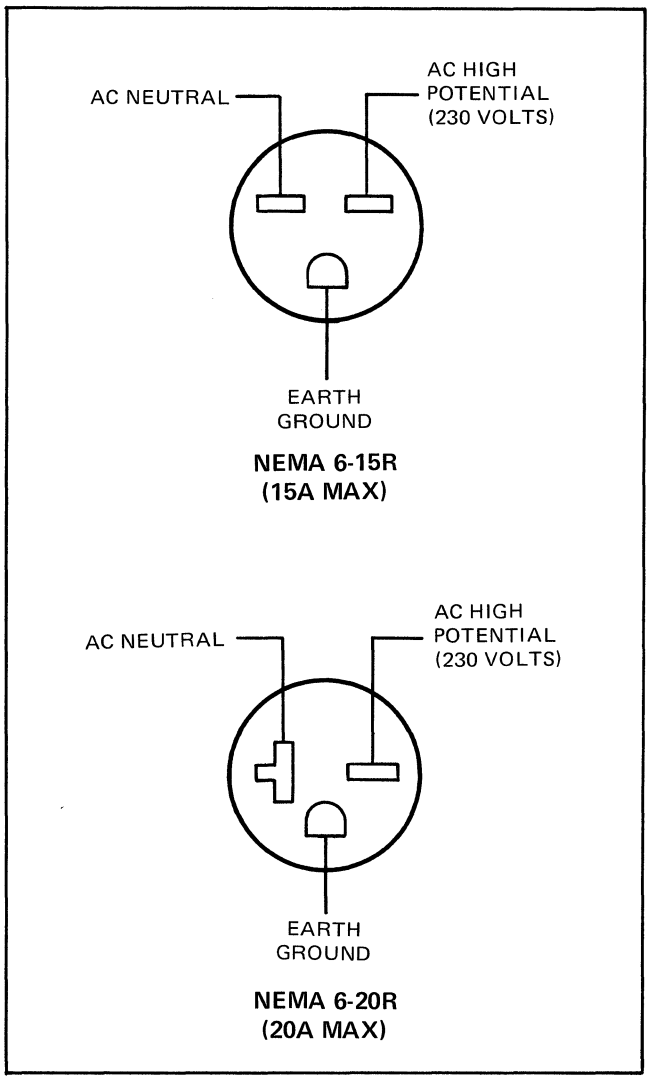
Figure 2-3. NEMA Type 5-15R and 5-20R AC Outlets, Mating Side



2133-5

Figure 2-4. NEMA Type 6-15R and 6-20R AC Outlets, Mating Side

if used, into the power cable. Do not make connection with the ac power source.

b. Set an ohmmeter to the RX100 scale, and zero the meter.

c. Connect one lead of the ohmmeter to the high-potential prong of the male connector which will plug into the ac source. (Refer to figure 2-3 or 2-4.)

d. Connect the other ohmmeter lead to terminal 4 of terminal board A26TB1. (See figure 2-5 for terminal identifications.)

e. Check the ohmmeter reading. The reading should be approximately zero (see figure 2-6). If the reading is infinite, the power cable connections are incorrect. Make the necessary corrections as described in step "k" below.

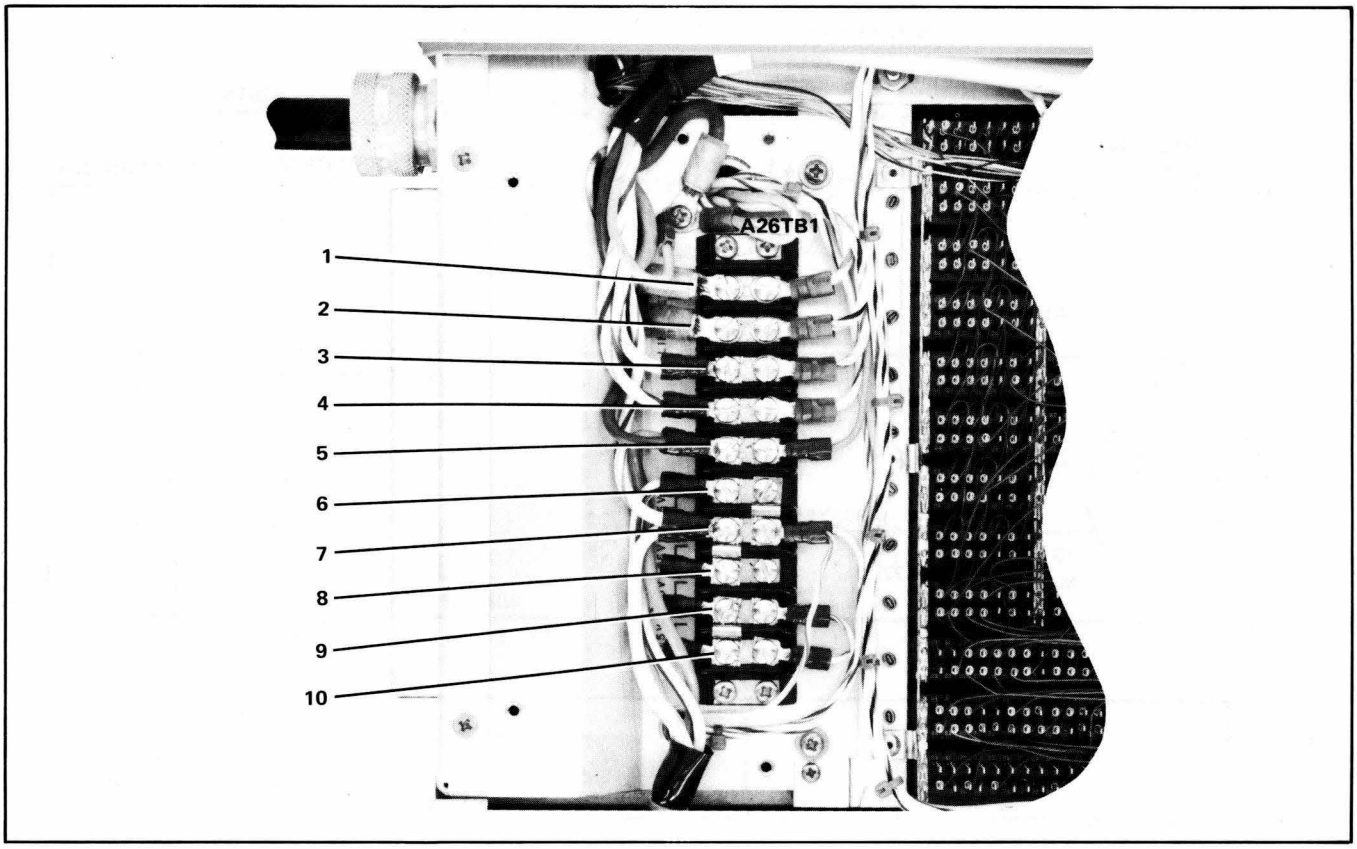
f. If the test in step "e" is correct, remove fuse A26F1. (See figure 1-11, item 24 for fuse location.) The ohmmeter reading should be infinite. If not, the power cable connections are incorrect. Install the fuse.

g. If the test in step "f" is correct, remove the ohmmeter lead from the high potential prong of the power connector, and connect it to the ac neutral prong of the connector.

h. Remove the other ohmmeter lead from terminal 4 of terminal board A26TB1, and connect it to terminal 3.

i. Check the ohmmeter reading. The reading should be approximately zero. If not, the power cable connections are incorrect.

j. If step "i" is satisfactory, check the resistance between the earth ground prong of the power connector and the



2133-16A

Figure 2-5. Terminal Identification for AC Power Cable Check

frame of the computer. Zero ohms should be indicated. If the reading is infinite, the power cable is incorrectly wired.

k. If any of the preceding measurements is incorrect, make the necessary changes in connector wiring. If an extension cable is used, change connections in one of the extension-cable connectors, rather than in the factory-wired ac power cable. After making the correction, repeat the entire procedure, starting with step "b" preceding.

l. Remove all circuit cards from the computer card cage (leave power supply cards in place).

WARNING

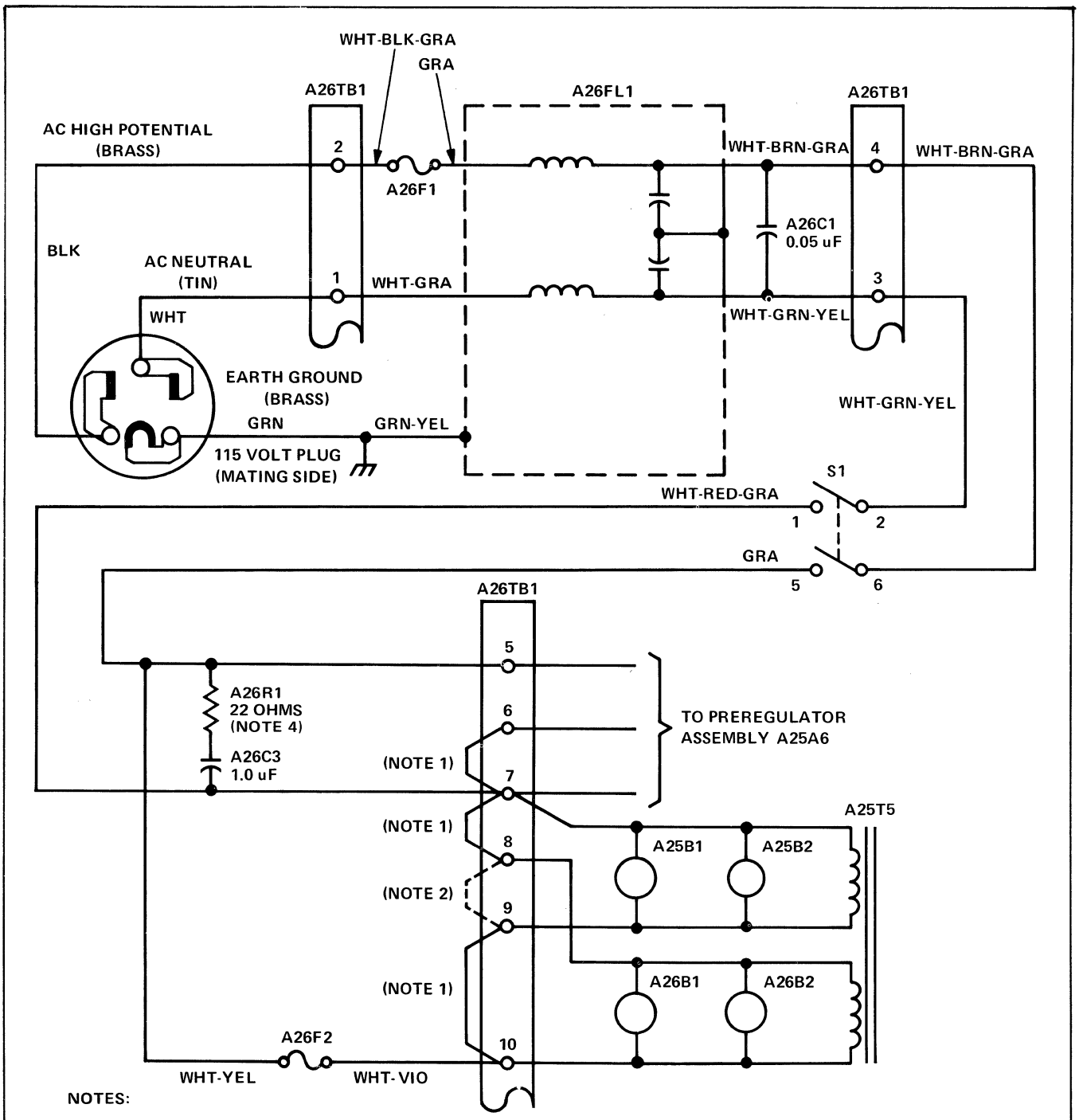
Primary power voltage is present at the exposed terminals of terminal board A26TB1 with the plenum chamber bottom cover removed and the power cable connected to the primary power source. Use extreme caution when making measurements in this area.

m. Ensure that the POWER switch is set to OFF, then connect the power cable to the primary power source.

n. Turn POWER switch to ON. With an ac voltmeter set to measure the primary power voltage (115 volts ac or 230 volts ac), measure the ac voltage between terminal 7 of terminal board A26TB1 and the computer frame. The voltmeter reading should be approximately zero volts ac. If the voltmeter indicates primary power voltage, either the ac neutral potential available at the primary power receptacle is not grounded, or the power supply is incorrectly wired. However, proceed to step "o" to determine if the power supply is wired correctly.

o. Measure the ac voltage between terminal 5 of terminal board A26TB1 and the computer frame. The voltmeter reading should be 115 volts ac (or 230 volts ac). If the voltmeter indicates zero volts ac, the power supply is wired incorrectly. Contact the nearest Hewlett-Packard Sales and Service Office for wiring corrections. If the voltmeter indicates 115 volts ac (or 230 volts ac) and the proper indication was not obtained in step "n", the power supply is wired correctly, but the ac neutral is not maintained at ground potential (refer to paragraph 2-34). Contact a qualified electrician to correct primary power source wiring.

p. Turn POWER switch to OFF and unplug computer power cable from primary power source. Before replacing the card cage cards, plenum chamber bottom cover, and the computer bottom panel perform the power supply checkout in paragraph 2-39.



1. JUMPER POSITIONS FOR 115-VOLT OPERATION; JUMPERS ARE REMOVED FOR 230-VOLT OPERATION.
2. JUMPER POSITION FOR 230-VOLT OPERATION; JUMPER IS REMOVED FOR 115-VOLT OPERATION.
3. SWITCH S1 IS A CAM-OPERATED SWITCH. CONTACTS ARE CLOSED IN THE POWER ON AND LOCK ON POSITIONS.
4. ON COMPUTERS WITH SERIAL NUMBERS PREFIXED BELOW 1145, THE VALUE IS 21.5 OHMS.

2133-90A

Figure 2-6. AC Power Connection Check Diagram

2-39. POWER SUPPLY CHECKOUT.

2-40. The computer power supply should be checked to verify that the dc supplies are functioning properly before operating the computer. In the procedure that follows, the card cage cards are removed to prevent damage to these cards should the power supply malfunction due to undiscovered damage during shipment. The power supply is checked again under normal load conditions after mounting (refer to paragraph 2-44). To check the power supply, proceed as follows:

a. Ensure that the POWER switch is set to OFF and the computer power cable is disconnected from the primary power source.

b. Remove the computer top panel and the card cage card retainer (see figure 1-3). Remove all cards from the computer card cage except the inhibit driver load card A106.

c. Connect the computer power cable to primary power source and turn POWER switch to ON.

d. With a voltmeter, measure the power supply operating voltages at the test jacks on the rear panel. Refer to the power supply manual for voltage tolerances and for adjusting the power supply operating voltages. If the operating voltages are within the specified limits, proceed to step "e".

e. Turn POWER switch to OFF and disconnect the computer power cable from the primary power source. Replace the card cage cards, card retainer, and all covers and panels.

2-41. MOUNTING.

2-42. The computer is designed either for bench installation or for mounting in a standard 19-inch equipment rack. When installed on a shelf, bench, or table, the computer need not be fastened down except for shipboard, aircraft, or other mobile use. For these mobile installations, shock mounts must be used. When installed in a rack, mount the computer in accordance with the instructions included in the rack-mounting kit. In mobile installations the entire rack, rather than the computer itself, must be shock mounted.

2-43. After the computer has been mounted, install and connect optional devices which are external to the computer. (Internal devices are factory-installed.)

2-44. Connect the computer and external devices to the ac power source. Then perform the voltage check procedures specified in the power supply manual. When this has been completed, make a performance check of the computer and all optional features as explained in the next paragraph.

2-45. PERFORMANCE CHECK.

2-46. The performance check of the computer consists of two parts. The first part is a pretest checkout of computer controls and program-loading ability. This is referred to as the basic checkout. The second part is a performance test, using diagnostic programs. Instructions for both the basic checkout and diagnostic test are given in section IV of this manual. Performance checks of I/O devices are described in the manuals for the devices.

2-47. CLAIMS.

2-48. If the computer is incomplete or damaged and fails to meet specifications when received, notify the nearest Hewlett-Packard Sales and Service Office. (Sales and Service Offices are listed in the back of this manual.) If damage occurred in transit, notify the carrier also. Hewlett-Packard will arrange for replacement or repair without waiting for settlement of claims against the carrier. In the event of damage in transit, retain the packing carton and packaging materials for inspection.

2-49. REPACKAGING FOR SHIPMENT.

2-50. SHIPMENT USING ORIGINAL PACKAGING.

2-51. The same containers and materials used in factory packaging can be used for reshipment of the computer. Alternatively, containers and packing materials may be obtained from Hewlett-Packard Sales and Service Offices. If the computer is being sent to the factory for servicing, attach a tag to the computer specifying the return address, the type of service required, the computer model number, and the full serial number of the computer. Mark the container "FRAGILE" to assure careful handling. In any correspondence, refer to the computer by model number and full serial number.

2-52. SHIPMENT USING NEW PACKAGING.

2-53. The following instructions should be followed when packaging the computer with commercially available materials:

a. Wrap the computer in heavy paper or sheet plastic. If shipping the computer back to the factory, first attach a tag to the computer with the return address and indicate the type of service required, the computer model number, and full serial number.

b. Use a strong shipping container. A double-wall carton of 350-pound test material is adequate.

c. Use enough shock absorbing material (3- to 4-inch layer) on all sides of the computer to provide a firm cushion and to prevent movement inside the container. Use particular care to protect corners and front of the computer.

d. Seal the shipping container securely, and mark it "FRAGILE."

e. In any correspondence with the factory, refer to the computer by model number and full serial number.

SECTION III THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section provides the theory of operation for the 2100A Computer. This discussion is conducted on a functional level using block diagrams to show relationships and the functional operation of the sections of the computer. An understanding of the information presented in this section is essential when performing troubleshooting or maintenance on the computer.

3-3. REFERENCE INFORMATION.

3-4. The following paragraphs provide general information which is required for understanding the operation of the computer.

3-5. BINARY SIGNAL LEVELS.

3-6. The binary signal levels used in the computer are approximately +2.5 volts dc, representing a true signal condition or a logic 1, and ground, representing a false signal condition or a logic 0. These signal levels may vary from these approximate amounts depending on the type of integrated circuit providing the signal, its condition, and its load. The minimum and maximum input and output voltages for each type of integrated circuit are specified in the Diagrams Manual.

3-7. LOGIC CIRCUITS.

3-8. The logic circuits employed in the computer use positive logic. That is, all inputs to an "and" or "nand" gate must be +2.5 volts for coincidence to occur. Similarily, if any input to an "or" or "nor" gate is +2.5 volts, the output is +2.5 volts for an "or" gate and ground for a "nor" gate. The output from the set-side of a flip-flop is +2.5 volts when the flip-flop is in the set state and ground when the flip-flop is in the clear state.

3-9. The logic symbols used in this manual are described in the Diagrams Manual.

3-10. SIGNAL NAMES.

3-11. Signals are named in one of the following ways:

a. As a condition which either exists or does not exist.

b. In accordance with the name of a flip-flop, amplifier, or switch which is the source of the signal.

c. In accordance with the name of a bus which carries the signal.

d. As a command or order expressed in the imperative grammatical mode.

3-12. Signal names throughout the computer are positive-true. The following paragraphs describe the expression "positive-true" as applied to the four types of signal names listed above.

3-13. When a signal is named in accordance with a condition, the signal level is positive when the condition exists and ground when the condition does not exist. For example, the signal MBSY (Memory Busy), when positive, means that the memory is busy. Conversely, when signal MBSY is a ground level, the memory is not busy.

3-14. When a signal is named in accordance with a flip-flop which is its source, the signal taken from the set-side output of the flip-flop is positive (true) when the flip-flop is set. For example, signal FBFF (Flag Buffer Flip-Flop) is true when the Flag Buffer Flip-Flop is set. If the signal is taken from the clear-side output of the flip-flop, the signal name is the complement of the flip-flop name and is true when the flip-flop is in the clear state. For example, signal $\overline{\text{AAFF}}$ ("not" A-Addressable FF) is taken from the clear-side output of the A-Addressable FF and is true when the flip-flop is in the clear state.

3-15. When a signal is named in accordance with a switch that is its source, the signal name depends, in part, on the voltage level output from the switch when the switch is activated. For example, the output signal from the RUN switch is named $\overline{\text{RUN}}$ ("not" Run) because when the RUN switch is pressed, its output goes to ground. A false (ground) $\overline{\text{RUN}}$ signal is a double negative meaning that the command "run" is true.

3-16. When a signal is named in accordance with a bus which carries it, the signal is positive when the bus carries a logic 1 and ground when the bus carries a logic 0. For example, signal SB2 (S-Bus, bit 2) is positive when bit 2 of the S-Bus is a logic 1.

3-17. When a signal is named in the imperative mode, it becomes positive to bring about the action commanded. For example, signal STF (Set Flag) becomes positive to set a flag flip-flop.

3-18. Definitions of abbreviated signal names (mnemonics) used in the computer are given in the signal lists located in the Diagrams Manual.

3-19. COMPUTER FUNCTIONAL SECTIONS.

3-20. From a functional standpoint, the computer consists of five sections. These sections, as shown in figure 3-1, are listed and defined as follows:

a. Memory. The Memory Section provides storage for the machine language computer program and all related information. The memory is addressed, read from, and written into on command from the computer control section.

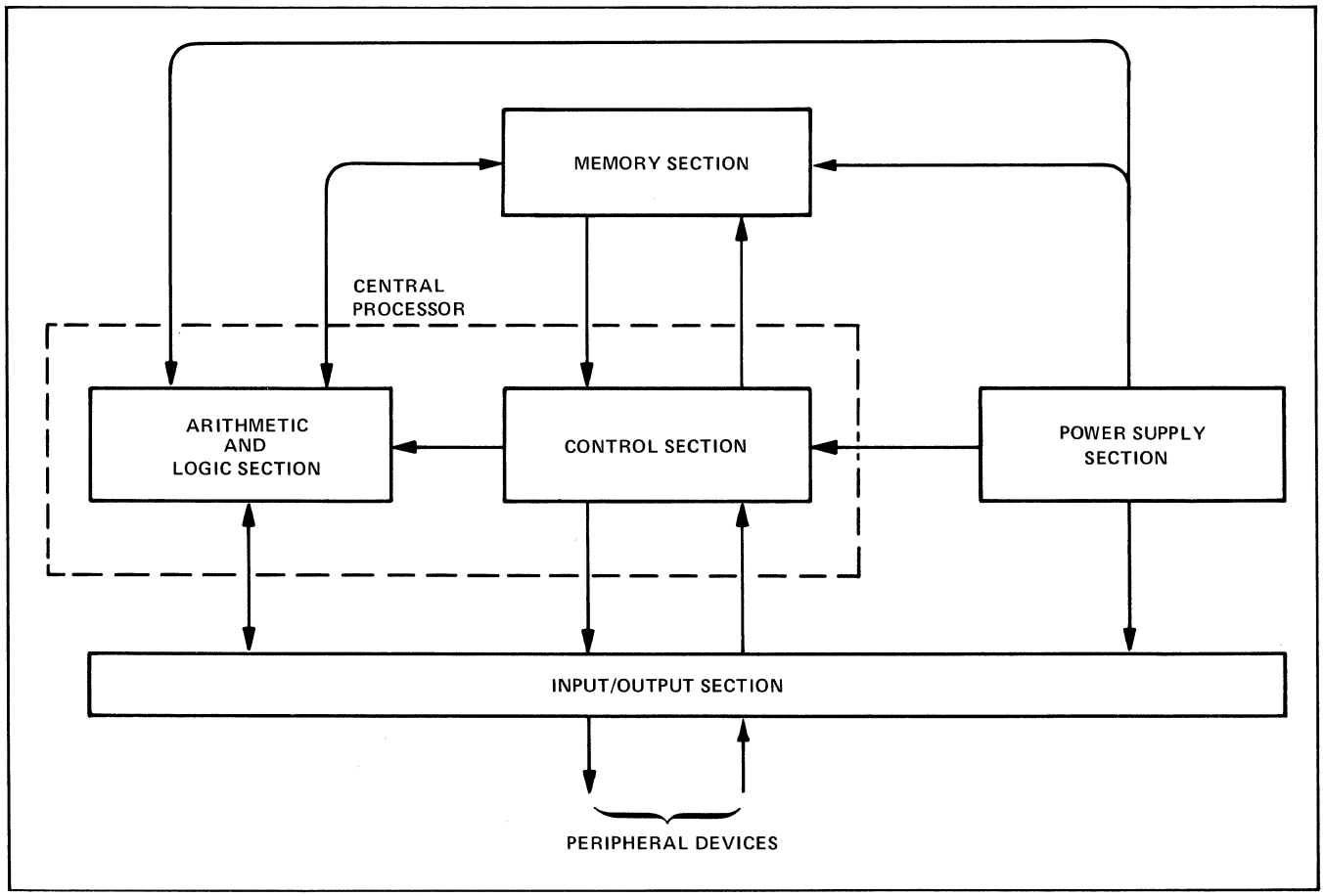
b. Arithmetic and Logic. The Arithmetic and Logic Section provides the adders, shifters, registers, and other related logic circuitry to perform the data manipulations required by any of the machine language program instructions.

c. Input/Output. The Input/Output (I/O) Section provides the control circuitry and registers necessary for orderly communication between the computer and various peripheral devices such as teletype, disc memory, tape punch, tape reader, etc. The operator panel functions in many respects as an I/O device and is considered part of the I/O Section.

d. Control. The Control Section directs the overall operation of the Memory, Arithmetic and Logic, and Input/Output Sections of the computer. It fetches and decodes the machine language instructions from memory, enables the correct sequence of arithmetic functions and/or logic gates, directs the storage of modified information in memory if required, and controls the transfer information between the computer Memory Section, Input/Output Section, and the related peripherals.

e. Power Supply. The Power Supply Section converts the input power, 115 or 230 volts ac, to the regulated dc supplies required for operation of all circuits within the computer.

3-21. As shown by figure 3-1, the combination of the Control Section and the Arithmetic and Logic Section is referred to as the Central Processor.



2133-20

Figure 3-1. Major Computer Functional Sections, Block Diagram

3-22. OVERALL BLOCK DIAGRAM DISCUSSION.

3-23. Figure 3-2 illustrates the internal makeup and relationships of the major sections of the computer. (The power supply section is discussed separately in the power supply Operating and Service Manual and is not shown in figure 3-2.) In addition, figure 3-2 provides the physical location (printed-circuit card number) of each functional block. The following paragraphs provide a functional description of each block shown by figure 3-2.

3-24. BUS SYSTEM.

3-25. Four 16-bit data buses are employed for data transfer within the computer. They are designated R-Bus, S-Bus, T-Bus, and I/O-Bus. The R-Bus and T-Bus apply only to the arithmetic and logic section and are discussed in detail along with the arithmetic and logic section discussion. The S-Bus is associated with all sections of the computer and is used for transfer of all data between sections. The I/O-Bus provides a 16-bit path for data transfer between the input/output section and all peripheral interface circuits.

3-26. MEMORY SECTION.

3-27. The computer memory section provides storage for programs to be executed by the computer. As described in Section I of this manual, the memory is available in varying storage capacities to a maximum of 32K (32,768) 17-bit words. Figure 3-2 shows the functional blocks of the memory section as configured for a 32K storage capacity. The following paragraphs list and describe each block.

3-28. CORE STACK. The heart of the computer memory is the Core Stack. The computer employs a conventional coincident-current, parallel-readout, ferrite core memory. Use of a single wire for sensing and inhibiting operations permits the use of three wires through each core rather than the more common four wires.

3-29. Figure 3-2 shows that the individual Core Stacks contain a maximum of 8K word locations and four of these stacks are installed to make a 32K memory.

3-30. MEMORY TIMING AND CONTROL. The Memory Timing And Control Circuits receive read-write and clear-write commands from the computer control section and supply all the necessary control signals for a memory cycle. The timing of the memory circuits is described in detail in paragraph 3-90 of this section.

3-31. MEMORY SECTION REGISTERS. Two registers located in the memory section are the M-Register (15-bits) and the T-Register (16-bits). The M-Register, referred to as the Memory Address Register, always contains the address of a computer word being read from or written into memory. The M-Register can be incremented or decremented by operator panel control. The T-Register, referred to as the Memory Data Register, contains the actual word being read from or written into the memory address specified by the M-Register. The M-Register is loaded with the required memory address via the S-bus prior to a memory read-write or clear-write operation. The T-Register is loaded with the contents of the memory address during a read-write operation, and is loaded via the S-bus with the information to be stored during a clear-write operation.

3-32. MEMORY ADDRESS DECODER. The Memory Address Decoder circuits convert the 15-bit contents of the M-Register to the format required to drive the addressing wires in the core stack.

3-33. X-Y DRIVER/SWITCHES. The X-Y Driver/Switches are selected by the output of the Memory Address Decoder and supply the current required to address the actual core locations in the memory Core Stack. The addressing wires are referred to as X and Y wires within the Core Stack. The X and Y currents from the X-Y Driver/Switches coincide at the 17 addressed cores. During a read operation, the current directions drive the addressed cores to what is chosen to be the logic 0 state. During a write operation, both X and Y currents are reversed and drive the addressed cores to the logic 1 state.

3-34. SENSE AMPLIFIERS. The above paragraph stated that during a read operation, the 17 addressed cores are driven to the logic 0 state. If any of these cores are storing a logic 1, the act of switching causes a voltage pulse to be induced in the sense/inhibit wire. This pulse is detected by a Sense Amplifier (SA) which generates a signal that sets the corresponding bit-position FF in the T-Register. If the core is storing a logic 0, no core-state switching is involved and no voltage pulse is generated. The T-Register FF for that bit then remains clear.

3-35. INHIBIT DRIVERS. During a write operation, the X-Y Driver/Switch currents drive the addressed cores to the logic 1 state. Any T-Register bit that is a logic 0 causes an Inhibit Driver (ID) to generate an inhibit current in the corresponding sense/inhibit wire. This current opposes the effect of the X-Y currents and prevents the core from switching to the logic 1 state. If a T-Register bit is a logic 1, no inhibit current is generated and the core is allowed to change from the logic 0 to the logic 1 state.

3-36. PARITY LOGIC. To provide a continuous check on the operation of the memory circuits, a parity bit (bit-16) is written into and read from the memory during all read-write memory operations. The parity circuits operate in the odd parity mode. That is, a true parity bit is generated and stored with each word when required to make the number of true bits in each word odd. All words are checked during a read operation and if the number of true bits per word is not odd, a bit has been added or dropped and a parity error indication is generated.

3-37. ARITHMETIC AND LOGIC SECTION.

3-38. The arithmetic and logic section of the computer consists of the blocks shown by figure 3-2. The arithmetic and logic circuitry is interconnected by the R-, S-, and T-Buses. All data manipulation required for the execution of any machine language instruction is performed in this section.

3-39. REGISTERS. The arithmetic and logic section registers consist of two one-bit registers and two groups of 16-bit registers referred to as R-Bus registers and S-Bus registers. The following paragraphs list and describe the arithmetic and logic section registers.

3-40. R-Bus Registers. The R-Bus Registers are:

a. A-Register. The A-Register is a 16-bit accumulator register that receives its input from the T-Bus and outputs to the R-Bus. It can be right-shifted when required to perform certain arithmetic functions. The A-Register is directly addressed by any memory reference instruction with operand address 000000 and can be displayed on the computer operator panel by pressing the A switch.

b. B-Register. The B-Register is a 16-bit accumulator register that receives its input from the T-Bus and outputs to the R-Bus. The B-Register is directly addressed by any memory reference instruction with operand address 000001 and can be displayed on the computer operator panel by pressing the B switch.

c. Q-Register. The Q-Register is a 16-bit register that receives its input from the T-Bus and outputs to the R-Bus. The Q-Register can be left-shifted when required to perform certain arithmetic functions. This register is not accessible by the user.

d. F-Register. The F- (Fence) Register is a 16-bit register that stores the upper limit of a block of memory (from memory address 000002 to the memory address contained in the F-Register minus one) to be protected by the memory protect function of the computer. For use with memory protect, the F-Register is loaded by an OTA 05 or OTB 05 instruction in the computer program. The F-Register is also used when performing certain arithmetic functions in the same manner as the Q-Register. This register is not accessible by the user.

3-41. S-Bus Registers. The S-Bus Registers are:

a. P-Register. The P-Register is a 16-bit program counter used to point to the next instruction in the computer program to be executed. The P-Register is incremented by one during the execution of each program instruction except skip instructions, when the skip condition is met, and JMP or JSB instructions. A skip causes the P-Register to be incremented twice and a JMP or JSB instruction replaces the P-Register content with the operand address of the instruction. The P-Register receives its input from the T-Bus and outputs to the S-Bus. The content of the P-Register can be displayed on the computer operator panel by pressing the operator panel P switch.

b. SP-Registers. Four SP- (Scratch Pad) Registers, designated SP1, SP2, SP3, and SP4, are 16-bit registers used for temporary storage of information during various program operations. All four SP-Registers receive inputs from the T bus and output to the S-bus. These registers are not accessible by the user.

3-42. Extend Register. The Extend Register is a one-bit register used to link the A- and B-Registers for rotate operations and to save a carry from the A- or B-Registers during an add or increment operation. The Extend Register may be cleared, complemented, and tested by program instructions and complemented by operator panel control. The state of the Extend Register is continuously displayed on the computer operator panel.

3-43. Overflow Register. The Overflow Register is a one-bit register that indicates, when set, that an add or increment operation has caused one of the accumulators (A- or B-Registers) to exceed its maximum positive or negative number capacity. The Overflow Register may be cleared, set, or tested by program instruction and complemented by operator panel control. The state of the Overflow register is continuously displayed on the computer operator panel.

3-44. FUNCTION GENERATOR. The Function Generator block combines the R-Bus and S-Bus data in a manner described by the selected logic or arithmetic function. Functions that are available in the Function Generator integrated circuit packs are divided into two groups; arithmetic functions and logic functions. A signal from the computer control section to the Function Generator selects the function group and a four-bit function number selects the function within the group. The selected function is determined by the data manipulation required to execute the program instruction. Refer to the Diagrams Manual for detailed information of the Function Generator integrated circuit packs.

3-45. SHIFTER. The 16-bit output of the Function Generator (functionally combined R- and S-Buses) is applied to the Shifter circuits. All shifts and rotates are executed here as directed by the computer control section. The Shifter output is then placed on the T-Bus and stored in one of the arithmetic and logic section registers by a store command from the computer control section.

3-46. A- AND B-ADDRESSABLE LOGIC FFs. When a memory reference instruction addresses the A- or B-Registers, the respective A- or B-Addressable FF will set. When an attempt is made to read or write in locations zero or one, these FFs ensure that the operation is made with the A- or B-Register and not locations zero or one in the computer memory.

3-47. INPUT/OUTPUT SECTION.

3-48. The Input/Output (I/O) Section provides the hardware link for communication with all peripheral devices. The I/O Section consists of three registers, I/O Control and Instruction Decoder circuits, and all Interface Cards used in the computer system. For the purpose of this discussion, the Operator Panel circuits are also considered part of the I/O Section.

3-49. I/O SECTION REGISTERS. The following paragraphs list and describe the registers used in the computer I/O Section.

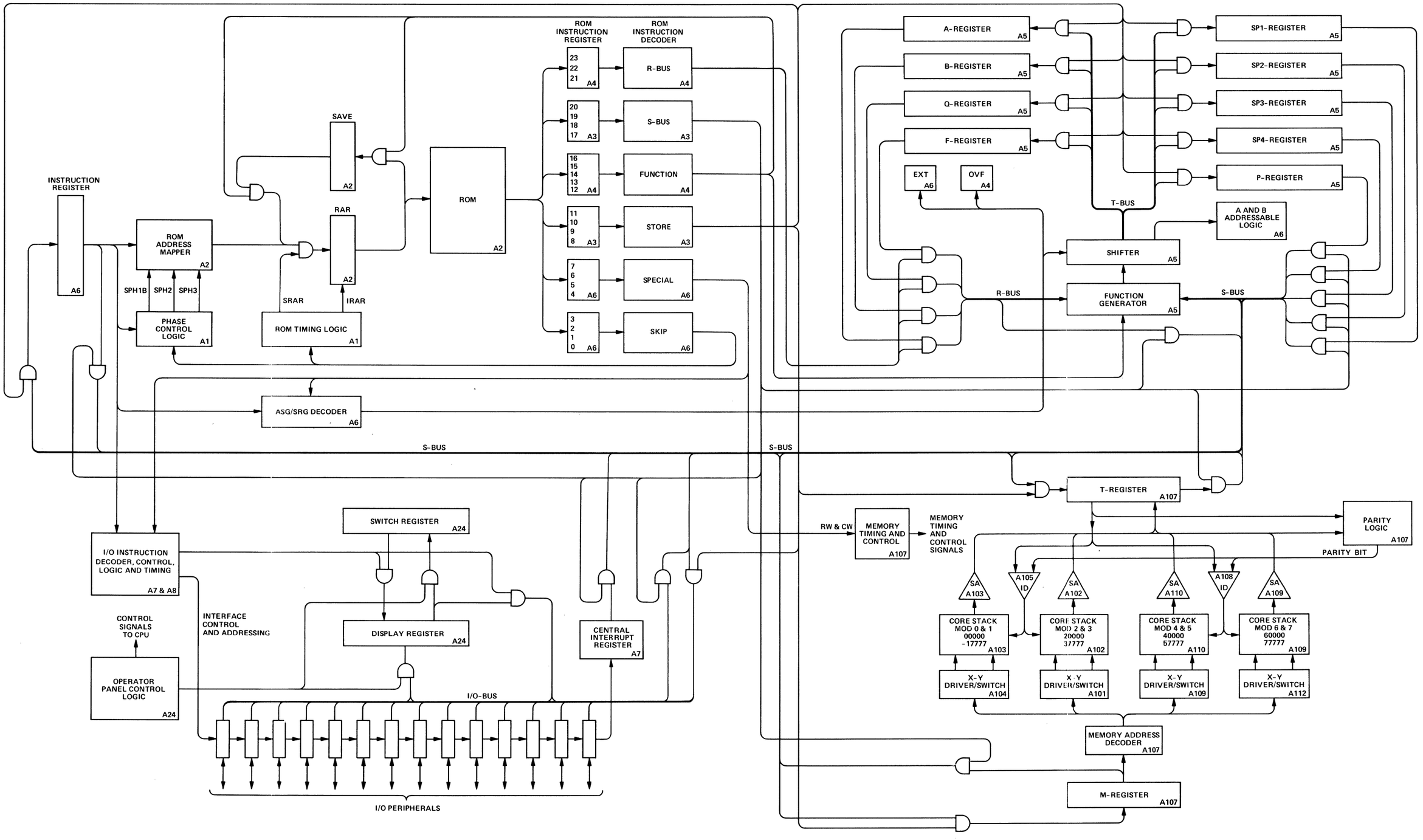


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Figure 3-2. 2100A Computer, Overall Block Diagram

3-50. Central Interrupt Register. The Central Interrupt Register is a 6-bit register that stores the I/O address (select code) of any peripheral that is requesting an interrupt. When the computer accepts an interrupt request and sets phase 1B (the interrupt "fetch" phase), the content of the Central Interrupt Register is transferred via the S-Bus to the memory section M-Register. The control section of the computer then fetches and executes the contents of the interrupt address in memory. The interrupt address normally contains a JSB instruction directing the computer to an interrupt subroutine to service the interrupting device.

3-51. S-Register. The S- (Switch) Register, located on the computer Operator Panel, is a 16-bit register that functions as an I/O device addressed by select code 01. The S-Register operates in conjunction with the Display Register as described in the following paragraph.

3-52. Display Register. The 16-bit Display Register is also located on the computer Operator Panel. The content of the Display Register is always shown by a series of 16 indicators on the computer Operator Panel. The Display Register can be loaded with the contents of the A-, B-, M-, S-, P-, or T- (memory data) Registers by pressing the appropriate Operator Panel switches. The contents of the Display Register may be modified by pressing the DISPLAY REGISTER switches. The Display Register outputs to the I/O-bus and Display Register data can be transferred from the I/O-bus via the S-bus to the A-, B-, M-, P-, or T-Registers. Data transfer between the S-Register and the Display Register is direct and does not require the use of any of the data buses.

3-53. I/O INSTRUCTION DECODER, CONTROL LOGIC, AND TIMING. The I/O Instruction Decoder, Control Logic, and Timing circuits receive the Instruction Register bits from the control section. All I/O instructions are decoded in the I/O Control and Instruction Decoder except LIA/B, MIA/B, and part of OTA/B. These circuits also decode the address of the peripheral specified by the I/O instruction and provide signals that enable the interface circuits used with the addressed peripheral.

3-54. Timing for the I/O section is generated by the I/O Instruction Decoder, Control Logic, and Timing circuits in the form of five 196-nanosecond time periods. For detailed I/O section timing information, refer to paragraph 3-88 in this section.

3-55. INTERFACE CARDS. The computer I/O section provides 14 card slots in the computer mainframe for interface cards. Each peripheral device in the computer system must be connected to the computer through an interface card. The interface cards provide control signals to the peripheral, status information to the computer, and adjust the data voltage levels to that required by the computer and the peripheral.

3-56. A priority chain connects all interface cards serially to prevent interrupt requests from two or more peripherals simultaneously. The interface card priority is determined by the interface card slot that the card occupies with slot 23 having the highest priority and slot 10 the lowest. Interrupts from a higher priority device inhibit lower priority interrupts by breaking the priority chain.

3-57. Refer to the Operating and Service Manual for the respective interface kit for detailed information on the interface cards.

3-58. CONTROL SECTION.

3-59. The primary function of the computer control section is to translate instructions into combinations of control signals that will result in the execution of these instructions. The term "instructions" is used broadly to mean status information from various sections of the computer and instructions from the computer program and/or operator panel. In the control section, all required combinations of control signals have been encoded and stored in a read-only memory (ROM). The instructions need only be interpreted by the control section as a starting address in the ROM. The encoded control signals are then read from the ROM, decoded, and applied to the respective computer circuitry.

3-60. The stored content of the ROM is referred to as a microprogram. The microprogram consists of a number of microinstructions; each microinstruction is further divided into six fields. The fields contain the encoded control signals referred to in the above paragraph.

3-61. The following paragraphs describe each control section block as shown by figure 3-2.

3-62. INSTRUCTION REGISTER. The Instruction Register is a 16-bit register which stores program instructions as read from the computer memory. The Instruction Register is loaded from the S-bus and can be read back, in part, onto the S-bus. The content of the Instruction Register is sensed by the Phase Control Logic (paragraph 3-63), ROM Address Mapper (paragraph 3-64), ASG/SRG Decoder (paragraph 3-70), and I/O Instruction Decoder (paragraph 3-53).

3-63. PHASE CONTROL LOGIC. The Phase Control Logic monitors the Instruction Register to determine the phase of operation required for any given computer cycle. Phases include two fetch phases (normal and interrupt), an indirect phase, an execute phase, and a special phase for operations involving the direct memory access capability (paragraph 3-172) of the computer. These phases are described in detail in paragraphs 3-106 through 3-113.

3-64. ROM ADDRESS MAPPER. The ROM Address Mapper decodes the Instruction Register bits and Phase Control Logic outputs to provide the appropriate starting address in the ROM microprogram. This address is loaded into the ROM Address Register (RAR).

3-65. ROM ADDRESS REGISTER. The ROM Address Register (RAR) is a 10-bit register with parallel input and indexing capabilities. The ROM Address Register always contains the address of the next ROM microinstruction to be decoded and executed.

3-66. SAVE REGISTER. The Save Register is a 10-bit register which follows the output of the ROM Address Register until a ROM Jump-to-Subroutine (JSB) microinstruction is encountered. At this point, the Save Register content is held to provide the return address in ROM after the ROM subroutine has been executed.

3-67. ROM. The ROM is an integrated-circuit, read-only memory. A microprogram is stored in the ROM as a series of 24-bit microinstructions which, when addressed, are transferred in parallel to the ROM Instruction Register.

3-68. ROM INSTRUCTION REGISTER. The ROM Instruction Register provides 24-bit buffer storage for the ROM microinstructions and transfers these microinstructions in parallel to the ROM Decoder circuits. This allows the current microinstruction to be executed while the next microinstruction is being fetched from ROM, thereby reducing the microinstruction execution time.

3-69. ROM INSTRUCTION DECODER. Figure 3-2 shows the ROM Decoder divided into six sections. Each section decodes one of the six fields that make up a single microinstruction. The six fields are listed and described as follows:

a. R-Bus Field. The R-Bus field consists of bits 21 through 23 of a ROM microinstruction. The decoded R-Bus field controls the source of information to be read onto the R-Bus.

b. S-Bus Field. The S-Bus field consists of bits 17 through 20 of a ROM microinstruction. The decoded S-bus field controls the source of information to be read onto the S-Bus.

c. Function Field. The Function Field consists of bits 12 through 16 of a ROM microinstruction. The decoded Function Field specifies arithmetic, logic, shift, or special control functions to be applied when combining and reading the R- and S-Buses onto the T-Bus. Conditional or unconditional jumps with the ROM microprogram can also be directed by the Function Field. In this case, bits 0 through 7, 12, and 17 of the ROM instruction register specify the address of the jump.

d. Store Field. The Store Field consists of the microinstruction made up of bits 8 through 11 of a ROM microinstruction. The decoded store field specifies the register in which the T-Bus or S-Bus information is to be stored after executing the R-Bus, S-Bus, and Function Fields. (Storing from the S-Bus does not involve the function field.)

e. Special Field. The Special Field consists of bits 4 through 7 of a ROM microinstruction. The Special Field enables alter-skip, shift-rotate, and input/output group operations and initiates memory read-write and clear-write operations.

f. Skip Field. The Skip Field consists of bits 0 through 3 of a ROM microinstruction. The decoded Skip Field initiates conditional and unconditional skips within the ROM microprogram.

3-70. SRG/ASG DECODER. To execute program instructions in the shift-rotate or alter-skip groups, the SRG/ASG Decoder provides control signals in addition to those provided by the ROM Decoder circuits.

3-71. COMPUTER FUNCTIONAL OPERATION.

3-72. The following paragraphs describe the functional operation of the computer by first discussing the general concept of microprogram control as used in the 2100A Computer. Details on central processor, I/O section, and memory section timing are presented along with information on the timing synchronization requirements between these sections. The phase logic portion of the discussion describes the actual operation of the computer in response to user programmed instructions.

3-73. ROM MICROPROGRAM CONTROL.

3-74. In a computer operated by microprogram control, each user instruction word is interpreted as a series of step-by-step microinstructions directed to the computer hardware. In effect, the user is telling the computer what to do by providing a machine language instruction. The control logic then tells the computer hardware how to do it by providing the microinstructions. These microinstructions are permanently stored in the ROM and are accessed as required by the user instructions.

3-75. Figure 3-3 shows the organization of the portion of the ROM microprogram required to fetch and execute the user ADD instruction. Assuming that the user has stored an ADD instruction in memory, set the program counter (P-Register) to the address of the ADD instruction, and pressed the RUN switch, the computer will first execute the microinstructions at ROM addresses 000, 001, and 002 sequentially. The contents of these microinstructions are shown in table 3-1. Ignoring the CFLG in the function field for the time being, the microinstructions at ROM address 000 directs the computer hardware to perform the following:

a. (P) Put the P-register content on the S-bus.
b. (M) Store the S-bus data in the M-register.
c. (RW) Start a memory read-write cycle and check for possible addressing of the A- (000000) or B- (000001) registers.

3-76. The CFLG code in the function field resets a portion of the central processor that may have been used during the preceding operation. It has no effect on the above operation.

3-77. The microinstruction at ROM address 001 is then executed, resulting in the following:

a. (AAB) If the A- or B-register is addressed in the above operation, put that register content on the R-bus.

b. (COND) If the A- or B-register is addressed, put the R-bus data on the S-bus. If the A- or B-register is not addressed, put the T-register content (memory data) on the S-bus.

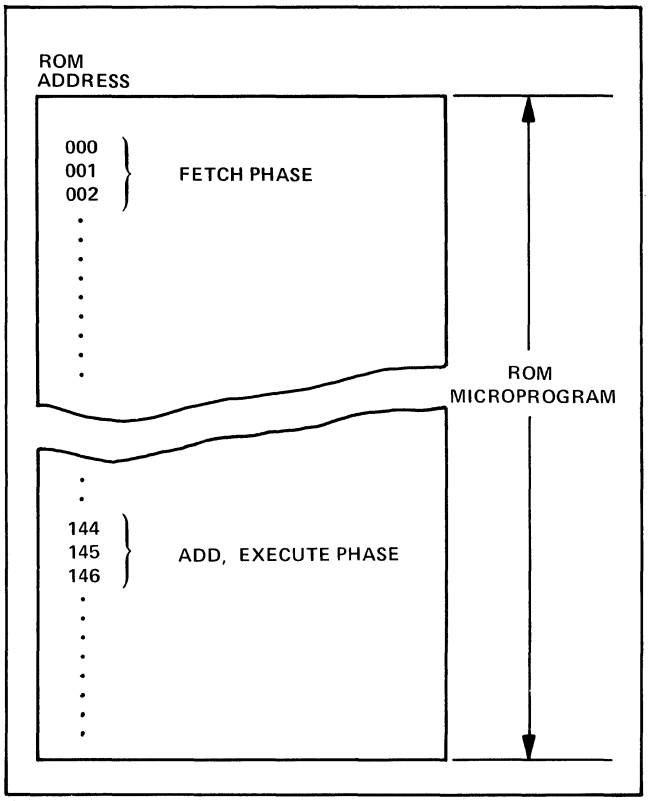


Figure 3-3. ROM Microprogram Organization

c. (IOR) The IOR microinstruction has no effect on this operation and is considered a NOP.

d. (IR) Store the S-bus data in the I- (Instruction) register.

e. (EOP) This microinstruction signals that the next microinstruction is the last operation of the present phase (fetch phase in this case). The ROM address mapper now examines the user instruction in the instruction register and locates the starting ROM address for the execute phase of that instruction.

3-78. The last microinstruction of the fetch phase operation (ROM address 002) has significance only if the user instruction is a memory reference group instruction. Execution of this microinstruction results in the following:

a. (ADR) Put the full operand address of the user instruction (part of the I-register and part of the P-register) on the S-bus.

b. (IOR) Logically inclusive-OR the R-bus data (0's due to the NOP) with the S-bus data (operand address) and place the result on the T-bus.

c. (S1) Store the T-bus data (operand address) in the SP1- (Scratch Pad 1) register.

d. (AAB) Check the T-bus data for a possible operand address of 000000 (A-register) or 000001 (B-register) and set the A- or B-addressable logic if A- or B-register is addressed.

Note: If the user instruction is not a memory reference instruction, the ROM skip logic is set and the microinstruction at ROM address 002 is executed as a NOP.

3-79. In summary, the fetch operation leaves the computer with the fetched ADD instruction in the I-register, the operand address of the instruction in the I-register, and the A- or B-addressable logic set if the operand address is 000000 or 000001 respectively. The computer is now directed to the execute phase of the ADD instruction beginning at ROM address 144.

3-80. The microinstructions required to execute the ADD instruction are shown in table 3-2. Execution of the microinstruction at ROM address 144 results in the following:

a. (S1) Put the SP1-register content (operand address) on the S-bus.

b. (IOR) Inclusive-OR S-bus (operand address) with R-bus (all 0's). Result goes to the A- and B-addressable logic.

c. (M) Store the S-bus content (operand address) in the M-register.

d. (RW) Start a memory read-write cycle and enable the A- and B-addressable logic.

3-81. The microinstruction at address 145 is then executed resulting in the following:

a. (AAB) If the A- or B-register is addressed in the above operation, put that register content on the R-bus.

b. (COND) If the A- or B-register is addressed, put the R-bus data on the S-bus. If the A- or B-register is not addressed, put the T-register content (memory data) on the S-bus.

Table 3-1. Fetch Phase Microinstructions

ROM ADDRESS	R-BUS FIELD	S-BUS FIELD	FUNCTION FIELD	STORE FIELD	SPECIAL FIELD	SKIP FIELD
000	NOP	P	CFLG	M	RW	NOP
001	AAB	COND	IOR	IR	NOP	EOP
002	NOP	ADR	IOR	S1	AAB	NOP

Table 3-2. ADD Instruction Execute Phase Microinstructions

ROM ADDRESS	R-BUS FIELD	S-BUS FIELD	FUNCTION FIELD	STORE FIELD	SPECIAL FIELD	SKIP FIELD
144	NOP	S1	IOR	M	RW	NOP
145	AAB	COND	IOR	S2	NOP	EOP
146	CAB	S2	ADDO	CAB	NOP	NOP

c. (IOR) The inclusive OR function has no effect on this operation and simply allows transfer of the S-bus data to the T-bus.

d. (S2) Store the T-bus content (A-register or B-register or memory data) in the SP2-register.

e. (EOP) Signal that the next microinstruction is the last operation of the present phase (execute phase). Control will be returned to the fetch phase microinstructions after execution of the microinstruction at ROM address 146.

3-82. The last microinstruction of the ADD instruction, execute phase is then executed resulting in the following:

a. (CAB) Put the A- or B-register content (selected by IR11) on the R-bus.

b. (S2) Put the SP2-register content on the S-bus.

c. (ADD0) Perform the add arithmetic function on the R- and S-bus data with the overflow logic enabled. The result goes to the T-bus.

d. (CAB) Store the T-bus data in the A- or B-register (selected by IR11).

3-83. It is important to realize that similarly named operations in different microinstruction fields have entirely different meanings. For example, the AAB operation in the R-bus field (paragraph 3-77, step "a") does not have the same meaning as the AAB operation in the special field (paragraph 3-78, step "d"). When using a ROM microprogram listing, attention must be given to the operation name and the location within the microinstruction in which it occurs.

3-84. A complete listing of the ROM microprogram is provided in Section IV of this manual.

3-85. COMPUTER TIMING.

3-86. All timing for the 2100A Computer is controlled by a 196-nanosecond clock located in the central processor. The timing cycles for the central processor, I/O section, and memory section are different and are described separately in the following paragraphs. These three sections operate independently except during operations that require control signal or data transfer between sections. The cycle times for the central processor, I/O section, and memory section are briefly described as follows:

a. I/O Cycle. An I/O cycle has a duration of 980 nanoseconds and is the time required for the execute phase of one programmed I/O instruction. The I/O cycle is divided into five 196-nanosecond time periods designated T2, T3, T4, T5, and T6.

b. Memory Cycle. A memory cycle has a duration of 980 nanoseconds and is the time required to read and restore (write) one word location in the computer memory. A memory cycle consists of a read or clear time and a write time.

c. Central Processor Cycle. A central processor cycle has a duration of 196 nanoseconds and is the time required for execution of one ROM microinstruction.

3-87. The following paragraphs provide detailed timing information for each of the three timing cycles.

3-88. I/O SECTION TIMING. Figure 3-4 provides timing information for the computer I/O section. A five-stage ring counter in the I/O section is clocked by the central processor clock $\overline{CLK3}$ (paragraph 3-95) and provides five 196-nanosecond time periods designated T2, T3, T4, T5, and T6.

Note: Time periods designated T0 and T1 are intentionally omitted to keep existing HP interface and peripheral hardware compatable with the 2100A Computer.

3-89. The computer I/O cycle always starts at time T2 and ends at time T6. Figure 3-4 shows the control signals provided to the interface circuits as a result of the various programmed I/O instructions. Refer to the applicable interface kit Operating and Service Manual for the effects of these signals. Detailed information on the I/O system operation including interrupt operation is provided in the 2100A Computer Reference Manual.

3-90. MEMORY SECTION TIMING. To simplify certain I/O operations, the Memory Section timing is synchronized with the I/O Section timing. A memory read-write or clear-write operation always begins during I/O time T2 and ends during I/O time T6. Figure 3-5 illustrates the timing signals that control the operation of the memory circuits.

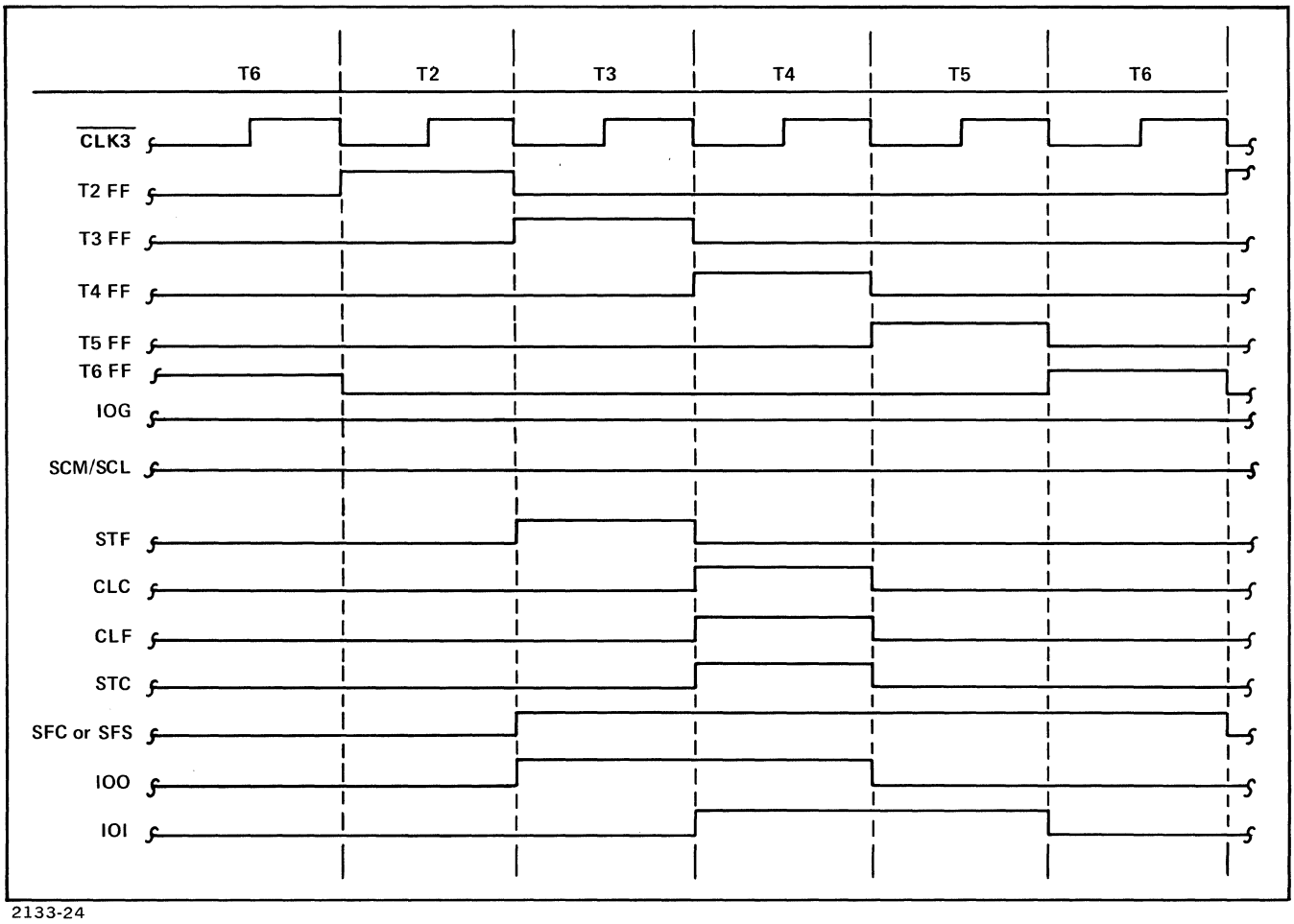


Figure 3-4. I/O Section, Timing Diagram

3-91. Memory Read Time. Memory read time (MRT) begins approximately 50 nanoseconds after the start of I/O time T2 and is considered complete by the start of I/O time T4. During the last half of T3, a signal from the MST (Memory Strobe Time) FF strobes the data from the memory sense amplifiers into the Memory Section T-register. The DTRY (Data Ready) signal shown by figure 3-5 goes false at the start of memory read time and is true again at time T4, signaling to the computer that data has been read from memory and is in the T-register ready to be transferred to the S-bus.

3-92. Memory Write Time. Memory write time begins midway through time T4 and is completed during time T6. The MWT signals enable the X-Y driver/switches for the write cycle and MIT enables the inhibit drivers.

3-93. As shown by figure 3-5, the MBSY signal is true for the duration of the memory cycle. The MBSY signal indicates to the computer that the M-register cannot be modified during this time.

3-94. CENTRAL PROCESSOR TIMING. Central processor timing is derived from a 10.204-MHz crystal-controlled oscillator which provides clock pulses 196 nanoseconds in duration. The central processor runs continuously, executing one ROM microinstruction every 196 nanoseconds except as described in paragraphs 3-98 through 3-105. Every time a ROM microinstruction is loaded into the ROM instruction register to be executed, the ROM address register is indexed to the next ROM address as determined by the ROM address mapper.

3-95. Figure 3-6 shows the five clock signals generated in the central processor in relation to the shaped output of the 10.204 MHz oscillator. Signals $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, and $\overline{\text{CLK3}}$ are designated "not" clocks implying that the clocking action takes place on the negative-going edge of the clock signal.

3-96. The primary function of the STCLK signal is to execute the store field of any ROM microinstruction. This clock occurs at the end of a central processor cycle to ensure that the data buses have time to settle after execution of the R-bus, S-bus, and function operations.

3-97. Signal $\overline{\text{CLK3}}$ runs continuously when computer power is on and is used by the Memory and I/O Sections as a time base for memory and I/O cycles. The remaining clock signals can be inhibited by an operation referred to as a central processor freeze as shown by figure 3-6. The central processor freeze operation is described in detail in the following paragraphs.

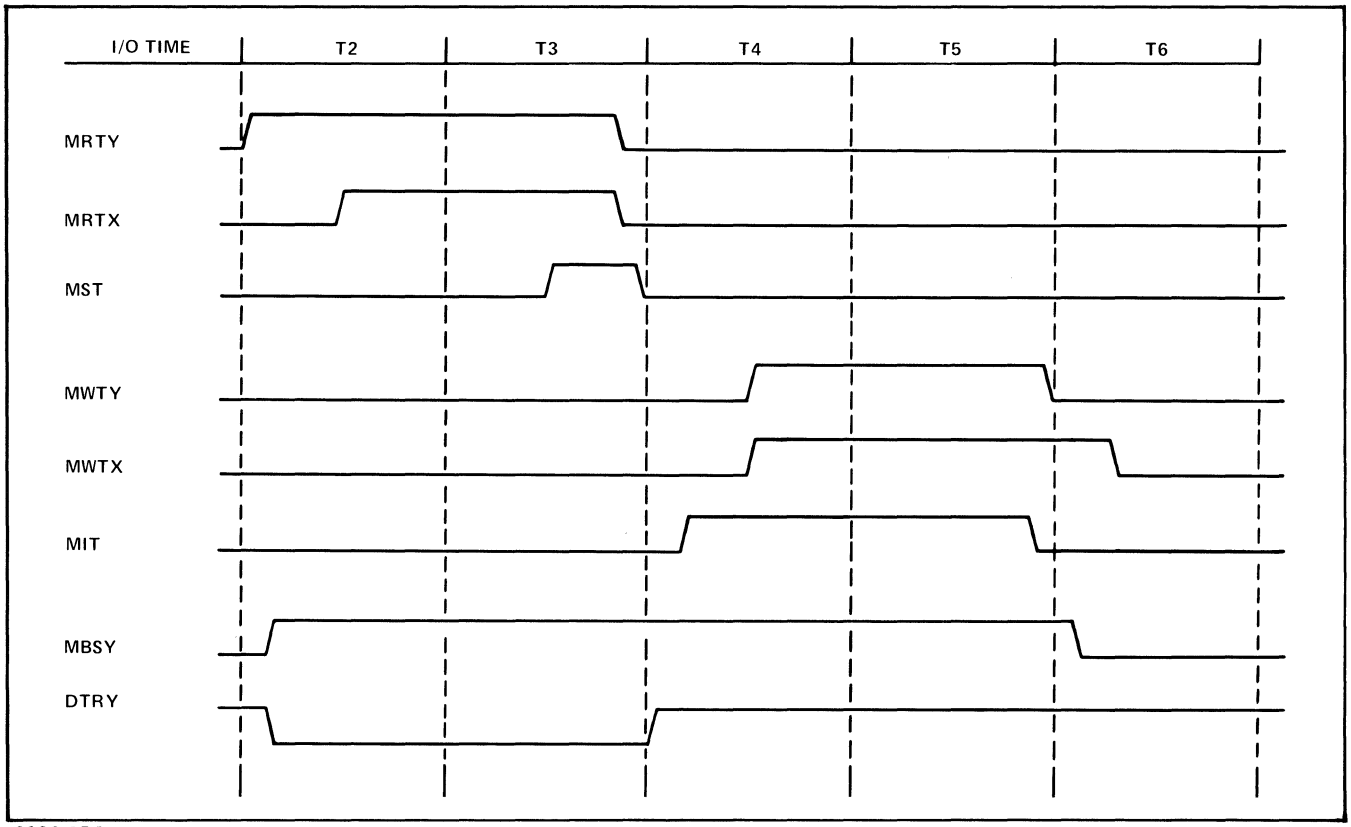


Figure 3-5. Memory Section, Timing Diagram

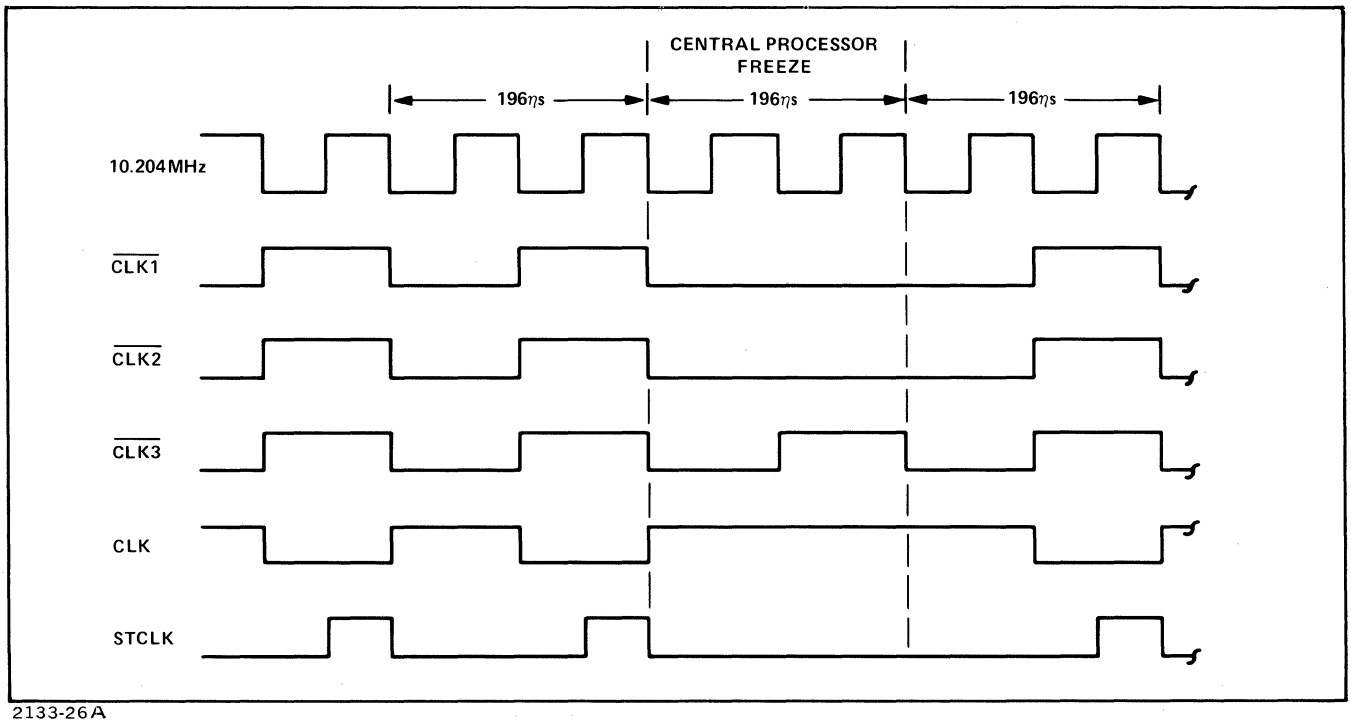


Figure 3-6. Central Processor, Timing Diagram

3-98. The preceeding discussion on memory and I/O timing has shown that memory and I/O operations are restricted to specific time periods relative to the I/O section ring counter. Therefore, the execution of any ROM microinstruction that requires transfer of data or control information between the central processor and memory or I/O sections must be done in synchronization with these sections.

3-99. Figure 3-7 is a flowchart showing the timing considerations that are made prior to executing each microinstruction. If, for example, the store field selects M and the MBSY signal is true, the central processor will freeze until MBSY is again false. MBSY goes false at the end of I/O time T5 during a memory cycle as shown by the memory timing diagram (figure 3-5).

3-100. The central processor freeze operation inhibits all clocks except $\overline{CLK3}$. This prevents the ROM address register and ROM instruction register from being changed and inhibits execution of the ROM microinstruction. This prevents altering the contents of any registers, flags, etc. within the central processor or memory section. When the freeze operation ends, the microinstruction causing the freeze is executed in the normal manner. The next microinstruction is then stored in the ROM instruction register and checked for a possible freeze requirement.

3-101. Re-examination of the fetch phase operation described in paragraphs 3-75 through 3-79 shows how the above described timing considerations apply to a typical ROM operation.

3-102. The microinstruction at ROM address 000 provides a read-write (RW) command to the memory section. This microinstruction can be executed only at time T6 relative to the I/O section ring counter.

3-103. The microinstruction at ROM address 001 calls for the T-register to be read to the S-bus (COND). This cannot occur until memory data is ready (DTRY). (This assumes that the instruction is in core, rather than in the A- or B-register.)

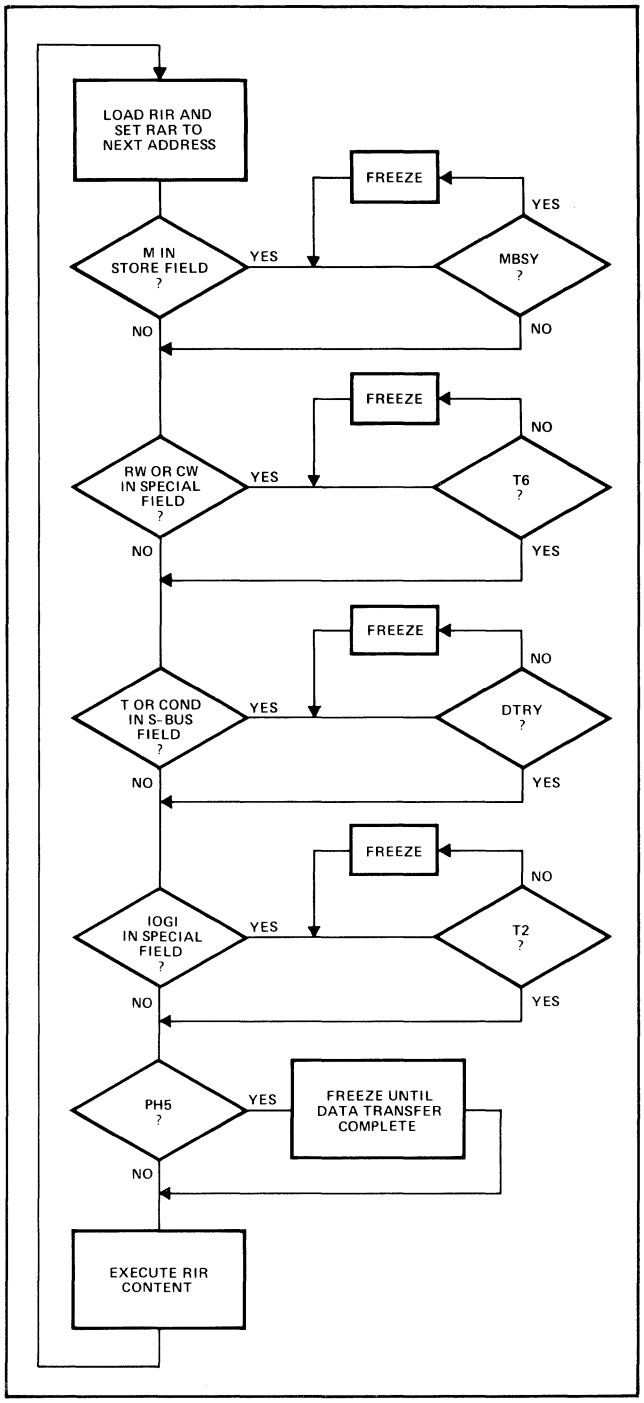
3-104. The microinstruction at ROM address 002 requires no data or control signal transfer between sections, allowing it to be executed immediately following the microinstruction at ROM address 001.

3-105. Figure 3-8 shows the timing of the central processor, I/O section, and memory section during execution of these three microinstructions.

3-106. PHASES OF OPERATION.

3-107. To process a machine language instruction stored in the computer memory, the instruction must first be fetched from memory and then executed. These operations are referred to as the fetch and execute phases. If a memory reference instruction specifies indirect addressing, a third phase (indirect phase) is required. An additional phase controls Direct Memory Access (DMA) operations if the DMA accessory is installed in the computer. The computer will be operating in one of these phases at all times. The following paragraphs describe the computer phases of operation.

3-108. FETCH PHASE. The fetch phase is the time during which a programmed instruction word is obtained from the computer core memory. The computer employs



2133-27

Figure 3-7. Central Processor, Timing Flowchart

two different fetch phases, both of which are controlled by routines within the ROM microprogram. The two fetch phases, designated phase 1A and phase 1B, are described as follows:

a. Phase 1A. Phase 1A (PH1A) is the normal computer fetch phase. During phase 1A, the memory address (P-register content) of the instruction word to be fetched is transferred to the M-register via the S-bus and the memory is signaled to perform a read-write operation. This places the fetched instruction word in the T-register. The T-register content is then transferred via the S-bus to the instruction register. The last step of a phase 1A operation is executed only if the fetched instruction is a memory reference instruction, in which case the operand address portion of the instruction is transferred via the S- and T-buses to the SP1-register to be referenced during the execute phase (or indirect phase, PH2, if bit 15 of the instruction is set) of the instruction. Refer to Section IV of this manual for the microinstructions executed during the phase 1A operation.

b. Phase 1B. Phase 1B (PH1B) is a special fetch phase used in the event of an I/O interrupt. When an interrupt occurs and is accepted, the computer enters phase 1B. The address of the interrupting I/O device is loaded into the I/O section central interrupt register at the beginning of phase 1B. During this phase, the content of the central interrupt register is transferred via the S-bus to the M-register and the memory is signaled to perform a read-write operation. (The instruction located at this memory address, referred to as a trap cell, is normally a JSB instruction directing the computer to a subroutine to service the interrupting I/O device.) The content of the trap cell is now stored in the memory section T-register. The P-register is then decremented to prevent losing the next instruction-in-sequence following the servicing of the interrupt. The T-register content is then transferred via the S-bus to the instruction register and, as in a phase 1A operation, the operand address of the instruction word is transferred to the SP1-register. Refer to Section IV of this manual for the microinstructions executed during a phase 1B operation.

3-109. INDIRECT PHASE. The computer indirect phase, designated phase 2 (PH2), is entered immediately after the fetch phase of a memory reference instruction which specifies indirect addressing. The operand address of the fetched instruction word, stored in the SP1-register as a result of the fetch phase, is transferred via the S-bus to the M-register and the memory is signaled to begin a read-write operation. Since indirect addressing specifies that the operand address of the original fetched instruction word is the address in memory of a new operand address, the resulting T-register content replaces the original content of the SP-1 register. Additional levels of indirect addressing are accomplished with successive phase 2 operations. Refer to Section IV of this manual for the microinstructions executed during the phase 2 operation.

3-110. EXECUTE PHASE. The execute phase (PH3) is the time during which the fetched instruction is actually executed. Each machine language instruction is assigned an entry point in the ROM microprogram and is executed by the portion of the microprogram defined by that entry point. The ROM address mapper determines the proper entry point by decoding the content of the instruction register. Refer to Section IV of this manual for details on the microinstructions executed during each execute phase.

3-111. PHASE 5. Computer phase 5 (PH5) is a special phase of operation used only during direct memory access (DMA) controlled I/O operations. During a phase 5 operation, the central processor is disabled while the DMA circuits generate the required control signals to transfer information directly between the computer memory and an I/O device. I/O operations under DMA control are discussed in detail in paragraphs 3-172 through 3-187.

3-112. SET PHASE LOGIC. At the end of each phase of operation, several possibilities must be considered before entering a new phase. This is done by the computer set phase logic during execution of the second-to-last microinstruction of each phase. This microinstruction always contains an EOP (End Of Phase) in the skip field which enables the set phase logic.

3-113. Depending on the present phase of operation, the set phase logic is described by one of the four flowcharts in figure 3-9.

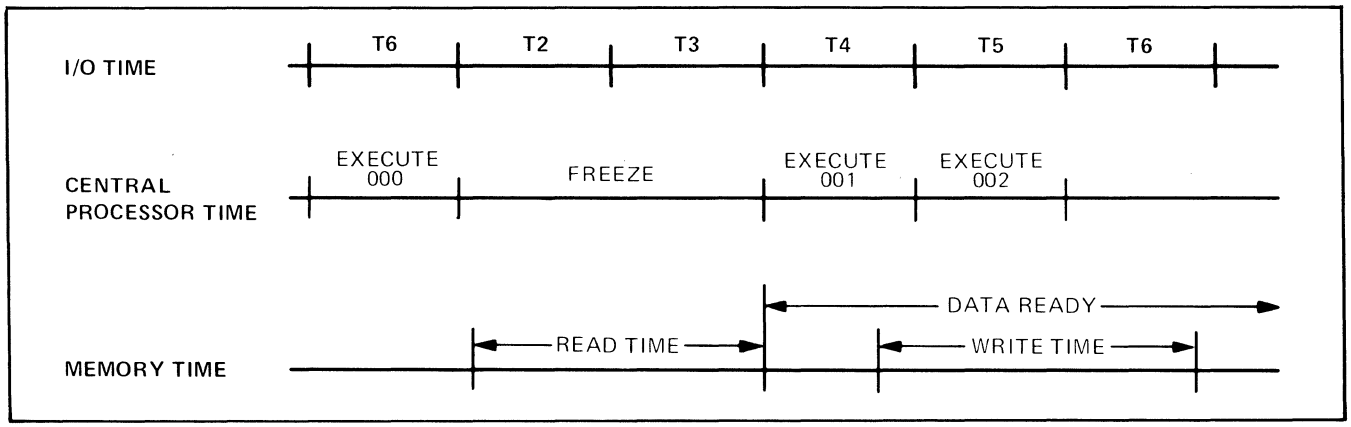


Figure 3-8. Computer Timing During Fetch Phase, Timing Diagram

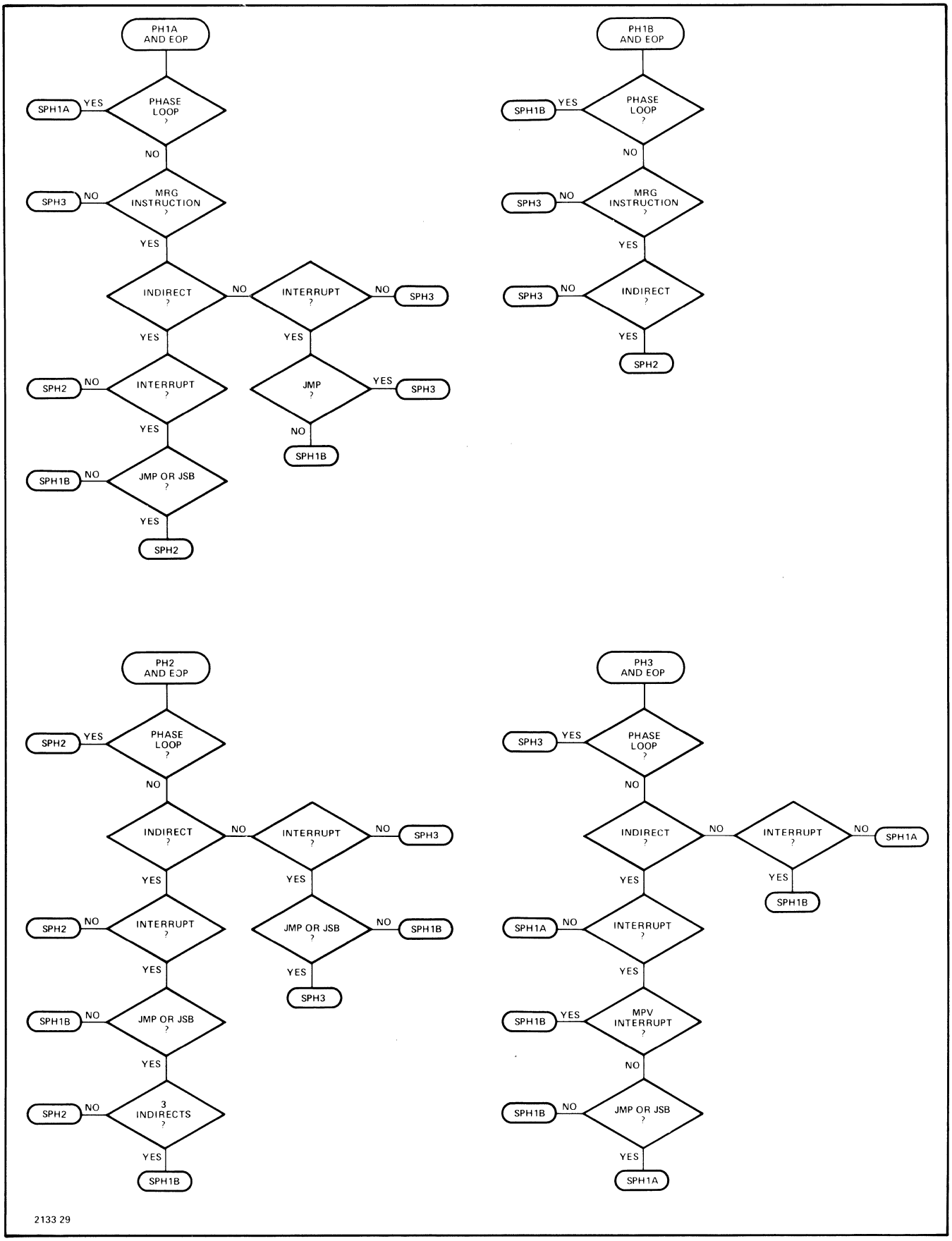


Figure 3-9. Set Phase Logic, Flowcharts

3-114. OPERATOR PANEL.

3-115. The computer operator panel provides means of controlling and observing the operational status of the computer. The operator panel is primarily a maintenance aid and an understanding of its operation greatly simplifies maintenance of the computer.

3-116. The following discussion describes each of the panel switches and indicators and the overall functional operation of the operator panel.

3-117. PANEL SWITCHES AND INDICATORS.

3-118. Switches and indicators on the computer operator panel consist of the computer power switch, 17 display register switches, 17 operation switches, two special maintenance switches, and four indicators. Each switch and indicator is described in the following paragraphs.

3-119. COMPUTER POWER SWITCH. The computer power switch is a three-position key-operated switch. The three positions are POWER OFF (ac power not applied to the computer power supply), POWER ON (ac power applied to the computer power supply and all operator panel switches enabled), and LOCK ON (ac power applied to the computer power supply and all operator panel switches disabled). The key may be removed from the switch when in the POWER OFF or LOCK ON position.

3-120. DISPLAY REGISTER SWITCHES. The display-register is a 16-bit register with a control panel switch for each bit plus a CLEAR DISPLAY switch. Pressing any of the 16 display-register switches toggles the corresponding bit-position of the display register regardless of the run/halt status of the computer. Each switch is also an indicator showing the state (set or clear) of the display-register bit-position. When the computer is in the run mode, the display-register is logically equivalent to the switch register and is treated as an I/O device having select code 01. When the computer is in the halt mode, the display-register is used to display the content of a selected register. This is further described in the following paragraphs.

3-121. The CLEAR DISPLAY switch can be activated at any time and, when pressed, clears all bit-positions of the display-register.

3-122. OPERATION SWITCHES. Each of the 17 operation switches, when pressed, initiate an operator panel timing cycle during which the operator panel supplies control signals to the computer to accomplish the operation described by the operation switch. All operation switches except the HALT/CYCLE switch are inhibited when the computer is in the run mode.

3-123. Six of the operation switches are referred to as display-select switches. These switches allow the contents of five of the computer registers (A, B, M, S, and P) and the memory contents (MEMORY DATA) addressed by the M-register to be displayed by the display register. A set of six flip-flops, one for each display-select switch, provides storage for the last display-select switch pressed. When any operation switch is pressed, other than the previously operated display-select switch, the content of the display register is transferred to the register pointed to by the display select circuits.

3-124. The operation switches are listed and described as follows:

a. A. The switch designated A is a display-select switch which causes the computer A-register content to be transferred to the operator panel display register.

b. B. The switch designated B is a display-select switch which causes the computer B-register content to be transferred to the operator panel display register.

c. M. The switch designated M is a display-select switch which causes the computer M-register content to be transferred to the operator panel display register.

d. S. The switch designated S is a display-select switch which causes the computer S-register content to be transferred to the operator panel display register. The S-display-select logic is automatically enabled when the computer is put in the run mode.

e. P. The switch designated P is a display-select switch which causes the computer P-register content to be transferred to the operator panel display register. Also, the P-operation switch, when pressed, presets the computer to the fetch phase.

f. MEMORY DATA. The switch designated MEMORY DATA is a display-select switch which causes the content of the memory location presently addressed by the M-register to be transferred to the operator panel display register. The MEMORY DATA display-select logic is automatically enabled when the computer changes from the run to the halt mode.

g. DECREMENT M. The switch designated DECREMENT M is an operation switch which causes the computer M-register to be decremented by one each time it is pressed.

h. INCREMENT M. The switch designated INCREMENT M is an operation switch which causes the computer M-register to be incremented by one each time it is pressed.

i. LOADER ENABLE. The switch designated LOADER ENABLE is an operation switch which controls access to the upper 64 memory locations (location of the basic binary loader). Pressing the LOADER ENABLE switch toggles the enable-disable function of the switch. The indicator portion of the switch is on when access to the loader is enabled.

j. INTERNAL PRESET. The switch designated INTERNAL PRESET is an operation switch which presets the computer to the fetch phase, disables memory protect,

clears any parity error indication, and disables the computer interrupt system.

k. EXTERNAL PRESET. The switch designated EXTERNAL PRESET is an operation switch which clears all control FFs and sets all flag FFs from I/O address 06 and up. The EXTERNAL PRESET indicator lights when the switch is operated and when the power fail circuit control bit is cleared.

l. OVF. The switch designated OVF is an operation switch which toggles the state of the computer Overflow FF. The indicator portion of the switch lights when the Overflow FF is in the set state.

m. EXTEND. The switch designated EXTEND is an operation switch which toggles the state of the computer Extend FF. The indicator portion of the switch lights when the Extend FF is in the set state.

n. INTERRUPT SYSTEM. The switch designated INTERRUPT SYSTEM is an operation switch which toggles the state (enabled or disabled) of the I/O interrupt system. The indicator portion of the switch lights when the interrupt system is enabled.

p. RUN. The switch designated RUN is an operation switch which places the computer in the run mode, disables all control panel switches except HALT/CYCLE, DISPLAY REGISTER, and CLEAR DISPLAY, and sets the switch register display select circuits. The indicator portion of the switch lights when the computer is active (run, single instruction, or single cycle).

q. HALT/CYCLE. The switch designated HALT/CYCLE is an operation switch which, when the computer is in the run mode, halts the computer at the end of the present phase of operation and sets the memory data display select circuits. When the computer is in the halt mode, the HALT/CYCLE switch causes the computer to execute one phase at the present program location. The indicator portion of the switch lights when the computer is in the halt mode (not active).

r. INSTR STEP. The switch designated INSTR STEP is an operation switch which causes the computer to execute all phases necessary to process the machine language instruction addressed by the P-register. The indicator portion of the switch lights when the switch is pressed.

3-125. SPECIAL MAINTENANCE SWITCHES. Two slide-switches are located on the operator panel printed-circuit board and are accessible by removing the computer front cover. These switches are designated Operation Loop and Memory Test.

3-126. The Operation Loop switch, when in the Loop (L) position, causes the control panel circuits to repeat the operation as long as the operation switch is held on. All panel operations except halt and run can be looped by using this switch.

3-127. The Memory Test switch, in the INH position, prevents the display-register from being clocked thereby locking the display-register so that it cannot be modified. By using the Memory Test switch along with the Operation Loop switch and INCREMENT M or DECREMENT M switches, all locations in memory can be loaded with a preselected word.

3-128. INDICATORS. Four positions on the operator panel serve as indicators only. They are designated FETCH, INDIRECT, EXECUTE, and PARITY. The FETCH, INDIRECT, and EXECUTE indicators light to show the phase of operation of the computer. The PARITY indicator lights when a parity error is detected during a memory read operation.

3-129. OPERATOR PANEL FUNCTIONAL OPERATION.

3-130. GENERAL. Figure 3-10 is a block diagram of the computer operator panel showing the major components of the panel. Note that the Control Circuits receive inputs from the operator panel circuits that are designated as Operation Switches. When any of these switches are pressed, or a program halt is detected, an operator panel cycle is initiated. The operator panel cycle is described in detail in paragraph 3-132.

3-131. The display register switches operate independently of the operation switches. The block labeled SWITCH CONTROL provides a time delay to prevent switch contact bounce from affecting the display register.

3-132. OPERATOR PANEL CYCLE. An operator panel cycle is initiated when any operation switch is pressed, provided the computer is in the halt mode. If the computer is in the run mode, an operator panel cycle is initiated by pressing the HALT/CYCLE operation switch or by executing a programmed halt instruction. An operator panel cycle consists of nine time periods generated by the operator panel Control Circuits. These time periods are listed in the order that they occur and are described as follows:

a. OPIH. Operation Inhibit (OPIH) is generated at the start of any operator panel cycle and lasts for the duration of the cycle. This prevents any other operation switch from affecting the control for the duration of the operator panel cycle. During operator panel cycles generated by the EXTEND, OVF, INTERRUPT SYSTEM, EXTERNAL PRESET, or INTERNAL PRESET operation switches, OPIH time gates the appropriate control signals to the computer.

b. DTSR. During the Display To Selected Register (DTSR) time, the display register content is transferred to the register previously selected for display. If memory data was previously selected, the display register content is transferred to the T-register and a CW (Clear Write) signal is sent to the memory, causing the memory to store the new memory data. If the operation switch causing the operator panel cycle is the same as the previously operated display select switch, no operation

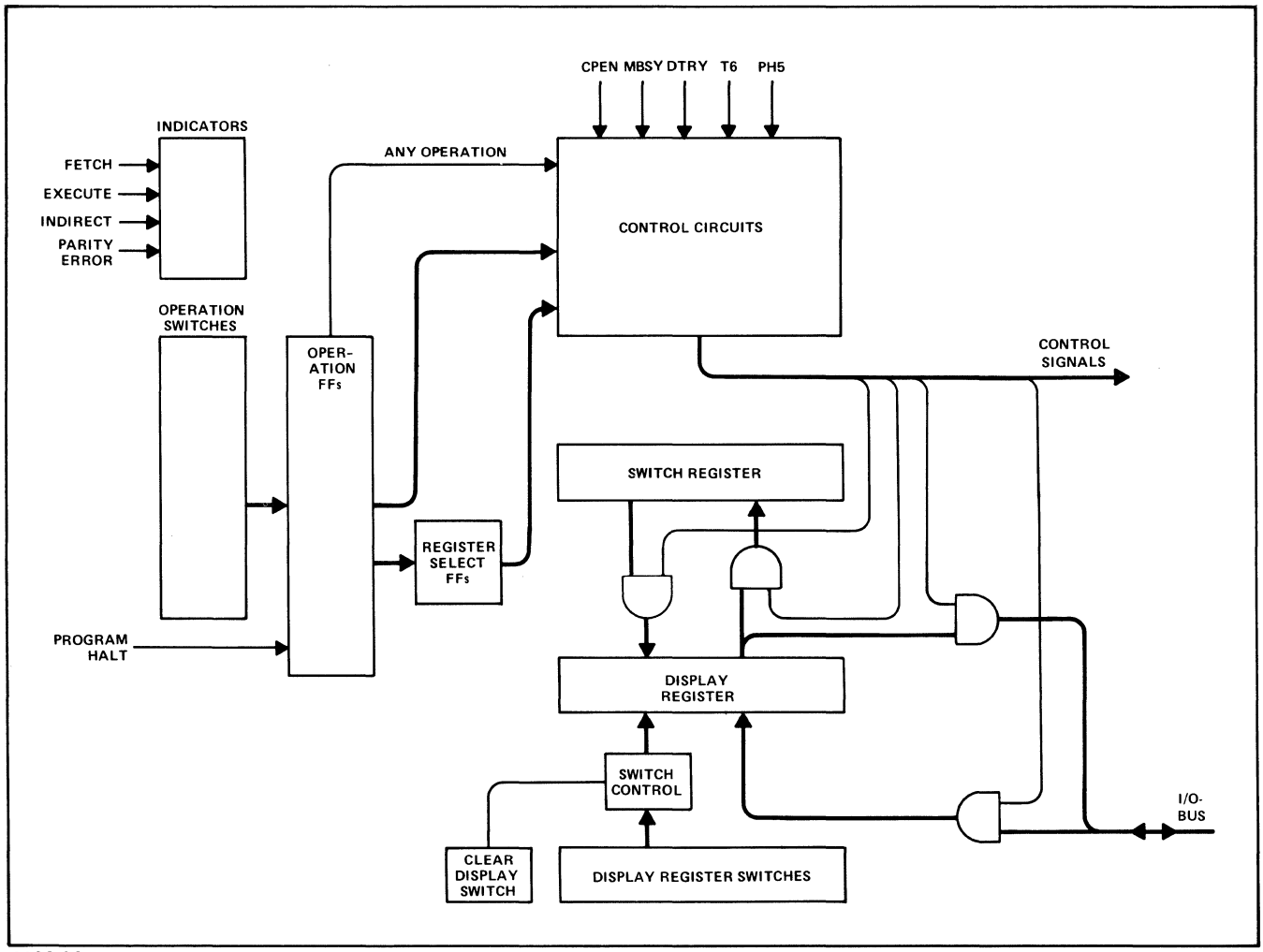
will occur during the display to selected register time. Display to selected register time lasts for one 196-nanosecond time period.

c. STM. The time period designated Store in Memory (STM) delays the operator panel cycle if the previous display select operation was memory data and a clear-write memory cycle is required. The panel Control Circuits monitor the MBSY signal from the memory section and when MBSY becomes false, the operator panel cycle is allowed to continue. Store in memory time lasts for 980 nanoseconds if a memory clear-write cycle is required and 196 nanoseconds if no memory cycle is required.

d. UDS. During Update Select (UDS) time, the Display Select FFs are clocked. If the operator panel cycle is initiated by pressing a display select operation switch, the update select time causes the corresponding Display Select FF to set. This Display Select FF indicates the source of the display register data at the end of the operator panel cycle and is used for reference during the display transfer time of the next operator panel cycle. Also, during update select time, an INCM or DECM signal is generated if the operation switch causing the cycle is INCREMENT M or DECREMENT M.

e. DO. The next time period in the operator panel cycle is designated DO. This applies primarily to the three operations that affect the run/halt status of the computer. These operations are cycle, instruction step, and run. The DO time of the operator panel cycle delays the remainder of the cycle until the computer control section signals that its part in the operation is complete. Also, if the operation is caused by the LOADER ENABLE switch, the loader enable circuitry is toggled during the DO time.

f. RDM. If the operator panel cycle is caused by a program halt, the HALT operation switch, or the MEMORY DATA operation switch, a read-write memory cycle is required to get memory data for display. This read-write cycle takes place during the Read Memory



2133-30

Figure 3-10. Operator Panel, Block Diagram

(RDM) time. The read memory time ends when the memory section signals that data is ready (signal DTRY true). If no read-write memory cycle is required, no operation occurs and RDM time ends after 196 nanoseconds.

g. SRTD. Selected Register To Display (SRTD) time is a 196-nanosecond time period during which the display register is updated to display the content of the selected register. This occurs every operator panel cycle even if no change is made in the selected display. If the selected display is MEMORY DATA, the selected register at this time is the memory section T-register.

h. WAIT. The time period designated WAIT is controlled by an RC time delay (approximately 6 milliseconds) circuit and is provided to ensure that the operation switch contacts have had sufficient time to stop bouncing before ending the cycle. WAIT time ends when the RC delay period has ended and the operation switch has been released.

i. DONE. DONE time is a 196-nanosecond time period that signifies the end of the operator panel cycle by disabling the OPIH circuits so that another operator panel cycle may be initialized.

3-133. CONTROLLER PANEL.

3-134. The controller panel (option 001 to the 2100A Computer) is an abbreviated version of the operator panel for use with applications that do not require panel control of the computer working registers. The controller panel consists of four switch-indicator combinations (RUN, HALT, PRESET, and LOAD), an indicator (PARITY), and five removable jumpers. The following paragraphs describe the functional operation of the switches, indicators, and jumpers on the controller panel.

3-135. CONTROLLER PANEL JUMPERS.

3-136. Positions for five jumper wires on the controller panel printed-circuit card are accessible by removing the controller panel cover. The presence or absence of these jumpers is determined by the size of the computer memory and the type (disc or paper tape) of the basic binary loader used with the computer. With these jumpers properly positioned, the starting address of the loader is placed on the I/O-bus lines, bits 4 through 14, during a load operation. The load operation generated by pressing the LOAD switch is further described in paragraph 3-140. Refer to paragraph 1-37 and figure 1-7 for information on the location and proper configuration of the jumpers for the various computer memory sizes.

3-137. CONTROLLER PANEL SWITCHES AND INDICATORS.

3-138. All controller panel switches, when operated, initiate a time delay circuit which inhibits further switch operations for the duration of the delay period (approximately six milliseconds). This prevents switch contact bounce from triggering the controller panel circuitry after an operation has started. The LOAD, PRESET, and RUN switches operate only when the computer is in the halt mode; the HALT switch operates only when the computer is running.

3-139. The following paragraphs provide a functional description of the operation of the controller panel switches and indicators.

3-140. LOAD SWITCH AND INDICATOR. If the jumpers described in paragraph 3-136 are properly placed, operation of the LOAD switch causes the starting address of the basic binary loader to be transferred via the I/O-, S-, and T-buses to the computer P-register. A true LOAD signal from the controller panel to the memory section allows access to the loader portion of the memory. The computer then enters the run mode and executes the contents of the loader. When the load operation is complete, a halt instruction in the loader program halts the computer and causes the LOAD signal to go false protecting the loader until the LOAD switch is again operated. The indicator portion of the LOAD switch is lit as long as the loader is enabled.

3-141. PRESET SWITCH AND INDICATOR. When the PRESET switch is operated, the controller panel generates several signals which preset the internal and external (I/O) circuitry of the computer and clear the A-, B-, and P-registers. The indicator portion of the PRESET switch lights when the PRESET switch is operated and when control FF 4 is cleared indicating that the power-fail circuitry is disabled. Pressing the PRESET switch sets control FF 4 which re-enables the power-fail circuitry.

3-142. HALT SWITCH AND INDICATOR. When the HALT switch is operated and the computer is in the run mode, a signal to the computer control section causes the computer to halt at the end of the present phase of operation. If the computer is running as a result of a load operation, pressing the halt switch causes the LOAD signal to go false protecting the loader. The indicator portion of the HALT switch is lit as long as the computer is in the halt mode

3-143. RUN SWITCH AND INDICATOR. The RUN switch, when pressed, places the computer in the run mode. This disables all controller panel switches except the HALT switch. Prior to actally beginning the run operation, the RUN switch circuitry clears the LOAD switch circuits to ensure that the loader is protected. The indicator portion of the RUN switch is lit as long as the computer is in the run mode.

3-144. PARITY INDICATOR. The Parity indicator lights when a memory section parity error has been detected indicating that steps must be taken to troubleshoot and correct the source of the parity error. If the parity error circuits are operating in the parity error halt mode, the PARITY indicator will remain lit until the PRESET switch is pressed. If the parity error circuits are operating in the parity error interrupt mode, the PARITY indicator remains lit only until the parity error interrupt has been acknowledged.

3-145. SPECIAL COMPUTER FUNCTIONS.

3-146. The theory of operation to this point has been concerned with the basic computer functions required for routine operation of the 2100A Computer. The following functions of the 2100A Computer are not required for computer operation but add to the versatility of the computer. These special functions are:

a. Parity Error.
b. Memory Protect.
c. Power-Fail.
d. Direct Memory Access.

3-147. The following paragraphs describe the operation of each of the above functions.

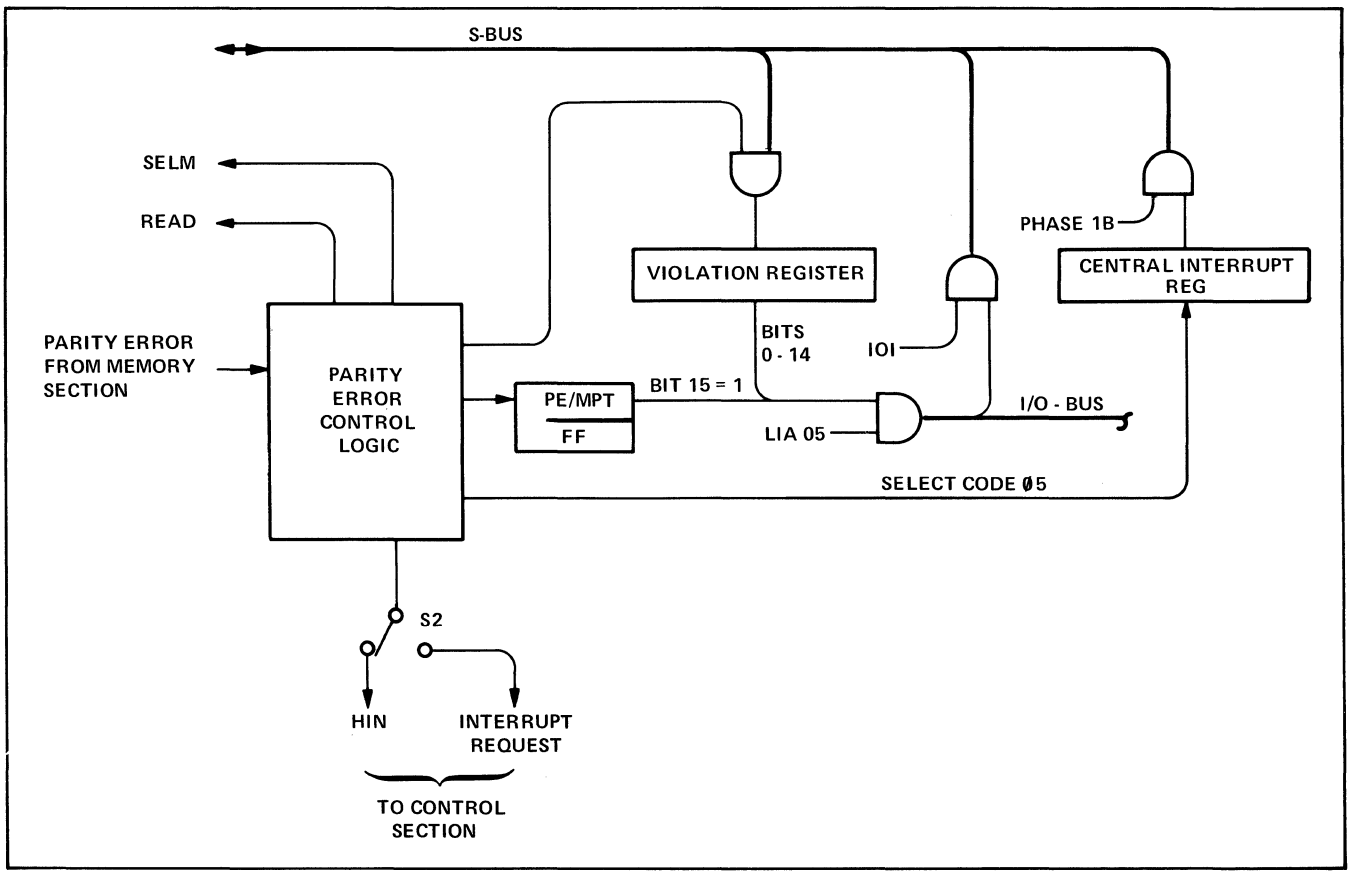
3-148. PARITY ERROR.

3-149. GENERAL. Paragraph 3-36 describes the memory section parity logic during memory read-write operations. If, during a memory read operation, a parity error is detected, the parity error function provides an orderly response by the computer.

3-150. Figure 3-11 is a functional diagram of the parity error and associated circuits. The parity error circuits are part of the computer I/O section. A two-position switch (S2 on I/O Buffer Card A8) allows the operator to select either the parity error halt or parity error interrupt mode of operation. The following paragraphs describe the functional operation in either mode when a parity error is detected.

3-151. PARITY ERROR HALT. With switch S2 in the HALT position, a parity error detected by the memory section parity logic results in a HIN signal to the computer control section. This simulates a programmed halt instruction and halts the computer at the end of the following phase of operation. A PEH signal is also generated and sent to the operator panel circuits to light the PARITY indicator on the panel.

3-152. PARITY ERROR INTERRUPT. With switch S2 in the INT position, a parity error causes an interrupt to a programmed subroutine to service the parity error. When a parity error occurs while the computer is running, the address of the word causing the parity error is transferred from the M-register (bits 0 through 14) via the S-bus to the Violation Register. This requires an extra clock period of 196 nanoseconds, which is inserted by freezing the central processor for one clock period. The Violation Register also stores the address of memory protect violations (paragraph 3-159). To distinguish between memory protect and parity error violations, bit 15 of the Violation Register is set by the Parity Error Control Circuits. This bit must be checked by software during the interrupt subroutine.



2133-31

Figure 3-11. Parity Error, Functional Diagram

3-153. The parity error also causes I/O address 05 to be stored in the Central Interrupt Register to provide a link to the parity error interrupt subroutine. An interrupt request from the Parity Error Control Circuits to the computer control circuits causes the computer to enter phase 1B. The computer then fetches the instruction stored at memory location 000005 (usually a JSB instruction) and proceeds with the interrupt subroutine. Typically, the subroutine transfers the Violation Register content via the I/O-bus and S-bus to the A- or B-register, checks bit 15, and uses bits 0 through 14 to fetch and display the memory word causing the parity error.

3-154. MEMORY PROTECT.

3-155. GENERAL. The memory protect function of the computer allows a selected area of memory to be protected against alteration by memory reference instructions. Also, when enabled, it prohibits the execution of I/O instructions except those referencing I/O address 01 (switch and overflow registers). This feature limits control of I/O operations to interrupt control only, giving exclusive control of I/O operations to a set of interrupt subroutines referred to as an executive program. The following memory reference instructions will initiate a memory protect interrupt if the instruction references a protected memory address.

a. JMP.
b. JSB.
c. ISZ.
d. STA.
e. STB.
f. DST.

3-156. The upper limit of the protected area of memory is loaded into the F- (Fence) register by an OTA or OTB instruction addressed to I/O address 05. The lower limit of the protected area is memory address 00002 for all of the above instructions. In addition, the JMP instruction is not allowed to reference the A- or B-registers (addresses 00000 and 00001).

3-157. DETECTING A MEMORY PROTECT VIOLATION. Figure 3-12 shows the functions involved in the detection of a memory protect violation. During the execute phase of any of the above listed memory reference instructions, a ROM microinstruction provides the following in the R-Bus, S-Bus, function, and skip fields respectively.

a. F. Transfer F-register content to the R-bus.

b. S1. Transfer SP1-register content to the S-bus.

c. DEC. Enable DEC function. The DEC function subtracts the S-bus content from the R-bus content and decrements the result.

d. NMPV. Enable NMPV (No Memory Protect Violation). The skip field NMPV checks bit 15 of the word resulting from the DEC function. If bit 15 is a logic 1, indicating no memory protect violation or if memory protect is turned off, a ROM skip is enabled. If bit 15 is a logic 0 and memory protect is on, there is a memory protect violation and the skip is not enabled. The presence or absence of a skip directs the ROM to the appropriate microinstruction to complete the execution of the instruction if no memory protect violation has occurred, or inhibit execution of the instruction if a memory protect violation has occurred. The skip field NMPV also checks the A- and B-addressable logic so that a JMP instruction referencing the A- or B-registers can be inhibited. If a memory protect violation is detected, the memory protect circuits are signaled to request an interrupt.

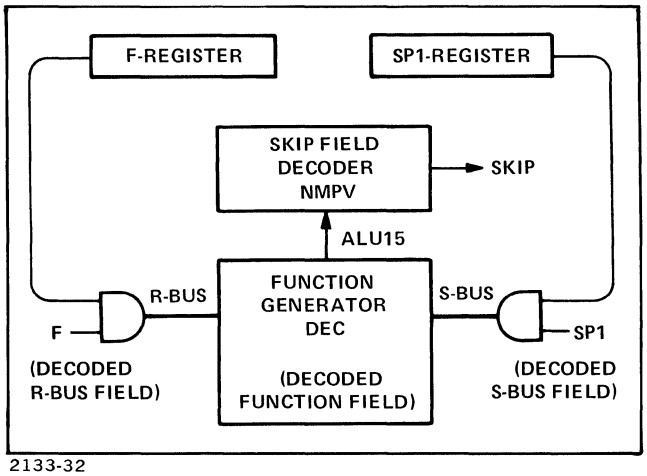
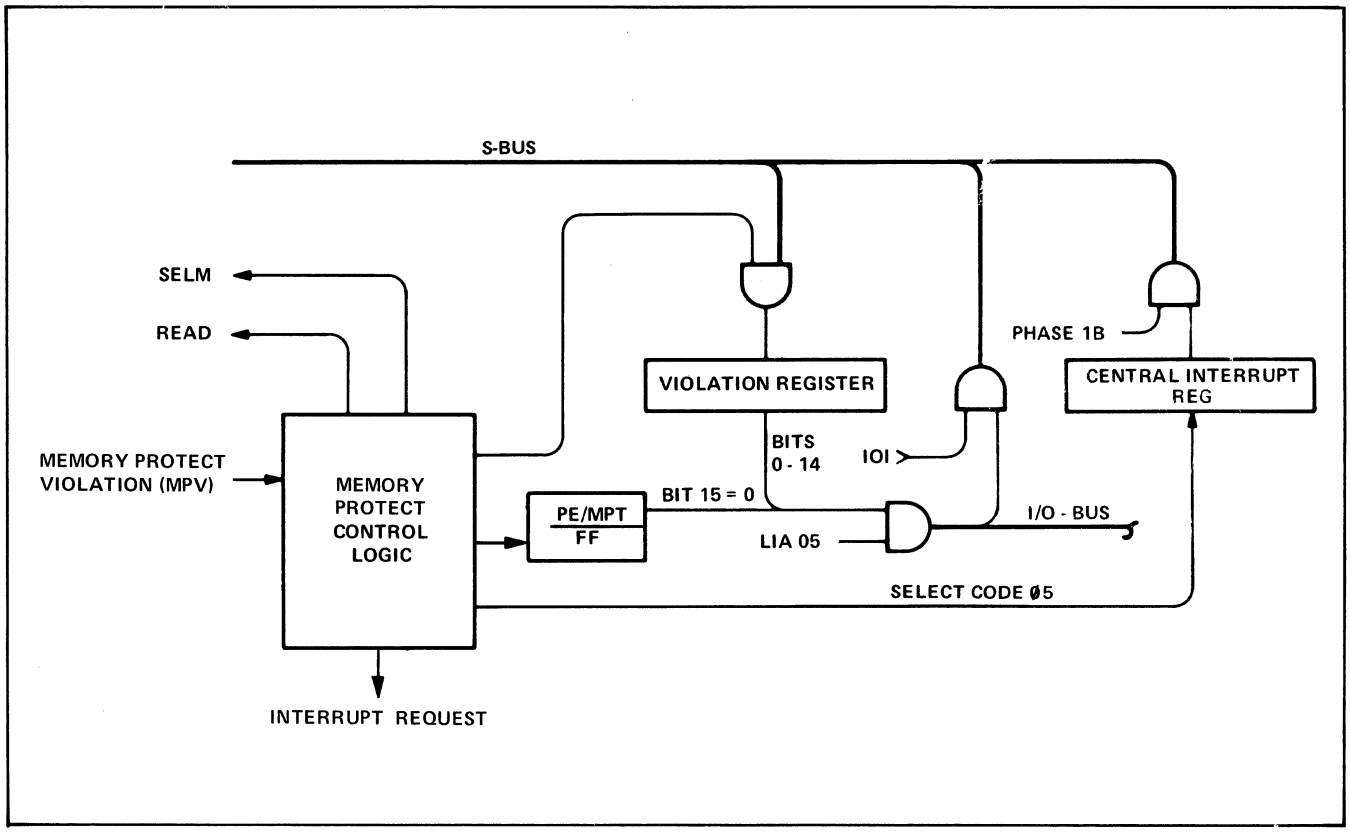


Figure 3-12. Memory Protect Violation Detection, Functional Diagram

3-158. Refer to Section IV of this manual for additional information on the ROM microprogram routines for the six memory reference instructions listed in paragraph 3-155.

3-159. MEMORY PROTECT INTERRUPT. Figure 3-13 is a functional diagram for a memory protect interrupt. When a memory protect violation is detected, the address of the violation is transferred from the M-register (bits 0 through 14) via the S-bus to the Violation Register. As described in paragraph 3-152, the Violation Register also stores the address of any parity error that may occur. Bit 15 of the Violation Register is provided by the PE/MPT FF which is always cleared by a memory protect violation. This bit is checked by software during the interrupt subroutine.

3-160. The memory protect violation also causes I/O address 05 to be stored in the Central Interrupt Register. An interrupt request from the Memory Protect Control circuits causes the computer to enter phase 1B. The computer then fetches the instruction stored at memory location 05 (usually a JSB instruction) and proceeds with the interrupt subroutine. Typically, the subroutine transfers the Violation Register content via the I/O-bus and the S-bus to the A- or B-register, checks bit 15, and uses bits 0 through 14 to display the memory word causing the memory protect violation.



2133-33

Figure 3-13. Memory Protect Interrupt, Functional Diagram

3-161. POWER-FAIL.

3-162. GENERAL. The power-fail function of the computer allows an orderly shutdown of the computer if power to the computer fails or drops below the minimum voltage required for proper operation. In addition, when power is restored, the computer can be set to automatically continue with the program that was being executed at the time of the power loss. The power-fail function can be operated in either the halt mode or interrupt mode. The following paragraphs describe these modes of operation.

3-163. In the halt mode, a drop in power causes the computer to halt at the end of the present phase of operation. Also, the memory section and the I/O section are disabled to prevent alteration of data during the time power is going down.

3-164. In the interrupt mode, a drop in power initiates an interrupt to memory location 00004. A JSB instruction at location 00004 directs the computer to a subroutine (described in the computer Reference Manual) which contains the necessary software to service the computer during power-down and power-up operations. During power-down, the subroutine stores the contents of all registers containing data that may be pertinent to remaining program operations, then halts the computer. A power-fail interrupt carries the highest interrupt priority and cannot be disabled by program means.

3-165. When power returns, an interrupt to location 00004 is again executed. The power-up portion of the subroutine then restores the register contents and returns control to the main program at the point where interrupted.

3-166. The power-fail circuits monitor the PWU signal to provide the halt and interrupt mode capabilities. The following paragraphs describe the generation and timing of these signals.

3-167. PWU SIGNAL. The Power Up (PWU) signal originates in the computer power supply where the logic supplies are monitored by the protection and control circuits in the power supply. Figure 3-14 illustrates the power supply output and resulting PWU signal levels during power-down and power-up conditions. The 700-millisecond delay during power-up is to ensure that all power supply voltages have reached proper regulated levels before starting the computer. If the power-fail function is in the halt mode, a false PWU signal generates an HIN (Halt Instruction decoded) signal to halt the computer. If in the interrupt mode, a false PWU signal initiates a power fail interrupt.

3-168. PON SIGNAL. The Power On Normal (PON) signal, shown in figure 3-15, monitors the PWU signal and provides a disabling signal to the memory and I/O sections in the event of a drop in power. The PON signal goes false approximately 550 microseconds after a false PWU signal is

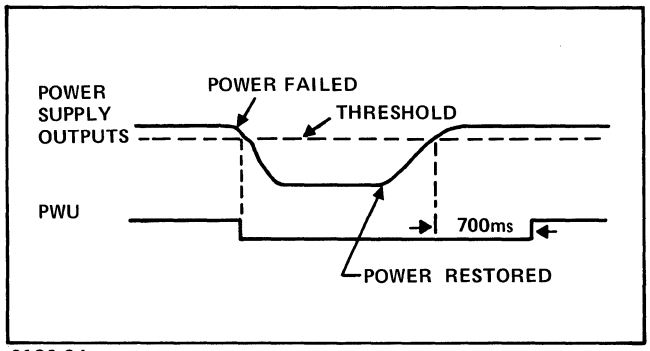


Figure 3-14. PWU Signal, Timing Diagram

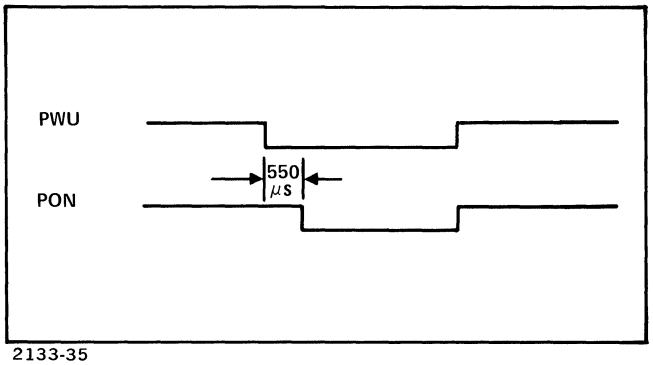


Figure 3-15. PON Signal, Timing Diagram

detected. This allows sufficient time to execute the power-down routine before disabling the computer memory. When power returns, the power-fail interrupt logic is enabled so that an interrupt to the power-up portion of the subroutine can be accomplished.

3-169. INTERRUPT OPERATION. Figure 3-16 shows the functional operation of the power-fail logic. This logic is located on I/O Control Card A7. With switch S1 in the ARS (Auto-Restart) position, a change in the state (high-to-low or low-to-high) of the PWU signal is felt by the interrupt logic which stores address 04 in the Central Interrupt Register and generates an INT signal. The INT signal causes the next computer phase to be phase 1B which fetches the contents of address 00004 in memory.

3-170. The Direction Logic consists primarily of a direction FF which sets during power-up and clears during power-down. After entering the subroutine, the direction flip-flop is tested by an SFC instruction addressed to address 04. If power is going down, an SKF signal directs the computer to the power-down portion of the subroutine. If power is going up, no SKF signal is generated and the computer executes the power-up portion of the subroutine. Refer to the sample power-fail subroutine in the computer Reference Manual for further information on the power-fail interrupt subroutine.

3-171. When a power-fail interrupt is generated, the interrupt logic clears the power-fail interrupt control logic to prevent any further attempts to interrupt during the subroutine. At the end of both power-up and power-down portions of the subroutine, the control logic must be set by a CLC 04 or STC 04 instruction to re-enable the interrupt logic. For program compatability with other HP computers, a CLC 04 is used at the end of the power-down routine and a STC 04 at the end of the power-up routine.

3-172. DIRECT MEMORY ACCESS.

3-173. GENERAL. The Direct Memory Access (DMA) function of the computer provides a two-channel direct data path between the compuer memory and a software selected I/O device. The DMA circuits accomplish data transfer by stealing a memory cycle rather than interrupting to a service subroutine. During a DMA data transfer, the central processor is disabled and the DMA circuits supply the required control signals to operate the memory and I/O device. Consecutive memory cycles can be utilized by DMA allowing a maximum data transfer rate of one million words per second. DMA data transfers are accomplished in blocks with the block length specified by software. Maximum block length is equal to the size of the computer memory. The DMA circuits can be programmed to interrupt at the end of a data block transfer to a subroutine to re-initialize DMA for another data block transfer.

3-174. Instructions for program initialization of the DMA circuits are provided in the computer Reference Manual. The following discussion provides a functional description of the initialization of the DMA circuits and the operation of the DMA circuits during a DMA cycle.

3-175. DMA INITIALIZATION. The computer Reference Manual describes three control words used to initialize a DMA channel. The control words are briefly described as follows:

a. Control Word 1 (CW1). Specifies the select code of the I/O device to provide or receive data (bits 0 through 5) and if CLC (bit 13) or STC (bit 15) signals are to be provided to the I/O interface after each word transfer.

b. Control Word 2 (CW2). Specifies input or output DMA operation (bit 15) and the starting address in memory (bits 0 through 14) of the data block.

c. Control Word 3 (CW3). Specifies the length of the data block (bits 0 through 15) and is expressed in 2's-complement form.

3-176. Figure 3-17 is a simplified logic diagram showing channel-one of the DMA circuits. The shaded area represents the control words as stored in the DMA circuits. All three control words are transferred to the DMA circuits via the S-Bus.

3-177. Control Word 1 is loaded into the Service Select Register, CLC Select FF, and STC Select FF by an OTA 06 instruction. Control words 2 and 3 are both loaded into their respective registers by an OTA 02 instruction. A programmed CLC 02 clears the Register Load Control and

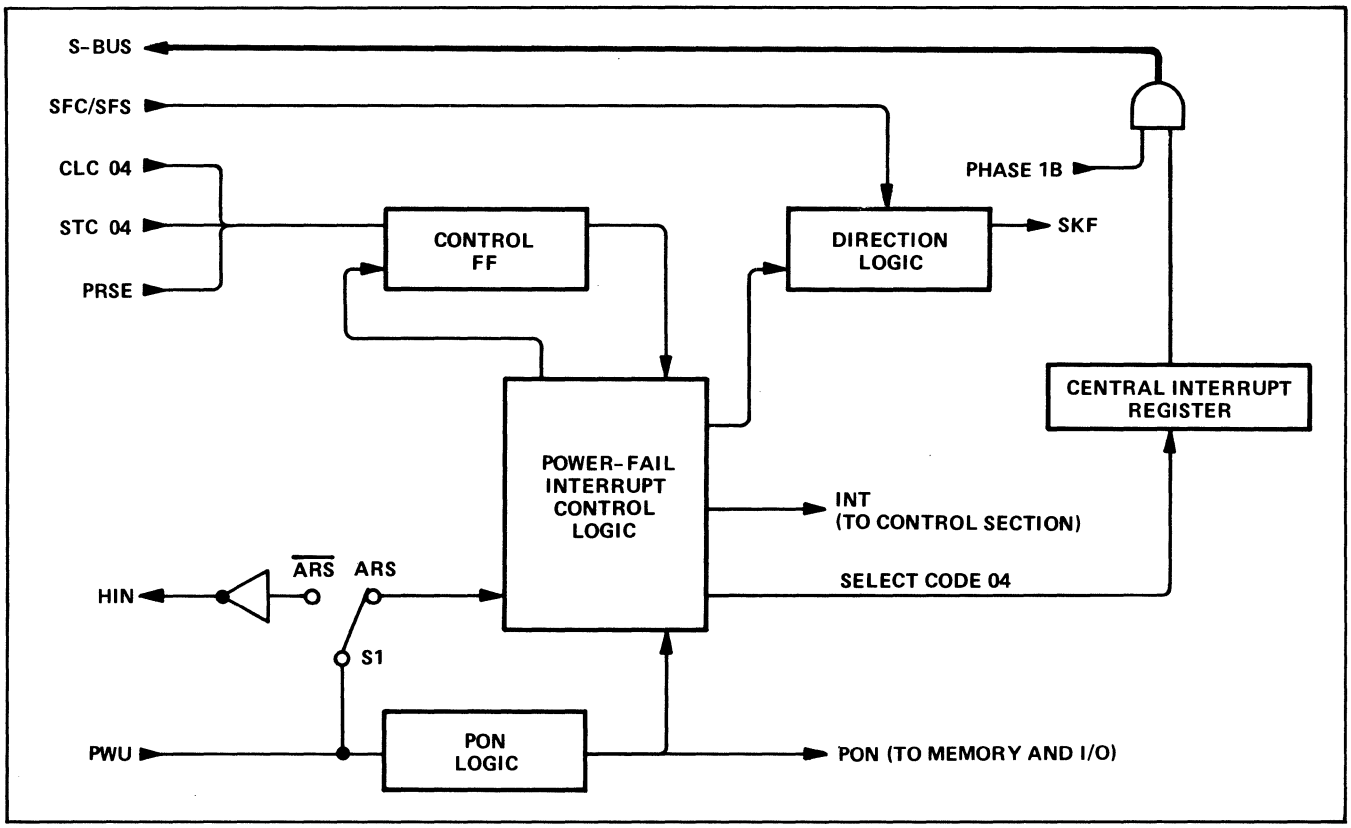


Figure 3-16. Power-Fail, Functional Diagram

enables the S-bus data to the Memory Address Register and the In/Out Select FF. An OTA 02 instruction with Control Word 2 in the computer A-register then transfers the control word to its respective registers. Prior to transferring Control Word 3, an STC 02 instruction sets the Register Load Control and enables the S-bus data to the Word Count Register. Another OTA 02 instruction with Control Word 3 in the computer A-register transfers the 2's complement of the data block length to the Word Count Register.

3-178. The last step to initialize the DMA circuits is accomplished by an STC 06 instruction. This sets the Control FF and the Transfer Enable FF. The Control FF in the set state enables the DMA interrupt logic and must be cleared by a CLC 06 instruction if an interrupt at the end of a data block transfer is not desired. The Transfer Enable FF in the set state enables the set input to the cycle request FF.

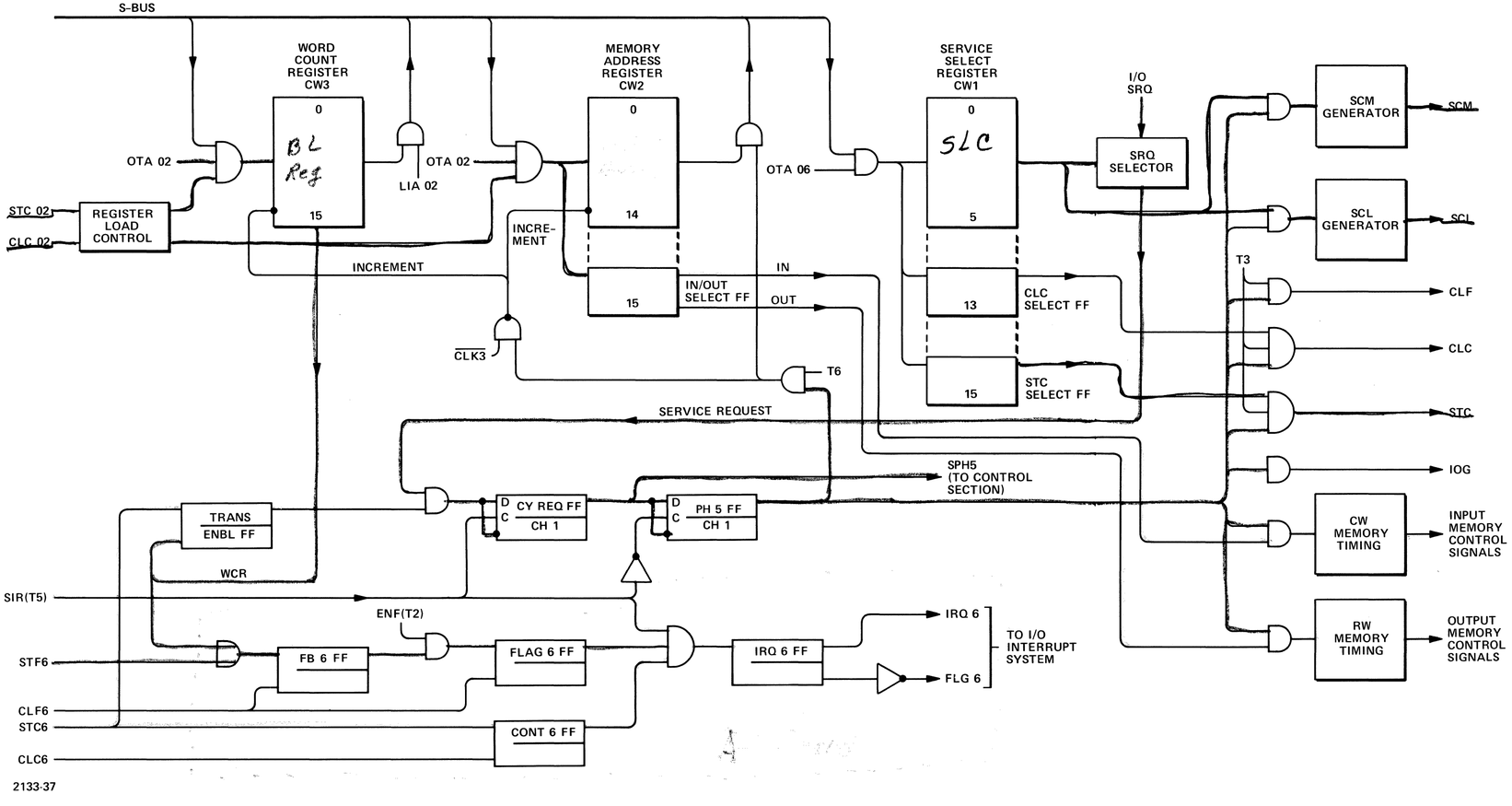
3-179. The channel-one DMA circuits are now initialized and a service request from the selected I/O device will initiate the first DMA cycle. Channel-two initialization is identical except for the select codes used to address the channel. For initialization of channel-two, select code 03 replaces select code 02 and select code 07 replaces select code 06.

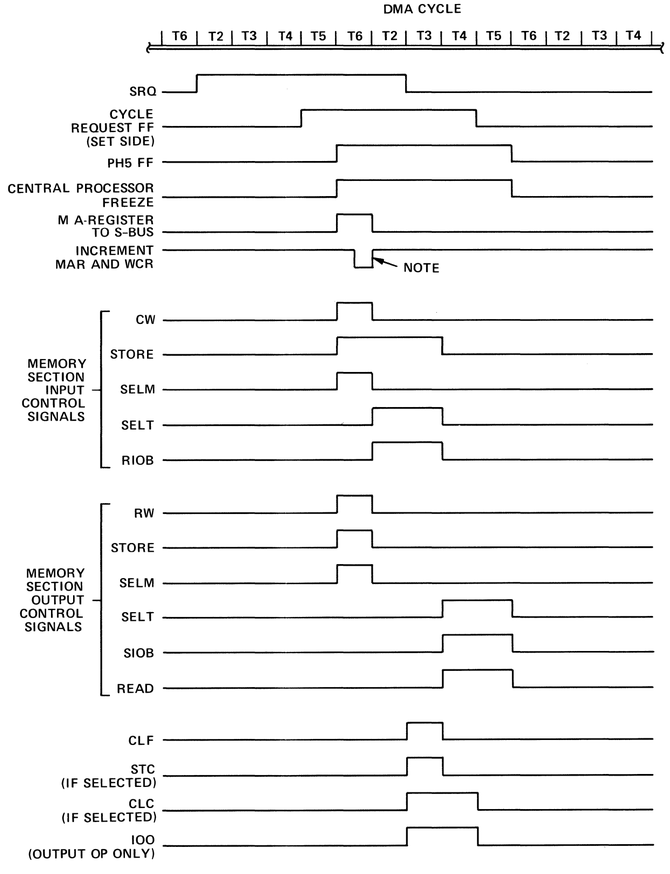
3-180. DMA CYCLE. In addition to the simplified logic diagram, figure 3-17 provides the overall timing of the DMA circuits during a DMA cycle. The timing diagram shows both input and output control signals; however, it is important to realize that these operations require separate initialization routines.

3-181. The DMA cycle is initiated when the selected I/O device signals, with a true SRQ signal, that it is ready for data transfer. The SRQ Selector provides a true Service Request to the Cycle Request FF. The Cycle Request FF is clocked to the set-state by the leading edge of signal SIR at T5 and the PH5 FF is clocked to the set-state by the trailing edge of the SIR signal (at the beginning of T6). The SPH5 signal to the control section causes the central processor to freeze at I/O time T6 to prevent further processing of programmed instructions until the DMA cycle is complete. The DMA cycle begins at T6 and continues until the PH5 FF is cleared at the next time T6. At T6 during the DMA cycle, the Memory Address Register output is strobed onto the S-bus and at the end of this time T6, the Memory Address Register and the Word Count Register are incremented for the next DMA cycle.

3-182. The remaining signals shown by figure 3-17 are DMA-generated control signals to the Memory and I/O sections of the computer for input and output DMA operations.

3-183. Input Operation. Control signals generated by the DMA circuits and shown by figure 3-17 perform the following operations during a DMA input operation:





NOTE: MEMORY ADDRESS AND WORD COUNT REGISTERS ARE INCREMENTED BY POSITIVE-GOING EDGE OF INCREMENT SIGNAL.

Figure 3-17. DMA Simplified Logic and Timing Diagram

a. Signal CW, at time T6, initiates a Memory Section clear-write cycle to begin at time T2.

b. Combined true STORE and SELM signals, at time T6, load the S-Bus data into the memory section M-register.

c. Signal RIOB, at time T2T3, transfers input data from the I/O device interface circuits via the I/O-bus to the S-bus.

d. Combined true STORE and SELT signals, at time T2T3, load S-bus data into the memory section T-register for transfer to the core memory.

e. Signal CLF, at time T3, causes the I/O device SRQ signal to go false.

f. Signal STC, at time T3, if selected during initialization, restarts the I/O device for the next data transfer. Signal CLC, at time T3T4, if selected, disables the I/O device.

3-184. The input DMA cycle is now complete for one data word transfer.

3-185. Output Operation. Control signals generated by the DMA circuits and shown by figure 3-17 perform the following operations during a DMA output operation:

a. Signal RW, at time T6, initiates a memory section read-write cycle to begin at time T2.

b. Combined true STORE and SELM signals, at time T6, load the S-bus data into the memory section M-register.

c. Combined true READ and SELT signals, at time T4T5, transfer memory section T-register data to the S-bus.

d. Signal SIOB, at time T4T5, transfers the S-bus data, via the I/O-bus, to the I/O interface circuits.

e. Signal CLF, at time T3, causes the I/O device SRQ signal to go false.

f. Signal STC, at time T3, if selected, signals the I/O device to accept data.

Note: Depending on the I/O device and its characteristics, signal STC may not be required. Refer to the applicable I/O device and interface kit operating and service manuals for details on this requirement.

3-186. END DATA TRANSFER. As stated in paragraph 3-177, the Word Count Register is loaded with the 2's complement of the data block length. The Word Count Register is incremented every DMA cycle so that during the last cycle of the data block, a carry is generated out of the last stage (bit 15) of the Word Count Register. This carry, designated Word Count Rollover (WCR), clears the Transfer Enable FF and sets the Flag Buffer FF. The Transfer Enable FF, in the clear state, inhibits any further service requests to the cycle request FF. The Flag Buffer FF, in the set state, initiates the DMA interrupt logic.

3-187. At time T2 during the last DMA cycle, the Flag FF sets; if the Control FF is set (paragraph 3-178), the IRQ FF sets at time T5. Signals FLG and IRQ from the IRQ FF initate an I/O interrupt to the DMA channel interrupt address (00006 or 00007). A DMA interrupt service routine may then be used to re-initialize the DMA channel for another data block transfer.

3-188. FLOATING POINT.

3-189. GENERAL. The HP 12901A Floating Point Hardware Accessory Kit provides the computer with the necessary logic to perform floating-point mathematical operations. The floating-point microprogram is contained in six ROM packs installed in the module 1 position (U25, U26, U27, U35, U37, and U65) on ROM Control Card A2. Mapping to the correct ROM starting address for execution of the floating-point user instructions is accomplished by the proper configuration of jumpers W4 and W5 in the ROM mapper circuits (refer to paragraph 3-271). The configuration of jumpers W1, W2, W3, and W6 in the Non-Existent ROM (NER) FF circuits (refer to paragraph 3-282) are also changed to include ROM module 1.

3-190. FLOATING-POINT OPERATION. Floating-point processing is a method of mathematically manipulating numbers written in exponential form. Within the computer this process applies to numbers written in binary form and normalized (that is, for positive numbers, the first digit to the right of the binary point is one and all digits to the left of the binary point are zeros. For negative numbers, the first digit to the right of the binary point is zero and all digits to the left of the binary point are ones). A floating-point number is a decimal number which has two components; a signed or unsigned leading number (integer or fraction or both) and a signed or unsigned exponent. The exponent specifies the power of 10 by which the leading number is multiplied. The floating-point number may have any of the following formats:

$$\pm n.n,\ \pm n.,\ \pm n.E\pm e,\ \pm .nE\pm e,\ \pm n.nE\pm e,\ \pm nE\pm e$$

("E" separates the exponential part from the leading number part.)

3-191. The floating-point number is converted to binary form, normalized, and stored in two computer words referred to as the floating-point quantity. The floating-point quantity is composed of two parts; the fraction and the exponent. If either the fraction or the exponent is negative, that part is stored in the two's complement form. Figure 3-1 explains the binary format of a floating-point quantity.

3-192. FLOATING-POINT INSTRUCTIONS. Floating-point has a repertoire of six instructions. They are as follows:

Note: In FAD, FSB, FMP, and FDV, add 980 ns to the execution time for each level of indirect.

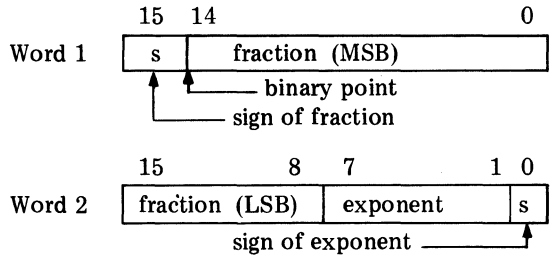
FAD; floating-point addition. Add the two-word floating-point quantity in the A- and B-registers to the two-word floating-point quantity in the specified locations. Store the two-word floating-point sum in the A- and B-registers.

Machine Code: 105000 octal

Calling Sequence:
```
FAD
DEF Y [,I]
```

Execution Time: 23.52 usec minimum
(fetch and execute) 59.78 usec maximum

Error Conditions: If the result is outside the range of representable floating-point numbers: $[-2^{127}, 2^{127}(1-2^{-23})]$. The overflow flag is set and the result $2^{128}(1-2^{-23})$ is returned to the A- and B-registers. If an underflow occurs (result within the range $[-2^{129}(1+2^{-22}), 2^{-129}]$), the overflow flag is set and the result 0 is returned.



The floating-point quantity is made up of a 23-bit fraction with sign and a 7-bit exponent with sign. The quantity must be in the approximate range of $\pm 10^{\pm 38}$ and zero.

Example: 0.45×10^{1} =

15	14 … 0	
0	100100000000000	word 1

15 … 8	7 … 1	0	
00000000	0000011	0	word 2

Reading the above binary form:

Bit 15 of word 1 indicates a positive fractional quantity.

Bit 0 of word 2 indicates a positive exponent.

Bits 7 through 1 of word 2 indicate an exponent of 3 ($\times 2^3$), indicating that the binary point is moved 3 places to the right of bit 14 of word 1 (between bits 12 and 11 of word 1).

Bits 14 through 12 of word 1 indicate a value of 4.

Bits 11 through 0 of word 1 and bits 15 through 8 of word 2 indicate a value of 0.5 (2^{-1}).

Thus the floating-point quantity is 4.5 or 0.45×10^{1}. (Note: bits to the right of the binary point have values of $2^{-1}, 2^{-2}, 2^{-3}, \ldots\ldots, 2^{-21}$.)

Figure 3-18. Binary Format of a Floating-Point Quantity

FSB; floating-point subtraction. Subtract the two-word floating-point quantity in the specified location from the two-word floating-point quantity in the A- and B-registers and store the difference in the A- and B-registers.

Machine Code: 105020 octal

Calling Sequence:
```
FSB
DEF Y [,I]
```

Execution Time: 24.50 usec minimum
(fetch and execute) 60.76 usec maximum

Error Conditions: Same as FAD

FMP; floating-point multiplication. Multiply the two-word floating-point quantity in the A- and B-registers by the two-word floating-point quantity in the specified locations. Store the two-word floating-point product in the A- and B-registers.

Machine Code:	105040 octal
Calling Sequence:	FMP DEF Y [,I]
Execution Time: (fetch and execute)	33.32 usec minimum 41.16 usec maximum
Error Conditions:	Same as FAD

FDV; floating-point division. Divide the two-word floating-point quantity in the A- and B-registers by the two-word floating-point quantity in the specified locations. Store the two-word floating-point quotient in the A- and B-registers.

Machine Code:	105060 octal
Calling Sequence:	FDV DEF Y [,I]
Execution Time: (fetch and execute)	51.94 usec minimum 55.86 usec maximum
Error Conditions:	Same as FAD

FIX; floating-point to integer format. Change the floating-point quantity in the A- and B-registers from floating-point format to integer format and place the integer in the A-register.

Machine Code:	105100 octal
Calling Sequence:	FIX
Execution Time: (fetch and execute)	5.88 usec minimum 8.87 usec maximum
Error Conditions:	If the floating-point exponent is <0, the integer 0 is returned. If the floating-point number is $\geq 2^{15}$, the decimal integer 32767 (=0777777 octal) is returned to the A-register and the overflow flag is set.

FLT; integer to floating-point format. Change the number in the A-register from integer format to floating-point format and place the floating-point quantity in the A- and B-registers.

Machine Code:	105120 octal
Calling Sequence:	FLT
Execution Time: (fetch and execute)	9.8 usec minimum 24.5 usec maximum
Error Conditions:	None

3-193. These instructions are non-interruptable. Any attempted interrupt is held off for the full execution time of the currently active floating-point instruction. However, DMA transfers are not held off.

3-194. DETAILED THEORY INTRODUCTION.

3-195. The detailed theory discussion is divided into functional logic blocks within each section of the computer, similar to the blocks shown in the overall block diagram of the computer (see figure 3-2). The reader should refer to the appropriate schematic diagram in the Diagrams Manual during the discussion to become familiar with the logic circuits.

3-196. CONTROL SECTION DETAILED THEORY.

3-197. CLOCK GENERATOR CIRCUITS.

3-198. The clock generator circuits, located on Timing and Control Card A1, consist of a 10.204 MHz oscillator, frequency divider circuit, and clock gating circuits. The clock generator circuits provide the necessary clock signals ($\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{CLK3}}$, CLK, and STCLK) for synchronous operation of the computer.

3-199. OSCILLATOR. The 10.204 MHz, crystal-controlled oscillator provides the time base for operation of the clock generator circuits. The oscillator output is applied to the clock inputs of the FDIV1 and FDIV2 FFs. The ENX (Enable External) and CLKX (Clock External) signals permit inhibiting the oscillator output and clocking the FDIV1 and FDIV2 FFs with a pulse generator, or similar device, to operate the computer at a slower clock rate during testing.

3-200. FREQUENCY DIVIDER. The frequency divider circuit, consisting of FDVI1 and FDIV2 FFs, divide the 10.204 MHz oscillator frequency by 2. The output from the FDIV1 FF furnishes the time period for the $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{CLK3}}$, and CLK signals. (See figure 3-19.) The combined outputs from both FFs furnish the time period for the STCLK signal.

3-201. CLOCK GATING CIRCUITS. The clock gating circuits permit the outputs from the frequency divider FFs to furnish the five clock signals. The clock gating circuits are enabled and disabled by the freeze logic on Microinstruction Decoder 1 Card A3 and the parity error and input/output group freeze logic on Timing and Control Card A1.

3-202. When the freeze logic on card A3 applies a false $\overline{FRZ}$ signal to the clock gating circuits, the $\overline{CLK1}$, $\overline{CLK2}$, and STCLK signals are inhibited. This prevents the ROM Address Register and ROM Instruction Register from being changed and inhibits execution of the ROM microinstruction. This prevents altering the contents of any registers, flags, etc., within the central processor or memory section.

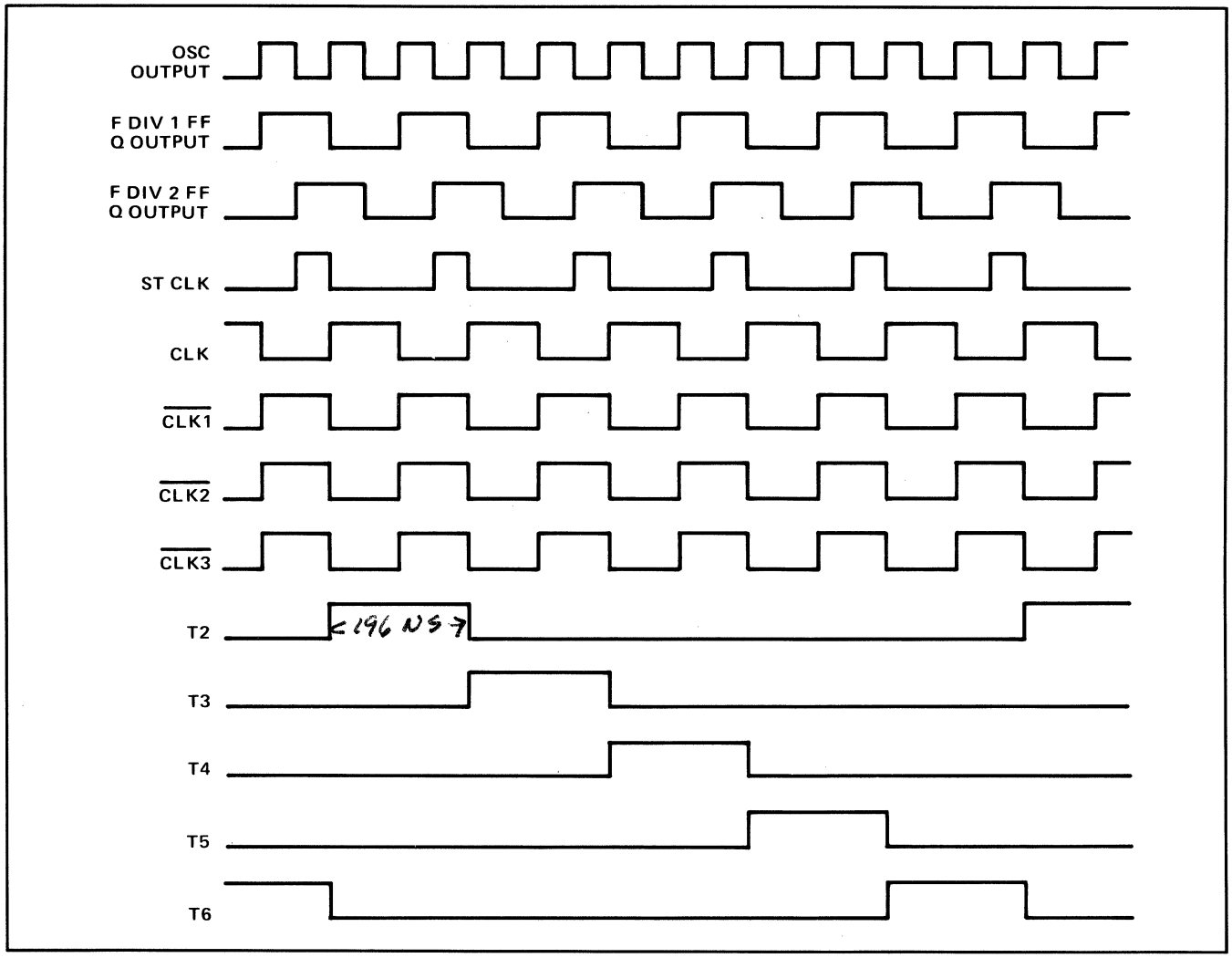
3-203. When the $\overline{FRZ}$ signal becomes true, the microinstruction causing the freeze is executed in the normal manner. The next microinstruction is then stored in the ROM Instruction Register and checked for a possible freeze requirement by the freeze logic.

3-204. PARITY ERROR FREEZE. If a parity error is detected by the parity error logic on I/O Buffer Card A8, the PEX signal applied to pin 63 of Timing and Control Card A1 becomes true during I/O time T4. This inhibits all clocks, except $\overline{CLK3}$, for one clock period. This furnishes an extra $\overline{CLK3}$ period to load the address of the word causing the parity error into the Violation Register on I/O Buffer Card A8 (refer to paragraph 3-152).

3-205. I/O FREEZE. The first ROM microinstruction in any of the microroutines for executing I/O instructions contains an IOG1 microcode in the special field. When the IOG1 microcode is detected by the special field decoder circuits, the IOG1 signal at pin 83 of Timing and Control Card A1 becomes true. If the ENF signal (which is always true at time T2) at pin 50 is false, all clocks are inhibited except $\overline{CLK3}$. This holds the microinstruction containing the IOG1 microcode in the ROM Instruction Register until the ENF signal is true. When ENF becomes true, the freeze is disabled and the microinstructions in the microroutine are executed sequentially starting at I/O time T2.

3-206. FREEZE LOGIC.

3-207. The freeze logic, located on Microinstruction Decoder 1 Card A3, consists of three flip-flops (HT6, PH5, and DT FFs) and gating circuits. The freeze logic monitors certain memory, interrupt, DMA, and divide operation signals to determine if a CPU freeze is necessary to synchronize the execution of the microprogram with the memory or I/O cycle. Some of the freeze conditions were discussed in the description of the clock generator circuits (refer to paragraphs 3-204 and 3-205).



2133-117

Figure 3-19. Clock Generator and I/O Time Period Generator Timing

3-208. If the requirements for a CPU freeze are met, the FRZ signal at pin 35 of card A3 becomes false. The false FRZ signal causes the clock generator circuits on Timing and Control Card A1 to inhibit all clocks ($\overline{CLK1}$, $\overline{CLK2}$, CLK, and STCLK) except $\overline{CLK3}$. This permits the memory and I/O cycles to continue while the execution of the microprogram in the central processor is inhibited.

3-209. When the freeze is no longer needed, the FRZ signal becomes true which enables all the clocks, and the central processor operation continues.

3-210. The conditions causing a CPU freeze that are detected by the freeze logic on card A3 are discussed in the following paragraphs. Two other conditions causing a freeze which are detected by the freeze logic on Timing and Control Card A1 is discussed in paragraphs 3-204 and 3-205.

3-211. MEMORY PROTECT OR PARITY ERROR INTERRUPT. When a memory protect or parity error interrupt occurs, the HT6 signal at pin 75 is true during time T5 of phase 1B. The HT6 FF sets at time T6 and remains set until time T6 of the following cycle. This provides a 980-nanosecond freeze to allow the priority chain to settle. Should there be another interrupt present in the I/O structure, this freeze prevents "inclusive-ORing" the two select codes into the Central Interrupt Register.

3-212. DMA CYCLE. When a DMA cycle is initiated, a true SPH5 signal is generated by the cycle request logic on Direct Memory Access (DMA) Card A9 beginning at time T5. The SPH5 signal remains true until the following time T5. The true SPH5 signal causes the PH5 FF in the freeze logic to set at time T6, and the PH5 FF remains set until the end of time T5 of the following cycle. This provides a 980-nanosecond freeze, beginning at time T6, to prevent further processing of programmed instructions until the DMA cycle is complete.

3-213. DIVIDE OPERATION. During execution of the ROM microroutine for the DIV user instruction, a DIV microcode is coded in the function field of one of the microinstructions. The execution time required for this microcode is 400 nanoseconds. Therefore, the freeze logic is used to gain the additional 200 nanoseconds.

3-214. When the DIV microcode is detected by the function field decoding circuits on Microinstruction Decoder 2 Card A4, and there is no skip condition present, the DIV signal at pin 83 of card A3 becomes false. The false DIV signal is inverted to provide a true input to gates A3U106A and A3U43A. The true output from the clear side of the DT FF is "anded" with DIV by A3U43A to start the CPU freeze. Also, the true clear output from the DT FF is "anded" with DIV by A3U106A to provide a true input to the set side of the DT FF. At the end of the present clock period, the DT FF sets which provides a false input to A3U43A and the freeze is disabled. At the end of the next clock period, the DIV signal is false and the DT FF clears. The 200-nanosecond freeze generated by the DIV signal provides the 400-nanosecond time period in which to execute the DIV microcode.

3-215. MEMORY READ/WRITE AND CLEAR/WRITE. Memory read/write and clear/write operations start at time T2 and end at the end of time T6. For memory operations to begin at time T2, the RW (Read/Write) or CW (Clear/Write) signal must be true at time T6 of the previous cycle. If an RW or a CW microcode is detected by the special field decoder during any time between T2 and T5, the freeze logic will cause a freeze until time T6. This will delay execution of the ROM microinstruction containing the RW (or CW) microcode until time T6.

3-216. When an RW or a CW microcode is detected by the special field decoder circuits, the RWCW signal at pin 31 of card A3 becomes true. If T6 is false, the freeze logic provides a false FRZ signal to the clock generator circuits and to the special field decoder circuits until T6 is true. The clock generator circuits inhibit all clocks (except $\overline{CLK3}$) until time T6. The special field decoder circuits inhibit the RW (or CW) signal from becoming true for a full clock period until time T6. (The memory circuits will not respond to a true RW or CW signal unless it is true during the last half of the clock period.)

3-217. READ T-REGISTER. During the first half of the memory cycle, data is read from memory into the T-register. Also during this time, the DTRY signal is false, indicating that valid data is not yet in the T-register. If a ROM microinstruction which contains a read T-register operation is decoded while the memory is executing the first half of a memory cycle, the freeze logic will cause a freeze to delay execution of the microinstruction until valid data is in the T-register.

3-218. The freeze logic determines the freeze requirement by monitoring the (T) signal line from the S-bus field decoder circuits and the DTRY signal at pin 25 of card A3. The (T) signal line is true when T is coded in the S-bus field, or when COND is coded in the S-bus field and neither the A-register or the B-register is addressed. If the (T) signal line is true when the DTRY signal is false, the freeze logic provides a false $\overline{FRZ}$ signal to the clock generator circuits to inhibit all clocks, except $\overline{CLK3}$. This holds the microinstruction in the ROM Instruction Register until the freeze logic is disabled. When the DTRY signal becomes true, the $\overline{FRZ}$ signal becomes true and the freeze is disabled.

3-219. STORE M-REGISTER. If an M microcode is detected in the store field of the ROM microinstruction, the true (M) signal from the store field decoder causes true STORE and SELM signals to be applied to the memory control logic on Data Control Card A107. The memory control logic, in turn, causes the data contained on the S-bus to be loaded into the M-register. If the memory is busy (MBSY signal is true), the SELM signal is inhibited, and the freeze logic generates a freeze (FRZ signal is false) until the MBSY signal becomes false near the end of the memory cycle. The microinstruction containing the M microcode is held in the ROM Instruction Register until the freeze is disabled ($\overline{FRZ}$ signal is true).

3-220. STEP GENERATOR LOGIC.

3-221. The step generator logic, located on Timing and Control Card A1, consists of two flip-flops (SG1 FF and SG2 FF) and associated gates and drivers. The function of the step generator logic is to provide a positive pulse, one clock period in duration, whenever an operational mode switch (RUN, HALT/CYCLE, or INSTR STEP) or the INTERRUPT SYSTEM, EXTEND, or OVF switch on the operator panel is pressed. The step generator logic also provides a positive pulse when power is resumed after a power fail with the computer set for automatic restart.

3-222. RUN LOGIC.

3-223. The run logic, located on Timing and Control Card A1, consists of five flip-flops and associated circuits for controlling the operational mode of the computer. The operational mode switches (RUN, HALT/CYCLE, and INSTR STEP) on the operator panel provide input signals to initiate the operation of the run logic. The circuit timing associated with the various modes is given in figures 4-97, 4-99, and 4-101 of the troubleshooting section.

3-224. RUN MODE. After the RUN switch on the operator panel is pressed, the Set Run Halt (SRH) signal becomes true. This causes the step generator logic to produce a positive pulse, one clock period in duration. The SRH signal, step generator pulse, and the true output from inverter A1U86F are "anded" to set the RH and RUN FFs and clear the DHLT FF at the end of the present clock period.

3-225. The true set output from the RUN FF provides a RUN signal to all the I/O slots and to the ROM control logic. The false set output from the DHLT FF causes a false Control Panel Enable (CPEN) signal which inhibits the operation of all switches on the operator panel except for the halt function of the HALT/CYCLE switch, the CLEAR DISPLAY, and DISPLAY REGISTER switches. The RH and RUN FFs remain set, and the DHLT FF remains cleared until the computer enters the halt mode. (Refer to paragraph 2-233.)

3-226. SINGLE INSTRUCTION MODE. The single instruction mode permits the computer to fetch one user instruction from memory and execute that instruction. After the instruction is executed, the computer enters the halt mode.

3-227. After the INSTR STEP switch on the operator panel is pressed, the Set Single Instruction (SSIN) signal from the operator panel becomes true. The SSIN signal, the step generator pulse, and the true output from inverter A1U86F are "anded" to set the SIN and RUN FFs and clear the DHLT FF at the end of the present clock period. The RUN and DHLT FFs perform the functions as described in the run mode discussion (refer to paragraph 3-219).

3-228. The SIN, RUN, and DHLT FFs remain in their present state until an EOP microcode is detected in the skip field during phase 3 of the ROM microroutine for the instruction being executed. When EOP is detected, the EOP signal becomes true. The set output from the SIN FF, the PH3 signal from the phase control logic, and the EOP signal from the end-of-phase logic are "anded", which clears the SIN and RUN FFs. At the end of the following clock period, the DHLT FF sets.

3-229. The false RUN signal applied to the ROM control logic causes false ENRM and IRAR signals which inhibit the ROM and prevents the RAR from incrementing. The true CPEN signal restores operation of the operator panel switches.

3-230. SINGLE CYCLE MODE. The single cycle mode permits the computer to operate for one phase only each time the HALT/CYCLE switch is pressed (with the computer in the halt mode). At the end of each phase, the computer enters the halt mode. This is accomplished by detecting EOP in the skip field of the ROM microinstruction. However, during execution (phase 3) of certain extended arithmetic group instructions and user macroinstructions, a CJMP microcode is located in the function field of the corresponding ROM microroutines. Detection of CJMP also will cause the computer to enter the halt mode at the end of the present clock period.

3-231. After the HALT/CYCLE switch is pressed, the Set Single Cycle (SSCY) signal from the operator panel becomes true. The SSCY signal, the step generator pulse, and the true output from inverter A1U86F are "anded" to set the SCY and RUN FFs and clear the DHLT FF at the end of the present clock period. The RUN and DHLT FFs perform the functions as described in the run mode discussion (refer to paragraph 3-219).

3-232. The SCY, RUN, and DHLT FFs remain in their present state until an EOP microcode is detected in the skip field, or a CJMP microcode is detected in the function field (whichever occurs first). When the EOP signal becomes true (or the $\overline{\text{CJMP}}$ signal false), it is "anded" with the set output from the SCY FF, which clears the SCY and RUN FFs. At the end of the following clock period, the DHLT FF sets.

3-233. HALT MODE. The halt mode is entered whenever one of the following conditions occur:

a. The HALT/CYCLE switch is pressed when the computer is in the run mode.

b. The user HALT instruction is decoded in the user program while the computer is in the run, single instruction, or single cycle mode (with memory protect function disabled).

c. A parity error is detected (with parity error switch on I/O Buffer Card A8 in the HALT position).

d. A power fail is detected (with automatic restart switch on I/O Control Card A7 in the $\overline{\text{ARS}}$, no automatic restart, position).

e. An EOP is detected during phase 3 of the single instruction mode (as described previously).

f. An EOP or CJMP is detected during the single cycle mode (as described previously).

3-234. Any of the conditions specified in steps "a" through "d" above cause the HIN signal to be true. The true HIN signal clears the RH FF which causes the output from inverter A1U86F to go true. The output from A1U86F enables gate A1U64C. When the EOP microcode is detected in the skip field, the output from A1U64C goes low which clears the RUN FF. At the end of the next clock period, the DHLT FF sets.

3-235. AUTOMATIC RESTART. When power is restored after a power failure, and the automatic restart switch on I/O Control Card A7 is set to the ARS (automatic restart) position, the run logic sets the computer to the run mode.

3-236. When power is restored, the automatic restart logic on I/O Control Card A7 provides a true Restart Pulse (RSSP) to the ROM control logic, step generator logic, and the run logic. The RSSP signal, step generator pulse, and the true output from inverter A1U86F are "anded" to set the RH and RUN FFs and clear the DHLT FF at the end of the present clock period. The computer is now in the run mode. (The affect of the RSSP signal on the ROM control logic is described in paragraph 3-317).

3-237. PHASE CONTROL LOGIC.

3-238. The phase control logic, located on Timing and Control Card A1, consists of four flip-flops and associated gating circuits. The purpose of the phase control logic is to determine which machine phase should be entered next, after the present machine phase is complete.

3-239. The machine phases are set by the $\overline{\text{PH1A}}$, PH1B, PH2, and PH3 FFs. The machine phase is changed when the flip-flops are clocked by "anding" the EOP signal from the end-of-phase logic on ROM Control Card A2 with the $\overline{\text{CLK1}}$ signal. The set phase signals (SPH1B, SPH2, and SPH3) are applied to the ROM mapper which provides ROM addressing information to the ROM Address Register (RAR). The true state of the appropriate set phase signal will set the corresponding flip-flop at the end of the clock period. Logic equations for the set phase signals are given in table 3-3. Flowcharts showing the various set phase conditions are contained in figure 3-9.

3-240. PHASE 1A. Phase 1A (the normal fetch phase) is entered only from phase 3. The conditions for entering phase 1A are: (1) no nterrupt present (INT signal false), or (2) the previous instruction was a JMP,I or JSB,I with no interrupt due to memory protect violation, nor was the instruction the third indirect executed in a sequence (IMPV signal true).

3-241. PHASE 1B. Phase 1B (the interrupt fetch phase) is entered from any of the other three phases or by an automatic restart. The conditions for entering phase 1B from phase 1A are: (1) an interrupt is present (INT signal true), (2) the instruction fetched during phase 1A was a memory reference group instruction, but not a JMP instruction, (3) either the instruction was not a JSB, or not an indirect, or an interrupt due to a memory protect violation.

3-242. The conditions for entering phase 1B from phase 2 are: (1) an interrupt is present (INT signal true) and (2) the instruction contained in the I-register is not a JMP,I or JSB,I (unless it is the third one in succession being processed, in which case the CT3 signal would be true).

3-243. The conditions for entering phase 1B from phase 3 are: (1) an interrupt is present (INT signal true), and (2) the previous instruction executed was not a JMP,I or a JSB,I, or if it was a JMP,I or JSB,I, the interrupt is due to a memory protect violation or the Indirect instruction is the third Indirect executed in a sequence (IMPV signal true).

3-244. The condition for entering phase 1B from an automatic restart is when power is restored, the automatic restart circuits on I/O Control Card A7 apply a true Restart Pulse (RSSP signal) to the step generator logic and to the ROM control logic. The step generator logic produces a positive pulse, one clock period in duration, which is "anded" with the true RSSP signal and the $\overline{\text{RH FF}} \cdot \overline{\text{SIN FF}} \cdot \overline{\text{SCY FF}}$ signal line (from the run logic) in the ROM control logic. The false output from gate A1U95B in the ROM control logic direct-sets the $\overline{\text{PH1A}}$ and PH1B FFs which causes the computer to enter phase 1B.

3-245. PHASE 2. Phase 2 (the indirect phase) is entered from either phase 1A, phase 1B, or phase 2.

3-246. The conditions for entering phase 2 from phase 1A are: (1) the user instruction contained in the I-register is an indirect memory reference group instruction, and no interrupt ($\overline{\text{INT}}$ signal is false) or memory protect violation interrupt ($\overline{\text{IMPV}}$ signal is false) is present; or (2) the user instruction contained in the I-register is a JMP,I or JSB,I, and no memory protect violation interrupt is present.

3-247. The conditions for entering phase 2 from phase 1B are: the user instruction contained in the I-register is an indirect memory reference group instruction, and no memory protect violation interrupt is present.

3-248. The conditions for re-entering phase 2 are: (1) the user instruction contained in the I-register is a memory reference group instruction, the operand address entering Scratch Pad 1 is an Indirect reference (SB15 signal is true), and no interrupt is present (INT signal is false); or (2) the user instruction contained in the I-register is a JMP or JSB instruction, the operand address entering Scratch Pad 1 is an Indirect reference (SB15 signal is true), and the instruction being executed is not the third Indirect in a sequence (CT3 signal is false).

Table 3-3. Set Phase Logic Equations for the Phase Control Logic

$$
\begin{aligned}
SPH1A &= PH1A\ FF * EOP * LOOP \\
&= PH3\ FF * EOP * \overline{LOOP} * \overline{INT} \\
&= PH3\ FF * EOP * \overline{LOOP} * IR15 * \overline{IMPV} * (JMP + JSB) \\
\\
SPH1B &= PH1B\ FF * EOP * LOOP \\
&= RSSP * STEP\ GEN * (\overline{RH\ FF} * \overline{SIN\ FF} * \overline{SCY\ FF}) \\
&= PH2\ FF * EOP * \overline{LOOP} * INT * \overline{JMP} * \overline{JSB} \\
&= PH2\ FF * EOP * \overline{LOOP} * INT * (JMP + JSB) * SB15 * CT3 \\
&= PH3\ FF * EOP * \overline{LOOP} * INT * ((\overline{JMP} * \overline{JSB}) + (\overline{IR15} + IMPV)) \\
&= PH3\ FF * EOP * \overline{LOOP} * INT * (JMP + JSB) * (\overline{IR15} + IMPV) \\
&= PH3\ FF * EOP * \overline{LOOP} * INT * \overline{JMP} * \overline{JSB} \\
&= PH1A\ FF * EOP * \overline{LOOP} * INT * MRG * \overline{JMP} * ((\overline{JMP} * \overline{JSB}) + (\overline{IR15} + IMPV)) \\
\\
SPH2 &= PH2\ FF * EOP * LOOP \\
&= PH2\ FF * EOP * \overline{LOOP} * MRG * SB15 * \overline{CT3} * (JMP + JSB) \\
&= PH2\ FF * EOP * \overline{LOOP} * MRG * SB15 * \overline{INT} \\
&= PH1A\ FF * EOP * \overline{LOOP} * MRG * IR15 * \overline{INT} * \overline{IMPV} \\
&= PH1A\ FF * EOP * \overline{LOOP} * MRG * IR15 * \overline{IMPV} * (JMP + JSB) \\
&= PH1B\ FF * EOP * \overline{LOOP} * MRG * IR15 * \overline{IMPV} \\
\\
SPH3 &= PH3\ FF * EOP * LOOP \\
&= PH1A\ FF * EOP * \overline{LOOP} * (\overline{MRG} + \overline{INT} * (\overline{IR15} + IMPV) + JMP * (\overline{IR15} + IMPV)) \\
&= PH1B\ FF * EOP * \overline{LOOP} * (\overline{MRG} + \overline{IR15} + IMPV) \\
&= PH2\ FF * EOP * \overline{LOOP} * \overline{SB15} * (\overline{INT} + JMP + JSB)
\end{aligned}
$$

3-249. PHASE 3. Phase 3 (the execute phase) is entered from either phase 1A, phase 1B, or phase 2.

3-250. The conditions for entering phase 3 from phase 1A are: (1) the fetched instruction is not a memory reference group instruction; or (2) the fetched instruction is a JMP,I, and a memory protect violation interrupt is present; or (3) the fetched instruction is a direct memory reference group instruction, and no interrupt is present.

3-251. The conditions for entering phase 3 from phase 1B are: (1) the fetched instruction is not a memory reference group instruction; or (2) the fetched instruction is a direct memory reference group instruction; or (3) a memory protect violation interrupt is present.

3-252. The conditions for entering phase 3 from phase 2 are that the operand address entering Scratch Pad 1 is not an indirect reference (SB15 signal is false) and that: (1) no interrupt is present (INT signal is false), or (2) the instruction contained in the I-register is a JMP or JSB.

3-253. FORCING PHASE 1A. Phase 1A can be forced by direct-clearing all four phase control logic flip-flops. Any one of four conditions will force a phase 1A:

a. Pressing the INTERNAL PRESET switch on the operator panel with the computer in the halt mode.

b. Pressing the P switch on the operator panel with the computer in the halt mode.

c. Decoding a P1A microcode in the function field of the ROM microinstruction. (Used mainly for diagnostics.)

d. Applying power either as a result of initial power turn on, or when power is restored after a power fail. (Also see paragraph 3-252.)

3-254. Internal Preset. When the INTERNAL PRESET switch on the operator panel is pressed, the PRSI signal at pin 4 of card A1 becomes true approximately 5 milliseconds later and remains true until the switch is released. The signal is "anded" with $\overline{CLK3}$ to produce a pulse train in phase with $\overline{CLK3}$. The pulse train is applied to the direct-clear inputs of the four phase control flip-flops to set phase 1A. The resulting false SPH1B, SPH2, and SPH3 signals cause the ROM mapper to provide the starting address of the phase 1A microroutine to the ROM Address Register.

3-255. P Switch. Before the computer is placed in the run mode, the P-register is loaded with the starting address of the program to be run. Phase 1A is forced so that the first instruction in the program can be fetched from memory. When the P switch on the operator panel is pressed, the P1A signal at pin 81 of card A1 becomes true approximately 5 milliseconds later (see P switch timing diagram, figure 4-71). The P1A signal is "anded" with $\overline{CLK1}$ to direct-clear all phase control flip-flops, thereby forcing phase 1A.

3-256. Decoding P1A. When P1A is decoded by the function field decoder circuits, this also causes the P1A signal to become true, forcing the setting of phase 1A and clearing the current phase as described in the P switch discussion above.

3-257. Power On. When power is applied by the POWER switch, or when power is restored after a power fail, the true state of the Power On Normal (PON) signal lags restoration of dc operating power to the computer logic by approximately 25 milliseconds. The false PON signal generates a system reset in the same manner as the PRSI signal, and phase 1A is set as described in paragraph 3-248 above. However, if automatic restart mode is set (switch S1 on I/O Control Card A7 is in the ARS position), phase 1B is forced within two I/O cycles (1,960 nanoseconds) after phase 1A. (Refer to paragraph 3-252.)

3-258. FORCING PHASE 1B. Phase 1B is forced by an automatic restart. When power is restored after a power fail (and switch S1 on I/O Control Card A7 is in the ARS position), the PON signal forces a phase 1A which clears any flip-flop in the phase control logic which may have been randomly set during restoration of dc operating power. At the second time T2 following the true state of the PON signal, a pulse is applied to the direct-set inputs of the $\overline{PH1A}$ and PH1B FFs from the ROM control logic. This pulse clears the phase 1A forced by the PON signal and sets phase 1B.

3-259. PHASE 1 SKIP. If, during the execution of the microroutines for phase 1A and phase 1B, the instruction in the I-register is not a memory reference group instruction, the microinstruction that loads the operand address into Scratch Pad 1 must be skipped.

3-260. I-register bits 12 through 14 are examined by gate A1U37C to determine if the instruction is a memory reference group instruction. If the bits are false, the $\overline{MRG}$ signal line from A1U37C is true. The set output from the $\overline{PH1A}$ FF and the clear output from the PH1B FF are "nanded" and applied to gate A1U15C. If the computer is in phase 1A, or phase 1B, and the instruction is not a memory reference group instruction, the P1SK signal at pin 13 of card A1 is true. The true P1SK signal is applied to the skip field decoder circuits where it is "anded" with the decoded EOP microcode to clear the $\overline{SKIP}$ FF. At the end of the present clock period, the $\overline{SKIP}$ FF clears and the skip condition is set.

3-261. PHASE LOOP. The phase control logic can be forced to re-enter the same phase for test purposes. The phase switch A1S1 controls two gates at the output of each phase control flip-flop. When the EOP signal is true with the switch in the NORM position, the true output from the flip-flop corresponding to the existing phase is "anded" with the true EOP * $\overline{LOOP}$ signal line. The resulting true output allows the phase control logic gates to determine the next phase to be entered.

3-262. When the EOP signal is true with the switch in the LOOP positon, the true output from the flip-flop corresponding to the existing phase is "anded" with the true EOP * LOOP signal line. (The EOP * $\overline{LOOP}$ signal line is disabled.) The resulting true output causes the set phase signal line corresponding to the existing phase to become true, ensuring that the same phase flip-flop remains set at the end of the existing clock period.

3-263. INDIRECT COUNTER.

3-264. The indirect counter, located on I/O Buffer Card A8, consists of two flip-flops (2^0FF and 2^1FF) which count the number of indirect phases that are set, in succession, by the phase control logic. When three indirect phases are counted, the indirect counter applies a true CT3 signal to the phase control logic. The phase control logic uses the CT3 signal to allow processing of interrupts after three indirect phases by setting phase 1B.

3-265. The first indirect phase (phase 2) is entered either from phase 1A or phase 1B. When the first SPH2 signal becomes true, the indirect counter flip-flops remain set because the PH1A (or PH1B) signal is still true. (The PH1A and PH1B signals are "nored" by gate A8U56B and applied to the direct-set inputs to the flip-flops.)

3-266. When the second true SPH2 signal occurs, the 2^0FF clears. When the third true SPH2 signal occurs, the 2^1FF clears which applies a true CT3 signal to the phase control logic. If an interrupt is present, the phase control logic sets the interrupt fetch phase (phase 1B).

3-267. ROM MAPPER.

3-268. The ROM Mapper located on ROM Control Card A2 consists of gating circuits which decode the Instruction Register bits (4 through 15) and set phase signals (SPH1B, SPH2, and SPH3) to provide the ROM starting address to the ROM Address Register (RAR). It also provides the "jump to" address to the RAR during ROM jump conditions.

3-269. SET PHASE SIGNALS. The set phase signals from the phase control logic on Timing and Control Card A1 control the starting address applied to the RAR. When the normal fetch phase (phase 1A) is entered (SPH1B, SPH2, and SPH3 signals are false), address 0000 is applied to the RAR which is the starting address in ROM for the normal fetch phase. When the interrupt fetch phase (phase 1B) is entered (SPH1B is true, and SPH2 and SPH3 are false), address 0004 is applied to the RAR, which is the

starting address in ROM for the interrupt fetch phase. When the indirect phase (phase 2) is entered (SPH2 is true, and SPH1B and SPH3 are false), address 0014 is applied to the RAR, which is the starting address in ROM for the indirect phase. When the execute phase (phase 3) is entered (SPH3 is true, and SPH1B and SPH2 are false), a particular set of gates are enabled which allow the instruction register bit decoding circuits of the mapper to provide the starting address in ROM.

3-270. I-REGISTER BIT DECODING. The instruction register bit decoding circuits are divided into two groups. One group decodes IR9 through IR15 to determine whether the current instruction is a memory reference group, shift-rotate group, alter-skip group, input/output group, extended arithmetic group, or user macroinstruction. The appropriate output line (MRG+SRG, ASG, EAG, or MAC) from this group enables a set of gates in the other group which translates IR4 through IR9 into the ROM starting address. Table 4-8 lists the starting address corresponding to each user instruction in the basic instruction set.

3-271. ROM MODULE ADDRESSING. If additional ROM modules are installed to extend the user's instruction set, these modules are addressed by decoding the user macroinstructions and by jumps coded in the ROM microprogram. Jumpers A2W4 and A2W5, which are referred to as "MAC" jumpers, are used to address the lowest ROM module installed in the computer (other than module 0) when a user macroinstruction is decoded by the mapper. The jumper configurations corresponding to the ROM modules installed is given in table 3-5.

3-272. Access to the higher numbered ROM modules is provided by a jump table contained in the lowest numbered module installed (other than module 0). When a user macroinstruction is decoded by the mapper, the resulting address will be a location in the jump table. The ROM microinstruction contained in that location will be either a jump to within the ROM module or a jump to a higher numbered module, depending upon where the routine for executing the user macroinstruction is located.

3-273. ROM JUMPS. When a jump in the ROM microprogram is required, the true RJMP signal from the ROM control logic on Timing and Control Card A1 enables a set of gates in the mapper which allow the ROM instruction register bits to provide the next ROM address to the RAR. RIR bits 0 through 7, 12, and 17 provide the "jump to" address whenever CJMP, JMP, or JSB is coded in the function field of the ROM program. Bits 12 and 17 specify which module that the "jump to" address is contained (refer to table 3-4). Bits 0 through 7 specify the ROM address within the module.

3-274. S-bus bits 0 through 3 may be used to specify a portion of the jump address. The microprogram contained in module 0 of the basic 2100A Computer does not use this feature. However, the microprogram contained in a higher numbered module (if installed) may be assembled to use it. If the microinstruction containing the jump has ADR coded in the S-bus field, bits 0 through 9 of the Instruction Register will be read onto the S-bus. Of these 10 bits, only bits 0 through 3 are used in modifying the jump address.

Table 3-4. ROM Module Addressing

INPUT BITS TO RAR		ROM MODULE ADDRESSED	ROM ADDRESSES WITHIN EACH MODULE
BIT 9	BIT 8		
0	0	0	0000 to 0377
0	1	1	0400 to 0777
1	0	2	1000 to 1377
1	1	3	1400 to 1777

3-275. ROM ADDRESS REGISTER.

3-276. The ROM Address Register (RAR) is comprised of U32, U52, and U53 on ROM Control Card A2. The RAR receives its address inputs (bits 0 through 9) from the mapper or the Save Register. The RAR can be loaded, incremented, or cleared by control signals from the ROM control logic ($\overline{\text{SRAR}}$ and IRAR) and clock generator circuits (STCLK) on Timing and Control Card A1, and from the INTERNAL PRESET switch (RESET) on the operator panel.

3-277. LOADING THE RAR. The address data from the mapper is loaded into the RAR by a false $\overline{\text{SRAR}}$ signal from the ROM control logic and a false STCLK signal from the clock generator circuits. The $\overline{\text{SRAR}}$ signal will become false by any of the following conditions:

a. By pressing the P switch on the operator panel.

b. By an EOP microcode detected in the skip field.

c. By a JMP or JSB microcode detected in the function field, with no previous skip condition.

d. By a RSB microode (return from ROM subroutine) detected in the function field. (Address data is provided by the Save Register.)

e. By a CJMP microcode detected in the function field when the computer enters the halt mode, or when an interrupt is generated.

f. By an auto-restart pulse from the auto-restart logic.

3-278. INCREMENTING THE RAR. The RAR is incremented by a true IRAR signal from the ROM control logic and a false STCLK signal from the clock generator circuits. Incrementing the RAR provides the consecutive addresses to ROM that are necessary to execute the user instruction after the starting address is set by the mapper. The IRAR signal is true when the SRIR signal is true (refer to paragraph 3-322), the RUN FF in the run logic on Timing and Control Card A1 is set, and there is no CJMP detected in the function field when operating the computer in the

single-cycle mode. If CJMP is detected during the single-cycle mode, the run logic will cause the computer to halt two clock periods after the detection of CJMP. The ROM control logic on Timing and Control Card A1 inhibits the ROM, which enters a NOP (all "1's") in the ROM Instruction Register at the end of the present clock period, and inhibits the IRAR signal, which prevents incrementing the RAR, thereby holding the address containing the CJMP microcode in the RAR while the computer enters the halt mode.

3-279. CLEARING THE RAR. The RAR is cleared by a false $\overline{\text{RESET}}$ signal. The RESET signal applied to ROM Control Card A2 is generated on Timing and Control Card A1 by a false PON signal (during power turn-on) or a true PRSI signal from the operator panel or controller panel (pressing the INTERNAL PRESET or PRESET switch, as applicable).

3-280. END-OF-PHASE LOGIC.

3-281. The end-of-phase logic, located on the ROM Control Card A2, consists of the Nonexistent ROM FF (NER FF), the Legal Entry Point FF (LEP FF), and their associated circuits. These circuits generate the EOP and SKIP signals. The EOP signal is generated whenever an EOP microcode is decoded in the skip field or whenever a nonexistent ROM module is addressed. The skip signal is generated whenever an illegal entry point is addressed during the execution of a user macroinstruction (an extended arithmetic group instruction, for example). The function of these circuits is explained in the following paragraphs.

3-282. NER FF. The NER FF monitors the ROM Address register bits 8 and 9 (RAR8 and RAR9) through jumpers A2W1 through A2W3 and A2W6. If a nonexistent ROM module is addressed, the enable inputs (CS1, CS2) to the ROM packs is high, thereby disabling the ROM. At the same time, a high is present to the set side input of the NER FF. At the end of the present clock period, the NER FF sets, and a NOP microinstruction is clocked into the RIR. The NOP microcode in the skip field provides high inputs (RIR0, RIR2, and RIR3) to "and" gate U57B. The remaining high input to U57B is provided by the inverted clear side output from the NER FF. The high output from U57B is "anded" with the Enable End Of Phase (EEOP) signal from Microinstruction Decoder 1 card A3 to produce the End Of Phase (EOP) signal. The EOP signal is applied to the phase control logic on Timing and Control card A1 to set the next phase.

3-283. Proper functioning of the NER FF depends on jumpers A2W1 through A2W6 being properly installed for the number of ROM modules within the computer. Table 3-5 lists the proper jumper installation for each possible ROM module configuration.

3-284. LEP FF. The Legal Entry Point (LEP) FF circuits monitor the ROM Instruction Register bits used as legal entry points for user macroinstructions. As long as the LEP FF remains in the set condition, either via the input circuits A2U57B, A2U86A, A2U87C, and A2U87D or circuits A2U85F, A2U57A, A2U86C, A2U87B, and A2U87D, the reset side of the FF will remain false and the SKIP signal will remain false. But, if the output of gate A2U81D becomes true, clearing the LEP FF, the SKIP signal will become true, causing the next microinstruction to be skipped. The next microinstruction is loaded into the RIR, but it is not executed. The true SKIP signal disables the function, store, special, and skip fields except for ROM jump conditions (JMPF signal) and function generator control in the function field. This skip condition will continue to be generated until a legal entry point (LEP microcode in the special field) or an end-of-phase (EOP microcode in the skip field) is reached in the microprogram, at which time the microprogram continues or an end-of-phase is processed and the next program instruction is fetched and executed.

Table 3-5. ROM Control Card A2 Jumper Connections for Various Module Configurations

MODULES	JUMPERS TO BE INSTALLED					
	W1	W2	W3	W4	W5	W6
0	A to B	D to K	E to F	in	none	H to L
0, 1	A to B	none	none	in	none	H to L
0, 2	none	D to K	E to F	none	in	none
0, 3	A to B	C to D	E to F	in	in	G to H
0, 1, 2	A to D	none	E to F	in	none	none
0, 1, 3	A to B	none	none	in	none	G to H
0, 2, 3	none	C to D	E to F	none	in	none
0, 1, 2, 3	none	none	none	in	none	none

3-285. SAVE REGISTER.

3-286. The Save Register located on ROM Control Card A2 consists of ten FFs which store the return address while the contents of the ROM subroutine addresses are being executed. The timing associated with the ROM JSB operation is shown in figure 3-20.

3-287. Normally the Save Register contains the ROM address present at the output of the ROM Address Register (RAR). Clocking the Save Register is caused by "anding" the STCLK signal with the JSB signal from the function field decoder circuits located on Microinstruction Decoder 2 Card A4. Each time the STCLK signal is true, the contents of the RAR are stored into the Save Register. However, when a JSB microcode is detected by the function field decoding circuits, clocking of the Save Register is inhibited. This latches the next sequential address in the ROM program into the Save Register which is the return address from the ROM subroutine.

3-288. Detection of JSB in the function field causes a false ENRM signal from the ROM control circuits, which disables the ROM. Disabling ROM causes all "1's" (a NOP) to be applied to the ROM Instruction Register (RIR). The detection of JSB also causes the $\overline{SRAR}$ signal from the ROM control logic to be false, enabling the parallel load function of the RAR.

3-289. At the end of the next clock period, the $\overline{JSB}$ FF in the function field decoding circuits is cleared which applies a false $\overline{JSB}$ signal to the Save Register clock circuits. At this point, the Save Register clock goes false, locking the address present at the output of the RAR in the Save Register. This is the address immediately following the address of the microinstruction containing the JSB microcode. The Save Register clock remains inhibited until the $\overline{JSB}$ FF is set.

3-290. At the end of execution of the ROM subroutine, an RSB microcode will be detected by the function field decoding circuits. The detection of RSB causes a true RSAV signal to be applied to the Save Register output gates which gates the contents of the register to the parallel input lines to the RAR. The true RSAV is also applied to the ROM control circuits which causes the $\overline{SRAR}$ and ENRM signals to be false. The false ENRM signal disables the ROM which applies all "1's" (a NOP) to the RIR. The false $\overline{SRAR}$ signal enables the parallel input function of the RAR.

3-291. At the end of the present clock period, the return address is clocked into the RAR, the NOP is clocked into the RIR, and the $\overline{JSB}$ FF is set. With the $\overline{JSB}$ signal true, clocking of the Save Register resumes until another JSB microcode is detected by the function field decoding circuits.

3-292. ROM.

3-293. The ROM contains the microinstructions necessary to execute the user instruction set. The 2100A Computer can contain up to four ROM modules, each comprised of 256 microinstructions. The basic instruction set (see figure 4-1) is executable by the ROM microprogram contained in module 0. A listing of this microprogram is contained in table 4-9. Any combination of modules 1, 2, and 3 may be installed in the computer to extend the user's instruction set through the use of macroinstructions. However, the basic 2100A Computer contains only module 0.

3-294. Six integrated circuit packs make up a ROM module. The ROM packs associated with each module and their respective locations are given in table 3-6.

3-295. Each ROM pack contains 256 locations of four bits each. The six ROM packs associated with each module provide 256 locations of 24-bit microinstruction words. The word contained in any location is addressed by the ROM address register bits. The word in the addressed location is present on the output lines when the enable inputs (CS1 and CS2) to the ROM packs are false. If the enable inputs are true, all "1's" (a NOP) will be present on the output lines. Bits 8 and 9 of the RAR and the ENRM signal determine which module will be enabled.

Table 3-6. ROM Module Locations

ROM MODULE	CIRCUIT CARD	REFERENCE DESIGNATIONS
0	ROM Control card A2	U15, U16, U17, U45, U47, and U55
1	ROM Control card A2	U25, U26, U27, U35, U37, and U65
2	Timing and Control card A1	U12, U22, U32, U42, U52, and U62
3	Timing and Control card A1	U11, U21, U31, U41, U51, and U61

3-296. When the ENRM signal from the ROM control logic circuits on Timing and Control Card A1 is true, bits 8 and 9 of the RAR enable the six ROM packs associated with the addressed module. The ENRM signal is true when the computer is in the RUN mode and no jump condition is present (i.e., CJMP, JMP, JSB, or RSB is not coded in the function field of the microinstruction present in the ROM instruction register).

3-297. If a jump condition is present, the ROM is inhibited to prevent the contents of the next sequential address in the ROM program, which is present in the RAR, from being executed. The next address to be executed following the jump condition should be the jump target.

3-298. THE ROM MICROPROGRAM.

3-299. A listing of the ROM microprogram contained in module 0 of the basic 2100A Computer is given in table 4-9. The discussion that follows is a definition of terms used to describe the program, and some of the basic considerations to help analyze the program.

3-300. MICROCODE. The term "microcode" refers to the specific coding in each field of the microinstruction. Bit coding and descriptions of each microcode is given in table 4-6 and 4-7, respectively, in the troubleshooting section.

3-301. MICROINSTRUCTION. The term "microinstruction" refers to the 24-bit word stored at a particular ROM address. The microinstruction is made up of appropriate microcodes in each field to perform a particular operation.

3-302. MICROROUTINE. The term "microroutine" refers to a group of microinstructions required to execute a phase operation or user instruction. Some microroutines consist only of one group of consecutive ROM addresses; others consist of different groups of consecutive ROM addresses. For example, the microroutine for phase 1A is stored at consecutive ROM addresses 0000 through 0002; while the microroutine for the MPY instruction consists of ROM addresses 0210 through 0213, 0362 through 0370, 0232 through 0235, and 0155 through 0163.

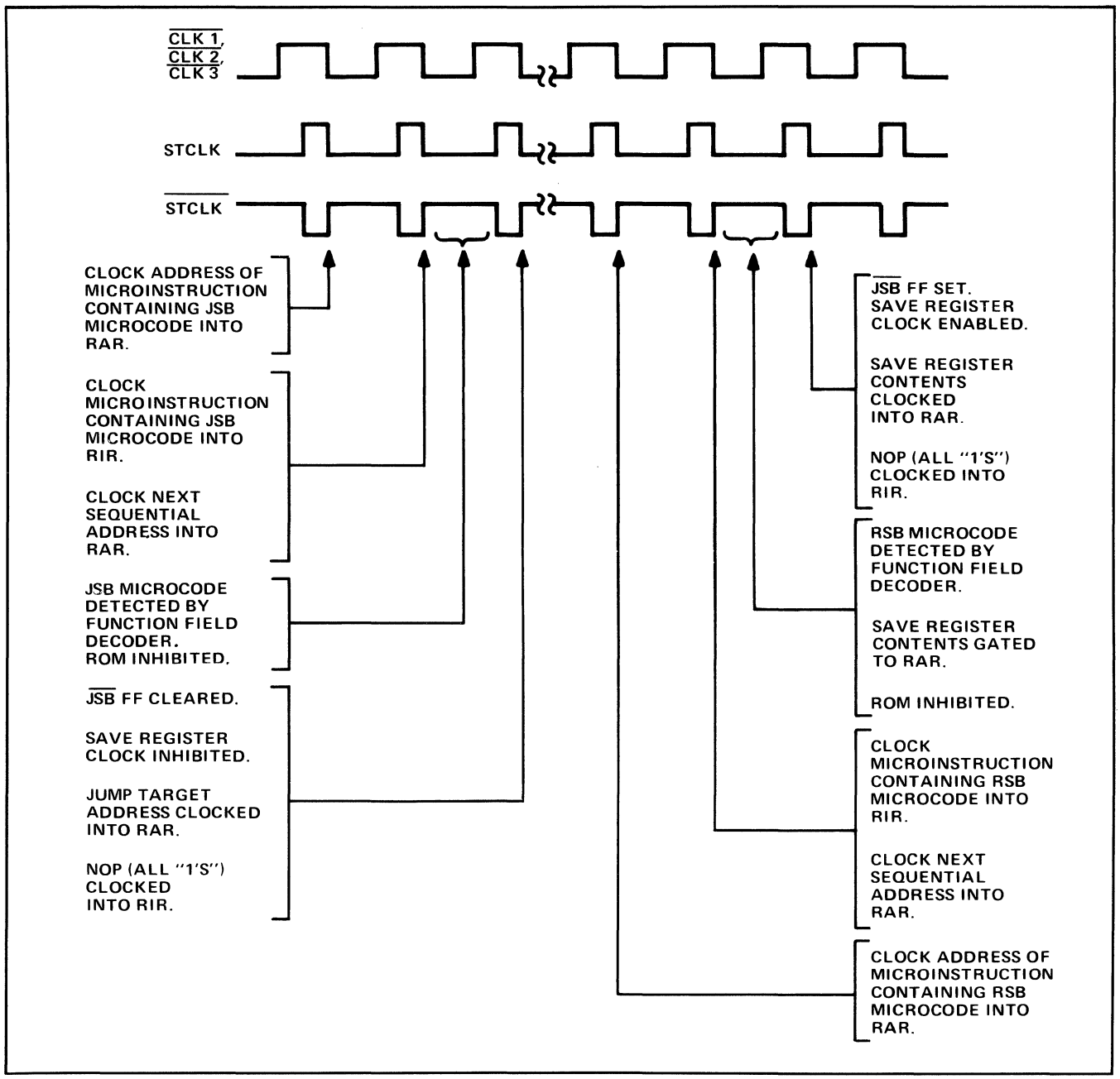


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Figure 3-20. ROM JSB Operation

3-303. SUBROUTINE. The term "subroutine" refers to a group of microinstructions used by more than one microroutine. Usually the subroutine is called by a JSB microcode in the function field. However, the PDEC subroutine at ROM addresses 0011 and 0012 is called by a JMP microcode. This is necessary since the PDEC subroutine call occurs at the end of the calling microroutine and it is not necessary to return to the calling microroutine.

3-304. ENTRY POINT LABELS. The entry point in the ROM microprogram, as directed by the ROM mapper, are labeled by function. For example, the entry point for phase 1A is PH1A, the entry point for the OTA/B instruction is OT*, the entry point for the decrement P-register subroutine is labeled PDEC, etc.

3-305. LEGAL ENTRY POINTS. At various points in the microprogram, LEP is coded in the special field. Should the mapper provide the wrong address to the RAR (as a result of an incorrectly coded user macroinstruction), the RAR is incremented, and the LEP FF circuits on ROM Control Card A2 cause a skip condition which does not allow any microinstruction to be fully executed until the LEP microcode, or an EOP microcode in the skip field, is detected.

3-306. END-OF-PHASE. The next-to-last microinstruction in any microroutine contains an EOP microcode in the skip field. This microcode allows the following microinstruction to be executed, then directs the phase control logic to set the next phase. The EOP microcode is detected also during skip conditions. The EOP microcode also does not allow the run logic to direct the computer into the halt mode until one clock period after EOP is detected.

3-307. ROM SKIP MODE. The term "skip", as used with the ROM microprogram, is unconventional in that, if a skip condition is detected, the following instruction is not "jumped over". Instead, the "skipped" microinstruction is actually forced to be a NOP (except for EOP). Normally ROM skips are caused by the microcodes contained in the skip field of the microinstruction (except for EOP, ICTR, RPT, and NOP). The skip condition causes the store, special, skip, and function field decoder circuits (except for function generator control) to be disabled. The "skipped" microinstruction is clocked into the RIR, but its full execution is inhibited.

3-308. There are two special cases which also cause a ROM skip, and these are caused by having a user instruction, other than a memory reference group, in the I-register while either phase 1A, or phase 1B, is set.

3-309. ROM JUMP MODE. ROM jumps are caused by JMP, JSB, RSB, and CJMP microcodes present in the function field. The jump target is indicated in the ROM program listing by entry point label appearing in special field column instead of a microcode. Bits 0 through 7 form the jump target address, therefore the special and skip field decoder circuits are inhibited. Also bits 12 and 17 are used for ROM module addressing. Since bit 17 occurs in the S-bus field, and the remaining three bits in the S-bus field are "1's", the P microcode execution is inhibited.

3-310. ROM jumps require two machine cycles to execute. The microinstruction containing the jump is executed during the first cycle, and a NOP is executed in the second cycle. The second cycle is used to allow data to be accessed from the new address.

3-311. ROM REPEAT MODE. The repeat mode is entered when the RPT microcode is detected in the skip field. Incrementing the RAR is inhibited, thereby holding the address of the microinstruction following the one containing the RPT microcode in the RAR. The clock to the RIR is inhibited so that the RIR contents do not change and the microinstruction is executed repeatedly until the skip condition specified in the skip field is met. When the skip condition is met, the RAR is incremented to the next address, and the repeated microinstruction is "skipped" (a NOP is executed).

3-312. SYNCHRONIZING WITH I/O TIME PERIODS. Whenever a RW or CW microcode appears in the special field of a microinstruction, that microinstruction is not executed until I/O time T6. This synchronizes memory timing to be compatible with input/output data transfers. The next microinstruction will be executed at time T2, etc.

3-313. Whenever an IOG1 microcode appears in the special field of a microinstruction, that microinstruction is not executed until I/O time T2. The following microinstruction will be executed at time T3, etc. (The IOG1 microcode appears in the first microinstruction of any of the I/O group microroutines.)

3-314. ROM CONTROL LOGIC.

3-315. The ROM control logic consists of gates located on Timing and Control Card A1. The function of the ROM control logic is to control the operation of the mapper, ROM Address Register (RAR), and ROM.

3-316. ROM JUMP CONTROL. When a ROM jump is required by the ROM program, the ROM control logic enables the ROM mapper to provide the jump target address to the RAR, enables the parallel input function of the RAR, and disables the ROM.

3-317. ROM jumps are sensed by the $\overline{\text{JMPS}}$ and $\overline{\text{CJMP}}$ signals provided to the ROM control logic by Microinstruction Decoder 2 Card A4. Whenever a JMP or JSB microcode is detected by the function field decoding circuits, and there is no previous skip condition, the $\overline{\text{JMPS}}$ signal becomes false. This causes the ROM control logic to provide a true RJMP signal to the mapper, a false $\overline{\text{SRAR}}$ signal to the RAR, and a false ENRM signal to the ROM.

3-318. Whenever a $\overline{\text{CJMP}}$ microcode is detected by the function field decoding circuits, the CJMP signal becomes false. If an interrupt is present (INT signal is true from the I/O Control Card A7), or a panel halt is detected (RH FF, SIN FF, and SCY FF in the RUN logic are cleared), the ROM control logic provides a true RJMP signal to the mapper, a false $\overline{\text{SRAR}}$ signal to the RAR, and a false ENRM signal to the ROM.

3-319. During the single cycle mode, detection of a CJMP microcode will cause the ROM control logic to provide a false ENRM signal to disable the ROM and a false IRAR signal to prevent incrementing the RAR. This is accomplished by the "or-tie" of buffers A1U33C and A1U33D. The ROM control logic also provides a true input to gate A1U65B to clear the SCY FF in the RUN logic. This will cause the computer to halt before an End of Phase (EOP) is detected.

3-320. RETURN FROM ROM SUBROUTINES. Returns from ROM subroutines are detected by an RSB microcode in the function field of the ROM microprogram. Whenever the RSB microcode is detected, the RSAV signal applied to the ROM control logic becomes true. This causes the ROM control logic to provide a false SRAR signal to enable the parallel load function of the RAR, and a false ENRM signal to disable the ROM.

3-321. END-OF-PHASE. When an EOP microcode is detected in the skip field of the ROM microprogram, the EOP signal from the end of phase logic on ROM Control Card A2 becomes true. The SRAR signal from the ROM control logic becomes false which enables the parallel load function of the RAR.

3-322. HALT MODE. The halt mode is detected by the ROM control logic by monitoring the set output from the RUN FF in the RUN logic. When the computer is in the halt mode, the RUN FF is cleared. This causes the ENRM and IRAR signals from the ROM control logic to be false, thereby disabling the ROM and preventing the RAR from incrementing.

3-323. AUTOMATIC RESTART. When power is resumed after a power fail and switch S1 on I/O Control Card A7 is in the ARS (automatic restart) position, the RSSP signal from the automatic restart logic on card A7 becomes true. During the next clock period, the step generator output becomes true. The RSSP signal, step generator output, and the clear outputs from the RH FF, SIN FF, and SCY FF, are "nanded" by gate A1U95B. The false output from A1U95B causes a false SRAR which enables the parallel input function of the RAR. Simultaneously, the false output from A1U95B direct-sets the $\overline{\text{PH1A}}$ FF and PH1B FF in the phase control logic and provides a SPH1B signal to the ROM mapper.

3-324. ROM INSTRUCTION REGISTER.

3-325. The 24-bit ROM Instruction Register (RIR) stores the contents of the ROM location addressed by the ROM Address Register (RAR) and provides the RIR bits to the field decoders. The six fields of the RIR are divided among three cards. The special and skip field decoders are located on ROM Control Card A2, the S-bus and store field decoders are located on Microinstruction Decoder 1 Card A3, and the R-bus and function field decoders are located on Microinstruction Decoder 2 Card A4.

3-326. INPUTS. The RIR receives its inputs from the contents of the addressed ROM location. However, during ROM jumps, jump-to-subroutines, and return-from-subroutines, ROM is inhibited for one clock period which supplies all "1's" (a NOP) to the RIR. ROM skips are accomplished by reading the microinstruction to be skipped into the RIR while disabling the function (except for function generator control to card A5), store, special, and skip fields.

3-327. CLOCKING. Normally, the RIR is clocked at the end of every clock period. However, if the repeat mode is set, the RIR clock is inhibited until a skip condition is met. This causes the microinstruction following the one that set the repeat mode to be executed a specified number of times. When the skip condition is met, the repeated microinstruction is skipped.

3-328. The RIR is clocked by "nanding" the SRIR signal from the skip field decoder circuits, on Instruction Register Decoder Card A6, with $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, or STCLK, depending upon which field is being clocked. The SRIR signal is true unless the $\overline{\text{REPEAT}}$ FF in the skip field decoder circuits is cleared (repeat mode is set). (Figure 3-21 shows the circuit operation during the repeat mode.) Clearing the $\overline{\text{REPEAT}}$ FF is accomplished by the RPT microcode in the skip field. The $\overline{\text{REPEAT}}$ FF is cleared at the end of the clock period after the RPT microcode is detected in the skip field. The RPT microcode is used with shifts, rotates, multiply, and divide instructions in the Extended Arithmetic Group.

3-329. The skip condition is determined by the contents of the Repeat Counter on card A6. When the Repeat Counter contains all "1's" (ignoring bit 4), a carry bit is generated which is tested by the CTRI microcode in the skip field. (This same microcode is also used to increment the counter during the repeat mode.) The carry bit and the CTRI signal cause a true skip condition to the set side of the $\overline{\text{REPEAT}}$ FF and to the clear side of the $\overline{\text{SKIP}}$ FF. The true skip condition also causes the SRIR signal to become true. At the end of the present clock period, the $\overline{\text{REPEAT}}$ FF sets, the next microinstruction is clocked into the RIR, and the RAR is incremented.

3-330. OUTPUT DESTINATIONS. The RIR output of each field is applied directly to corresponding field decoder circuits. RIR bits 0 through 7, 12, and 17 are also applied to the ROM mapper for addressing purposes during ROM jump operations (refer to paragraph 3-267). RIR bits 0 through 7 are also applied to the end-of-phase logic for decoding Legal Entry Points (LEP) and End-of-Phase (EOP). (Refer to paragraph 3-274.)

3-331. INSTRUCTION REGISTER.

3-332. The Instruction (I-) Register, located on Instruction Register Decoder Card A6, consists of 15 flip-flops (IR0 FF through IR15 FF) which store the user instruction fetched during phase 1A or phase 1B.

3-333. CLOCKING. The I-register is clocked by decoding IR in the store field which causes a true STI signal to be applied to pin 30 of card A6. The STI signal is "anded" with $\overline{\text{CLK2}}$ to load the data contained on the S-bus during the last half of the clock period. The IR microcode is present in the store field of the microroutines for phase 1A and phase 1B.

3-334. S-BUS DATA. The data contained on the S-bus when the I-register is clocked is determined by the microcode present in the S-bus field of the microinstruction that contains the IR microcode. COND is present in the S-bus field of the phase 1A and phase 1B microroutines. The COND microcode is used with AAB in the R-bus field to read either the A-, B-, or T-register onto the S-bus.

3-335. FUNCTION OF I-REGISTER BITS. Certain I-register bits are routed to various logic circuits throughout the computer to perform particular functions. The destinations of the IR bits and a brief description of their functions are given below:

a. Special Field Decoder. I-register bits 0 through 9, and 12 through 14 are applied to the special field decoder circuits on card A6 to decode alter-skip and shift-rotate group instructions.

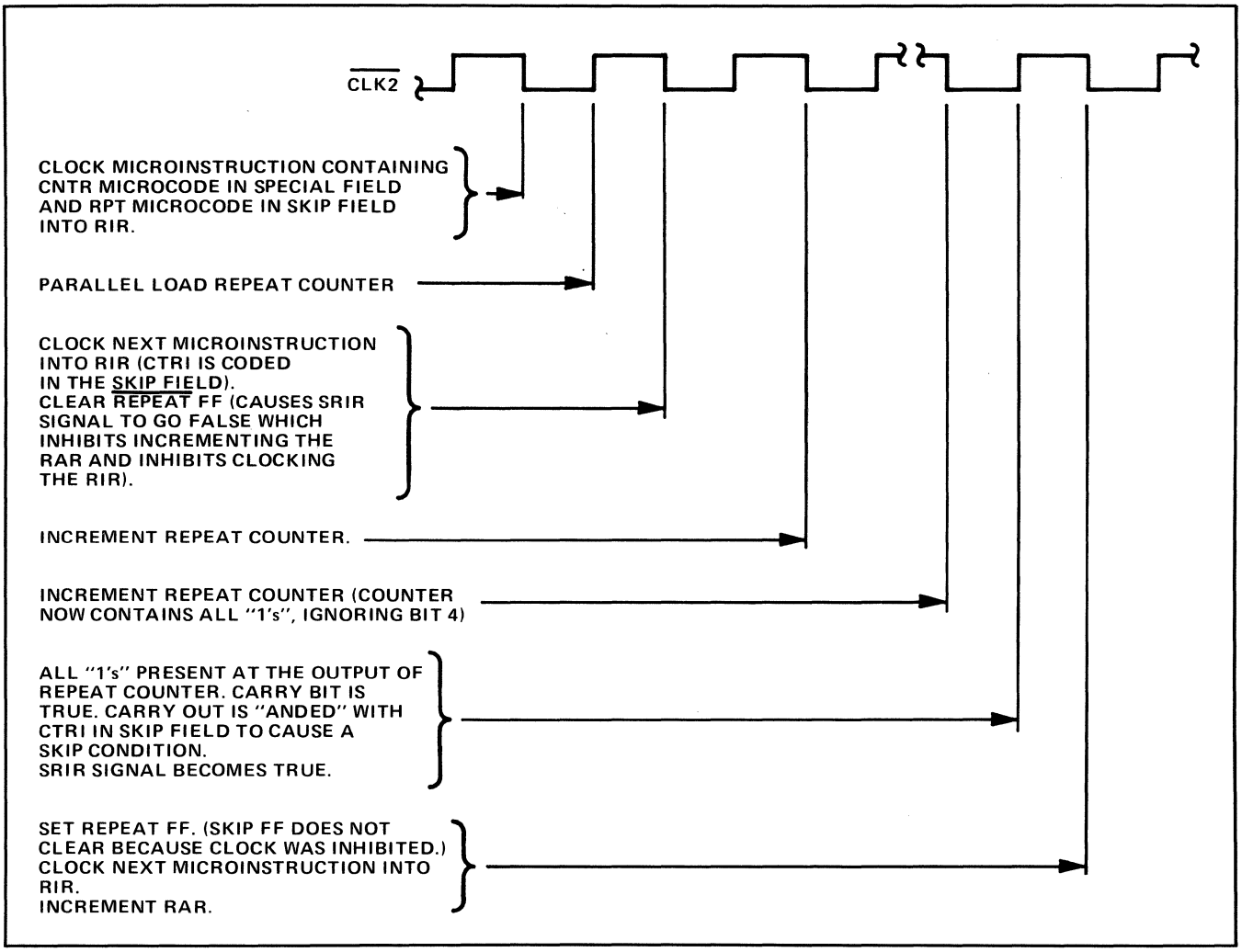

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Figure 3-21. Repeat Mode Operation

b. ROM Mapper. I-register bits 4 through 15 are applied to the ROM mapper on ROM Control Card A2 to determine the starting address of the appropriate microroutine in ROM for executing the instruction.

c. S-Bus Field Decoder. I-register bits 0 through 9 are applied to the S-bus gating circuits on ROM Control Card A2 for providing an operand address when ADR is coded in the S-bus field. Also, I-register bit 10 (the Z/C bit in the memory reference instruction) is applied to the S-bus field decoder circuits on Microinstruction Decoder 1 Card A3. Bit 10 is used for reading P-register bits 10 through 15 onto the S-bus (IR10 a "1") which provides a full operand address, or "0's" onto S-bus bits 10 through 15 (IR10 a "0"), when ADR is coded in the S-bus field.

d. Phase Control Logic. I-register bits 11 through 15 are applied to the phase control logic on Timing and Control Card A1 for detecting MRG (memory reference group instructions), JMP, JSB, and Indirect conditions.

e. Store Field Decoder. I-register bit 11 is applied to the store field decoder logic on Microinstruction Decoder 1 Card A3 to determine if the A-register (IR11 a "0"), or the B-register (IR11 a "1"), will be stored with the contents of the T-bus when CAB is coded in the store field.

f. R-Bus Field Decoder. I-register bits 9 and 11 are applied to the R-bus field decoder logic on Microinstruction Decoder 2 Card A4. If bit 9 is a "1", the Index Mode (INM) FF is set, and CQ is coded in the R-bus field, the Q-register will be read onto the R-bus (this is used only for diagnostic purposes). Bit 11 determines if the A-register (IR11 a "0"), or the B-register (IR11 a "1"), will be read onto the R-bus when CAB is coded in the R-bus field.

g. Select Code Encoder. I-register bits 0 through 5 are applied to the I/O select code encoder circuits on I/O Control Card A7 for generating select code most (SCM) and select code least (SCL) signals during execution of input/output group instructions.

h. I/O Group Decoder. I-register bits 6 through 9, and 11 are applied to the I/O group decoder logic on I/O Buffer Card A8 to decode input/output group instructions.

3-336. ROM MICROINSTRUCTION DECODER.

3-337. The ROM microinstruction decoder is divided into six sections; one for each field of a microinstruction. The six field decoders are designated and located as follows:

a. R-Bus Field Decoder. Microinstruction Decoder 2 Card A4.

b. S-Bus Field Decoder. Microinstruction Decoder 1 Card A3.

c. Function Field Decoder. Microinstruction Decoder 2 Card A4.

d. Store Field Decoder. Microinstruction Decoder 1 Card A3.

e. Special Field Decoder. Instruction Register Decoder Card A6.

f. Skip Field Decoder. Instruction Register Decoder Card A6.

3-338. R-BUS FIELD DECODER. The R-Bus Field Decoder monitors ROM Instruction Register bits 21, 22, and 23 and provides $\overline{RBE}$, RBS1, and RBS2 signals to control the source of data on the computer R-bus (refer to table 3-7). The "not" R-Bus Enable signal ($\overline{RBE}$) performs the enable/disable function of the R-bus multiplexer located on Arithmetic/Logic Card A5. If $\overline{RBE}$ is true, the multiplexer is disabled and the R-bus contains all zeros. Signals RBS1 and RBS2 (R-Bus Select 1 and 2) form a 2-bit code that controls the output of the multiplexer. Table 3-7 shows this code and the resulting multiplexer output. When the computer operator panel is active, a true CPEN signal disables the output of the R-Bus Decoder. The operator panel then supplies the control signals to the R-bus multiplexer as needed. Operation of the R-Bus Decoder for each of the R-bus field microcodes is described in the following paragraphs.

3-339. A (000). The microcode A in the R-bus field causes the R-bus multiplexer to unconditionally transfer the A-register content to the R-bus.

3-340. AAB (101). The microcode AAB in the R-bus field considers the A- and B-addressable logic. If the B-addressable logic is set (BAFF = logic 1), the B-register content is put on the R-bus, otherwise the A-register content is put on the R-bus. This microcode is frequently used in conjunction with the microcode COND in the S-bus field. In this case, if neither the A- or B-addressable logic is set, signal $\overline{RBE}$ becomes true and the R-bus becomes all zeros.

3-341. B (001). The microcode B in the R-bus field causes the R-bus multiplexer to unconditionally transfer the B-register content to the R-bus.

3-342. CAB (100). The microcode CAB in the R-bus field selects the A- or B-register as directed by bit 11 of the I-register. If bit 11 of the I-register is a logic 0, the A-register content is put on the R-bus. If bit 11 is a logic 1, the B-register content is put on the R-bus.

3-343. CQ (110). The microcode CQ in the R-bus field will result in the Q-register content being placed on the R-bus if the Index Mode (INM) FF is set and I-register bit 9 is a logic 1. Otherwise the R-bus will be all zeros. This microcode is not presently used by the computer microprogram and is listed here for reference purposes only.

3-344. F (011). The microcode F in the R-bus field causes the R-bus multiplexer to unconditionally transfer the F-register contents to the R-bus.

Table 3-7. R-Bus Field Microcode Processing

MICRO CODE	RIR BITS CONFIGURATION			R-BUS MULTIPLEXER CONTROL SIGNALS CONFIGURATION			OTHER SIGNAL CONSIDERATIONS	R-BUS MULTIPLEXER OUTPUT
	RIR23	RIR22	RIR21	RBE	RBS1	RBS2		
A	0	0	0	0	0	0	–	A-register
B	0	0	1	0	1	1	–	B-register
Q	0	1	0	0	0	1	–	Q-register
F	0	1	1	0	1	1	–	F-register
CAB	1	0	0	1	0	0	IR11	A- or B-register
AAB	1	0	1	1	1	0	BAFF, COND	A- or B-register, or all zeros
CQ	1	1	0	1	0	1	INM, IR9	Q-register, or all zeros
NOP	1	1	1	1	1	1	–	All zeros

3-345. NOP (111). The microcode NOP in the R-bus field causes the R-bus to remain all zeros during the execution of the microinstruction.

3-346. Q (010). The microcode Q in the R-bus field causes the R-bus multiplexer to unconditionally transfer the Q-register content to the R-bus.

3-347. S-BUS FIELD DECODER. The S-Bus Field Decoder monitors ROM Instruction Register (RIR) bits 17, 18, 19, and 20 and provides signals to control the source of data on the computer S-bus (refer to table 3-8). The S-bus decoder consists primarily of two binary-to-octal decoders, A3U25 and A3U26. RIR bit 20 selects one of the two decoders and RIR 17, 18, and 19 provide the 2^0, 2^1, and 2^2 inputs respectively to the decoders. An additional enable input to the decoders carries the "or" function of signals PEX (Parity Error) and PH5 (phase 5) both of which must be false to allow an S-bus microcode to be decoded. When active, the operator panel supplies the S-bus control signals as needed. Operation of the S-Bus Field Decoder for each of the S-bus field microcodes is given in the following paragraphs.

3-348. ADR (0110). The microcode ADR in the S-bus field results in the full operand address of the current instruction (memory reference only) being placed on the S-bus. Under most conditions, this is accomplished with a true ADR signal which gates I-register bits 0 through 9 to the S-bus and, if current page addressing is specified (IR10 = 1), a true RPHI signal which gates P-register bits 10 through 15 to the S-bus. If zero page addressing is specified (IR10 = 0), the RPHI signal is inhibited and bits 10 through 15 of the S-bus become zeros. The INM signal input to the S-bus decoder is not used in the present configuration of the 2100A Computer and must be false for proper operation of the ADR microcode. When fetching the contents of a trap cell as in a phase 1B operation, P-register bits 10 through 15 do not necessarily reflect the page address of the instruction. To prevent an erroneous operand address, the S-bus decoded CIR microcode (part of the first phase 1B microinstruction) sets flip-flop A3U55A which prevents generation of a true RPHI signal for the duration of the phase 1B operation. Since all trap cells are on zero page, the correct operand address is placed on the S-bus.

3-349. CIR (0000). The microcode CIR in the S-bus field results in the contents of the Central Interrupt Register (CIR) being read to the S-bus. This is accomplished with a true RCIR (Read Central Interrupt Register) signal sent to I/O Control Card A7. In addition, the true CIR output of decoder A3U25 sets flip-flop A3U55A as described in paragraph 3-342.

3-350. CL (1101). The microcode CL in the S-bus field results in a constant being read to the left half of the S-bus (bits 8 through 15). The constant is obtained from bits 0 through 7 of the ROM Instruction Register (normally special and skip fields of a microinstruction) by a true CL signal from the S-bus decoder to ROM Control Card A2. Gates A3U21A,C,D, and A3U11B recognize the CL code and provide a false ENSS signal to disable the special and skip fields of the microinstruction decoder.

Table 3-8. S-Bus Field Microcode Processing

MICRO CODE	OCTAL CODE	RIR BITS 20	19	18	17	DECODER USED	OUTPUT SIGNAL GENERATED	SOURCE OF DATA READ ONTO S-BUS*
CIR	00	0	0	0	0			Central Interrupt Register
IOI	01	0	0	0	1		RIOB	I/O Bus
T	02	0	0	1	0		SELT, READ, (CPU freeze)	T-register
M	03	0	0	1	1		READ	M-register
RRS	04	0	1	0	0	U25	RRSB	R-Bus
CNTR	05	0	1	0	1		RCTR	Repeat Counter
ADR	06	0	1	1	0		ADR	I- and P-registers
COND	07	0	1	1	1		COND	A-, B-, or T-register
S4	10	1	0	0	0		RSP4	Scratch Pad 4
S3	11	1	0	0	1		RSP3	Scratch Pad 3
S2	12	1	0	1	0		RSP2	Scratch Pad 2
S1	13	1	0	1	1	U26	RSP1	Scratch Pad 1
CR	14	1	1	0	0		CR	ROM Instruction Register
CL	15	1	1	0	1		CL	ROM Instruction Register
P	16	1	1	1	0		RPL0, RP9, RPH1	P-register
NOP	17	1	1	1	1		—	—

* Refer to text for specific bits read onto the S-bus.

3-351. CNTR (0101). The microcode CNTR in the S-bus field results in the content of the Repeat Counter, located on Instruction Register Decoder Card A6, to be read onto the S-bus bits 0 through 4. All other S-bus bits are zeros. This is accomplished by a true RCTR signal from the S-bus Decoder to Instruction Register Decoder Card A6.

3-352. COND (0111). The microcode COND in the S-bus field results in either the T-register content or the R-bus data being read onto the S-bus. If the A- or B-addressable logic is set as indicated by true AAFF or BAFF signals, a true RRSB signal is sent to Arithmetic/Logic Card A5 to transfer the R-bus data to the S-bus. If the A- or B-addressable logic is not set (signal $\overline{\text{ABF}}$ is true), true SELT and READ signals are sent to Memory Data Control Card A107 to transfer the T-register content to the S-bus. Note that if the T-register is selected and the DTRY signal from memory is false, a freeze operation results as described in paragraph 3-211.

3-353. CR (1100). The microcode CR in the S-bus field results in a constant being read to the right half of the S-bus (bits 0 through 7). The constant is obtained from bits 0 through 7 of the ROM Instruction Register (normally special and skip fields of a microinstruction) by a true CR signal from the S-Bus Decoder to ROM Control Card A2. Gates A3U21A,C,D, and A3U11B recognize the CR code and provide a false ENSS signal to disable the special and skip fields of the microinstruction decoder.

3-354. IOI (0001). The microcode IOI in the S-bus field results in the I/O-bus data being read onto the S-bus and is accomplished by an RIOB signal from the S-bus decoder to I/O Buffer Card A8.

3-355. M (0011). The microcode M in the S-bus field results in the M-register content being read onto the S-bus and is accomplished by true SELM and READ signals from the S-bus decoder to Memory Data Control Card A107.

3-356. NOP (1111). The microcode NOP in the S-bus field causes the S-bus to remain all zeros during execution of the microinstruction. No control signals are generated by the S-Bus Decoder.

3-357. P (1110). The microcode P in the S-bus field results in the P-register content being read onto the S-bus. This is accomplished by a true RPLO signal which transfers P-register bits 0 through 8, a true RP9 signal which transfers P-register bit 9, and a true RPHI signal which transfers P-register bits 10 through 15 to the S-bus. A false $\overline{\text{JMPF}}$ signal from the Function Decoder inhibits these three signals. Refer to paragraph 3-382 for detailed information on the $\overline{\text{JMPF}}$ signal.

3-358. RRS (0100). The microcode RRS in the S-bus field results in the R-bus data being read onto the S-bus and is accomplished by a true RRSB signal from the S-bus decoder to Arithmetic/Logic Card A5.

3-359. S1 (1011). The microcode S1 in the S-bus field results in the SP1-register content being read onto the S-bus and is accomplished by a true RSP1 signal from the S-Bus Decoder to Arithmetic/Logic Card A5.

3-360. S2 (1010). The microcode S2 in the S-bus field results in the SP2-register content being read onto the S-bus and is accomplished by true RSP2 signal from the S-Bus Decoder to Arithmetic/Logic Card A5.

3-361. S3 (1001). The microcode S3 in the S-bus field results in the SP3-register content being read onto the S-bus and is accomplished by a true RSP3 signal from the S-Bus Decoder to the Arithmetic/Logic Card A5.

3-362. S4 (1000). The microcode S4 in the S-bus field results in the SP4-register content being read onto the S-bus and is accomplished by a true RSP4 signal from the S-Bus Decoder to Arithmetic/Logic Card A5.

3-363. T (0010). The microcode T in the S-bus field results in the T-register content being read onto the S-bus and is accomplished by true SELT and READ signals from the S-Bus Decoder to Memory Data Control Card A107. Note that if the DTRY signal is not true, a freeze operation results as described in paragraph 3-211.

3-364. FUNCTION FIELD DECODER. The Function Field Decoder monitors ROM Instruction Register bits 12, 13, 14, 15, and 16 and provides control signals required to execute function field microcodes (refer to table 3-9). Function field operations include logical and arithmetic combinations of the R- and S-bus data, 16- and 32-bit shifts and rotates, conditional and unconditional jumps within the microprogram, and jumps to subroutines within the microprogram.

3-365. The logical and arithmetic combinations of the R- and S-bus data are provided by a function generator located on Arithmetic/Logic Card A5 and controlled by six signals from the Function Field Decoder circuits. Table 3-10 gives the functions and corresponding combinations of the six signals. One of the functions shown by table 3-10 is enabled as a result of each microcode in the function field.

3-366. The Function Field Decoder circuits are located on Microinstruction Decoder 2 Card A4. A portion of the Function Field Decoder provides the signals described in table 3-10 which select a logical or arithmetic function for each ROM microinstruction. The remainder of the Function Field Decoder provides control for shifts, rotates, jumps, and jumps to subroutines.

3-367. The following paragraphs describe the operation of the Function Field Decoder for each of the function field microcodes.

Table 3-9. Function Field Microcode Processing

MICRO CODE	OCTAL CODE	RIR BITS CONFIGURATION					OTHER SIGNALS NECESSARY	SIGNALS GENERATED	ALU FUNCTIONS GENERATED
		RIR16	RIR15	RIR14	RIR13	RIR12			
RFI	00	0	0	0	0	0	$\overline{\text{SKIP}}$	$\overline{\text{RFI}}$	F = R-bus
RFE	01	0	0	0	0	1	$\overline{\text{SKIP}}$	$\overline{\text{RFE}}$	F = R-bus
PIA	02	0	0	0	1	0	$\overline{\text{SKIP}}$	$\overline{\text{PIA}}$	F = R-bus
MPY	03	0	0	0	1	1	AR0	FN0, FN3	F = R-bus plus S-bus
DIV	04	0	0	1	0	0	$\overline{\text{SKIP}}$	DIV, CIN, FN1, FN2	F = R-bus minus S-bus
SUB	05	0	0	1	0	1		CIN, FN1, FN2	F = R-bus minus S-bus
DEC	06	0	0	1	1	0		FN1, FN2	F = R-bus minus S-bus minus 1
undefined	07	0	0	1	1	1			
INC0	10	0	1	0	0	0	$\overline{\text{SKIP}}$	ENOV, CIN, FN0, FN3	F = R-bus plus S-bus plus 1
INC	11	0	1	0	0	1		CIN, FN0, FN3	F = R-bus plus S-bus plus 1
ADD0	12	0	1	0	1	0		ENOV, FN0, FN3	F = R-bus plus S-bus
ADD	13	0	1	0	1	1	AR0	FN0, FN3	F = R-bus plus S-bus
AND	14	0	1	1	0	0		MC, FN0, FN1, FN3	F = R-bus • S-bus
NOR	15	0	1	1	0	1		MC, FN0	F = $\overline{\text{R-bus + S-bus}}$
XOR	16	0	1	1	1	0		MC, FN1, FN2	F = R-bus ⊕ S-bus
undefined	17	0	1	1	1	1			
JSB	20	1	0	0	0	0	$\overline{\text{SKIP}}$	MC, $\overline{\text{JMPF}}$, $\overline{\text{JMPS}}$, FN1, FN2, FN3, $\overline{\text{JSB}}$	F = R-bus + S-bus
JSB	21	1	0	0	0	1	$\overline{\text{SKIP}}$	MC, $\overline{\text{JMPF}}$, $\overline{\text{JMPS}}$, FN1, FN2, FN3, $\overline{\text{JSB}}$	F = R-bus + S-bus
JMP	22	1	0	0	1	0	$\overline{\text{SKIP}}$	MC, $\overline{\text{JMPF}}$, $\overline{\text{JMPS}}$, FN1, FN2, FN3	F = R-bus + S-bus
JMP	23	1	0	0	1	1	$\overline{\text{SKIP}}$, AR0	MC, $\overline{\text{JMPF}}$, $\overline{\text{JMPS}}$, FN1, FN2, FN3	F = R-bus + S-bus
CJMP	24	1	0	1	0	0	$\overline{\text{SKIP}}$	MC, $\overline{\text{JMPF}}$, FN1, FN2, FN3, $\overline{\text{CJMP}}$	F = R-bus + S-bus
RSB	25	1	0	1	0	1	$\overline{\text{SKIP}}$	MC, $\overline{\text{RSB}}$, FN1, FN2, FN3	F = R-bus + S-bus
LGS	26	1	0	1	1	0	$\overline{\text{SKIP}}$	MC, $\overline{\text{LGS}}$, FN1, FN2, FN3	F = R-bus + S-bus
CRS	27	1	0	1	1	1	$\overline{\text{SKIP}}$	MC, $\overline{\text{CRS}}$, FN1, FN2, FN3	F = R-bus + S-bus
ARS	30	1	1	0	0	0	$\overline{\text{SKIP}}$	MC, ENOV, $\overline{\text{ARS}}$, FN1, FN2, FN3	F = R-bus + S-bus
undefined	31	1	1	0	0	1		MC, FN1, FN2, FN3	F = R-bus + S-bus
LWF	32	1	1	0	1	0	$\overline{\text{SKIP}}$	MC, ENOV, $\overline{\text{LWF}}$, FN1, FN2, FN3	F = R-bus + S-bus
CFLG	33	1	1	0	1	1	$\overline{\text{SKIP}}$, AR0	MC, $\overline{\text{CFLG}}$, FN1, FN2, FN3	F = R-bus + S-bus
SFLG	34	1	1	1	0	0	$\overline{\text{SKIP}}$	MC, $\overline{\text{JMPF}}$, $\overline{\text{SFLG}}$, FN1, FN2, FN3	F = R-bus + S-bus
CL0	35	1	1	1	0	1	$\overline{\text{SKIP}}$	MC, $\overline{\text{CL0}}$, FN1, FN2, FN3	F = R-bus + S-bus
SOV	36	1	1	1	1	0	$\overline{\text{SKIP}}$	MC, $\overline{\text{SOV}}$, FN1, FN2, FN3	F = R-bus + S-bus
IOR	37	1	1	1	1	1		MC, FN1, FN2, FN3	F = R-bus + S-bus

3-368. ADD (01011). The microcode ADD in the function field results in the R-bus data being added to the S-bus data and placed on the T-bus. Overflow is not saved. Function Field Decoder output signals are those listed in table 3-9 for the ADD function. Signal ENOV is false, disabling the overflow logic.

3-369. ADDO (01010). The microcode ADDO in the function field results in the R-bus data being added to the S-bus data and placed on the T-bus. Overflow is saved. Function Field Decoder outputs are those listed in table 3-9 for the ADDO function. Signal ENOV is true, allowing the overflow logic to be set if an overflow condition occurs during the ADD operation. If the current user instruction is a memory reference group instruction or an ASG2 microcode is present in the special field, the extend logic is also enabled by the true ENOV signal.

3-370. AND (01100). The microcode AND in the function field results in the R-bus data being logically "anded" with the S-bus data and placed on the T-bus. Function Field Decoder output signals are those listed in table 3-9 for the AND function. No other control signals are generated by the Function Field Decoder.

3-371. ARS (11000). The microcode ARS in the function field results in an arithmetic shift of a 32-bit word contained in two of the Arithmetic and Logic section registers. The direction of the shift must be specified in the microinstruction special field (L1 or R1). If a right shift, the B-register contains the most significant 16 bits and the A-register the least significant 16 bits. The B-register content must be read onto the R-bus (microcode B in the R-bus field) and is shifted in the ALU Shifter. The A-register content is shifted internally. If a left shift, the most

significant 16-bits are contained in the F-register and the least significant bits in the Q-register. The F-register content is read onto the R-bus (microcode F in the R-bus field) and shifted in the ALU Shifter. The Q-register is shifted internally. After the shift, the new most significant 16-bits of the word are stored back into the B- (right shift) or F- (left shift) register.

Table 3-10. Function Generator Control

FUNCTION		CONTROL SIGNALS					
		MC	CIN	FN0	FN1	FN2	FN3
ADD	F = R plus S	0	1	1	0	0	1
AND	F = R • S	1	1	1	1	0	1
INC	F = R plus S plus 1	0	0	1	0	0	1
IOR	F = R + S	1	1	0	1	1	1
NOR	F = R + S	1	1	1	0	0	0
SUB 2's comp	F = R plus S plus 1	0	0	0	1	1	0
SUB 1's comp	F = R plus S	0	1	0	1	1	0
XOR	F = R ⊕ S	1	1	0	1	1	0
NOP	F = R	0	0	0	0	0	0

KEY: F = Function Generator Output.
R = R-Bus data.
S = S-Bus data.

3-372. During a right shift, the sign bit (ALU15) becomes ALX16 signal and is copied back into the bit 15 position of the ALU word. Signal ALU0 becomes the carry into A-register bit 15 and A-register bit 0 is shifted out and lost.

3-373. During a left shift, the sign bit (ALU15) becomes ALX14 and is copied back into the bit 15 position of the ALU word, the overflow logic is set if the exclusive "or" function of ALU14 and ALU15 is a logic 1, and bit 15 of the Q-register becomes signal LSI which is shifted into bit 0 position of the ALU word. Input to bit 0 position of the Q-register is zero. In addition to the above, microcode ARS enables the IOR function.

3-374. CFLG (11011). The microcode CFLG in the function field clears the central processor Flag FF and enables the IOR function.

3-375. CJMP (10100). The microcode CJMP in the function field results in a ROM jump if a halt or interrupt is in progress; otherwise, the microcode executes as a NOP. The Function Field Decoder provides false $\overline{\text{CJMP}}$ and $\overline{\text{JMPF}}$ signals. At Timing and Control Card A1, the $\overline{\text{CJMP}}$ signal is gated with signals that indicate a halt or interrupt condition. If halt or interrupt is in progress, the ROM control logic enables a ROM jump. Signal $\overline{\text{JMPF}}$ is routed to Microinstruction Decoder 1 Card A3 to generate false ENSS and EEOP signals which inhibit decoding of the skip and special fields of the microinstruction. The ROM Instruction Register bits in the skip and special fields form the jump-to address within the microprogram. Also signal $\overline{\text{JMPF}}$ disables signals RPLO, RP9, and RPHI to prevent reading the P-register to the S-bus. During execution of the CJMP microcode, the function IOR is enabled.

3-376. CLO (11101). The microcode CLO in the function field sets the $\overline{\text{OVF}}$ FF and enables the IOR function.

3-377. CRS (10111). The microcode CRS in the function field results in a circular shift (rotate) of a 32-bit word contained in two of the Arithmetic and Logic section registers. The direction of the shift must be specified in the special field of the microinstruction (L1 or R1). If a right shift, the B-register contains the most significant 16 bits and the A-register the least significant 16 bits. The B-register content must be read onto the R-bus (microcode B in the R-bus field) and is shifted in the ALU shifter. The A-register content is shifted internally. During the right shift, the AR0 signal becomes the ALX16 signal and is shifted into the ALU shifter bit 15 position. The ALU0 signal is the right shift input to the A-register bit 15 position.

3-378. If a left shift, the most significant 16 bits are contained in the F-register and the least significant bits in the Q-register. The F-register content is read onto the R-bus (microcode F in the R-bus field) and shifted in the ALU shifter. The Q-register is shifted internally. During the left shift, the ALU15 signal becomes the QSI signal and is shifted into the Q-register bit 0 position. The left shift carry out of the Q-register becomes the LSI signal and is shifted into the bit 0 position of the ALU word. In addition to the above, microcode CRS enables the IOR function.

3-379. DEC (00110). The microcode DEC in the function field performs a 1's complement of the S-bus word and adds the result to the R-bus word. This is most commonly used with the S-bus word equal to zero and actually results in a decrement of the R-bus word placed on the T-bus. This is accomplished by Function Field Decoder output signals shown for the SUB 1's complement function.

3-380. DIV (00100). The microcode DIV in the function field results in an integer divide step. The dividend is a positive 32-bit word with bits 0 through 15 in the A-register and bits 16 through 31 in the F-register. The divisor is a positive 16-bit word normally located in one of the scratch pad registers. As used in the extended arithmetic DIVID microroutine, the divide step is executed 16 times in a repeat loop to perform a complete binary divide.

3-381. To understand the DIV microcode, it is necessary to examine the complete microinstruction used to perform the divide operation. The microcodes are as follows:

a. R-bus field, F
b. S-bus field, S2
c. Function field, DIV
d. Store field, F
e. Special field, L1
f. Skip field, CTRI

3-382. The algorithm in table 3-11 shows the data manipulation required to perform a binary divide operation. Lines 1, 2, 3, and 4 show the required initialization before the actual divide is accomplished. The Q- and F-registers contain the dividend and scratch pad 2, the divisor. Some

previously executed routine must ensure that these are positive numbers and can be divided without error (that is divisor not equal to zero, etc.). Line 4 initializes a counter and line 5 states that as long as the count is not equal to 16, the following will be executed.

3-383. Lines 6 through 16 occur as a result of the microinstruction described in paragraph 3-375. Of these, lines 8, 9, 10, 12, 13, 14, and 15 can be attributed to the DIV microcode. This microinstruction, because of the DIV microcode, is executed in two cycles. As described in paragraph 3-207, the first cycle generates a central processor freeze. This inhibits any store operation until the condition stated by line 9 of the algorithm can be evaluated. Since the store operations specified by the microinstruction are inhibited by the freeze, no register content is changed. The second cycle is then identical to the first with the addition of the F-register and Q-register store operation selected by lines 9 and 13 of the algorithm.

3-384. Lines 18 and 19 state that after the 16 divide operations have been performed, the quotient is stored in the Q-register and the remainder is stored in the F-register.

3-385. INC (01001). The microcode INC in the function field results in the sum of the R-bus data, the S-bus data plus 1 being placed on the T-bus. This is generally used with zeros on one bus and a word to be incremented on the other. Control signals from the Function Field Decoder are those listed in table 3-10 for INC function.

Table 3-11. DIV Algorithm

LINE NO.	OPERATION
1	LET (Q) = DIVIDEND (0:15)
2	LET (F) = DIVIDEND (16:31)
3	LET (SP2) = DIVISOR (0:15)
4	LET COUNT = 0
5	WHILE COUNT ≠ 16 DO
6	R-BUS := (F)
7	S-BUS := (SP2)
8	ALU (0:15) := (R-BUS - S-BUS)
9	IF ALU (0:15) POSITIVE THEN DO
10	T-BUS := ALU (0:15) x 2 + (Q(15))
11	(F) := T-BUS
12	(Q) := (Q) x 2 + 1
13	ELSE
14	(F) := (F) x 2 + (Q(15))
15	(Q) := (Q) x 2
16	COUNT := COUNT + 1
17	END
18	QUOTENT := (Q)
19	REMAINDER := (F)
20	END

3-386. INCO (01000). The microcode INCO in the function field results in the R-bus data plus the S-bus data plus 1 being placed on the T-bus. Overflow is saved. Function decoder outputs are those listed in table 3-10 for INC function. The ENOV signal is true, allowing the overflow logic to be set if an overflow occurs. If the current user instruction is a memory reference group instruction, the extend logic is also enabled by the ENOV signal.

3-387. IOR (11111). The microcode IOR in the function field results in a logical inclusive "or" of the R-bus data and the S-bus data placed on the T-bus. Function Field Decoder output signals are those listed in table 3-10 for IOR function.

3-388. JMP (10010 or 10011). The microcode JMP in the function field results in a ROM jump. The Function Field Decoder provides false $\overline{\text{JMPS}}$ and $\overline{\text{JMPF}}$ signals. The $\overline{\text{JMPF}}$ signal is routed to Microinstruction Decoder 1 Card A3 to generate false ENSS and EEOP signals which inhibit decoding of the skip and special fields of the microinstruction. The jump-to address is formed by RIR bits 0 through 7 (the contents of the skip and special fields), bit 12 of the function field, and bit 17 of the S-bus field. Bits 0 through 7 are transferred to the corresponding bits of the ROM Address Register, bit 17 is transferred to bit 8 of the ROM Address Register, and bit 12 is transferred to bit 9 of the ROM Address Register. The $\overline{\text{JMPF}}$ signal also disables the RPLO, RP9, and RPHI signals to prevent reading the P-register onto the S-bus.

3-389. During execution of the JMP microcode, the function IOR is also enabled.

3-390. JSB (10000 or 10001). The microcode JSB in the function field has the same results as the JMP microcode except that JSB also causes the JSB FF to be set. This microcode causes the ROM Address Register to jump to the location of a microprogram subroutine and store the subroutine return address in the Save register.

Note: The microcodes JMP, JSB, RSB, and CJMP each require two machine cycles to execute. The microinstruction containing the jump is executed during the first cycle, and a NOP is executed in the second cycle. The second cycle is used to allow data to be accessed from the ROM control store at the new address.

3-391. LGS (10110). The microcode LGS in the function field results in a 32-bit logical shift. The direction of the shift is specified in the Special Field microcode (L1 or R1). The A- and B-registers are used for right shifts, and the F- and Q-registers are used for left shifts.

3-392. During execution of the LGS microcode, the function IOR is also enabled.

3-393. LWF (11010). The microcode LWF in the function field links the output of the Flag FF with the shifter. The linking of the Flag FF is dependent upon the microcode in the special field. If microcode L1 is in the special field, the content of the Flag FF is shifted into bit 0 of the shifter and the function generator output is trarsferred to the Flag FF. If microcode R1 is in the special field, the contents of the Flag FF is shifted to the right-shift input of the shifter, thereby shifting its content to T-bus bit 15, and the function generator output for bit 0 is transferred to the Flag FF.

3-394. During the execution of the LWF microcode, the function IOR is also enabled.

3-395. MPY (00011). The microcode MPY in the function field causes bit 0 of the A-register to be checked for an add decision on Microinstruction Decoder 2 Card A4. If this bit is high, the ALX16 signal is generated and the R- and S-bus inputs to the Arithmetic Function Generator circuits are added; if the bit is low, only the R-bus inputs are routed through the function generator. In either case, the output of the function generator is shifted right one place and stored back into the R-bus register specified by the Store Field microcode (normally the B-register). The A-register is shifted right independently of the function generator shift. The signals $\overline{\text{COUT}}$ and ALU0 of the function generator are routed to bits 15 of the specified R-bus register and the A-register, respectively, and bit 0 of the A-register is lost.

3-396. A valid multiply requires microcode R1 be specified in the special field; also, normally, the microcode B is specified in the R-bus and store fields, and S1, S2, S3, or S4 is specified in the S-bus field.

3-397. NOR (01101). The microcode NOR in the function field results in the logical "nor" of the R- and S-bus inputs to the function generator circuits. If an NOP is specified in the R-bus microcode field, the result is the complement of the S-bus. The opposite is true if the NOP is specified in the S-bus microcode field. If both the R- and S-bus microcode fields specify a NOP microcode, the output of the function generator will consists of all "1's".

3-398. P1A (00010). The microcode P1A in the function field causes phase 1A to be set and the current operating phase to be cleared. This microcode is used mainly by diagnostic programs.

3-399. RFE (00001). The microcode RFE in the function field causes the contents of the Flag and Extend flip-flops to be rotated.

3-400. RFI (00000). The microcode RFI in the function field causes the contents of the Flag and Index Mode flip-flops to be rotated. This microcode is not intended for use in special microprogramming. The use of this code will affect the operation of module 0 and consequently cause incorrect operation of HP software.

3-401. RSB (10101). The microcode RSB in the function field causes the contents of the Save register to be transferred to the ROM Address register and clears the JSB flip-flop. This microcode also enables the IOR function. (See JSB note.)

3-402. SFLG (11100). The microcode SFLG in the function field causes the Central Processor Unit (CPU) Flag flip-flop on Microinstruction Decoder 2 Card A4 to be set and enables the IOR function.

3-403. SOV (11110). The microcode SOV in the function field causes the Overflow flip-flop on Microinstruction Decoder 2 Card A4 to be set and the IOR function to be enabled.

3-404. SUB (00101). The microcode SUB in the function field causes the S-bus to be subtracted from the R-bus in 2's complement form.

3-405. XOR (01110). The microcode XOR in the function field causes the R- and S-bus to be logically exclusive "ored".

3-406. STORE FIELD DECODER. The Store Field Decoder monitors ROM Instruction Register bits 8, 9, 10, and 11 and provides control signals required to execute store field microcodes (see table 3-12). Store field operations include all data storing operations of the various registers within the computer and the transferring of the S-bus data onto the I/O bus for data transfer to an external peripheral device. The store field decoder circuits are located on Microinstruction Decoder 1 Card A3.

3-407. The following paragraphs describe the operation of the store field decoder for each of the store field microcodes.

3-408. A (1110). The microcode A in the store field causes the data on the T-bus to be stored in the A-register. The STA signal causes the A-register to accept the input data.

3-409. AAB (1100). The microcode AAB in the store field causes data on the T-bus to be stored in either the A- or B-register, depending on whether the A-Addressable FF or B Addressable FF is set. If neither flip-flop is set, no store will occur. The STA or STB signals cause the A-register or B-register, respectively, to accept the input data.

3-410. B (1101). The microcode B in the store field causes data on the T-bus to be stored in the B-register. The STB signal causes the B-register to accept the input data.

3-411. CAB (1011). The microcode CAB in the store field causes data on the T-bus to be stored in either the A- or B-register, depending on the state of Instruction Register bit eleven (IR11). If IR11 is low the T-bus data will be stored in the A-register. If IR11 is high the T-bus data will be stored in the B-register. The STA and STB signals cause the A-register and B-register, respectively, to accept the input data.

Table 3-12. Store Field Microcode Processing

MICRO CODE	OCTAL CODE	RIR BITS CONFIGURATION				DEOCDER USED	ENABLE SIGNAL	SIGNAL GENERATED	DESTINATION OF DATA TO BE STORED*
		RIR11	RIR10	RIR9	RIR8				
IOO	00	0	0	0	0	U93	$\overline{SKIP}$	$\overline{IOO}$	I/O Bus
M	01	0	0	0	1			$\overline{M}$	M-register and Violation register
T	02	0	0	1	0			$\overline{T}$	T-register
IR	03	0	0	1	1			$\overline{IR}$	I-register
S4	04	0	1	0	0			$\overline{S4}$	Scratch Pad 4
S3	05	0	1	0	1			$\overline{S3}$	Scratch Pad 3
S2	06	0	1	1	0			$\overline{S2}$	Scratch Pad 2
S1	07	0	1	1	1			$\overline{S1}$	Scratch Pad 1
P	10	1	0	0	0	U83		$\overline{P}$	P-register
F	11	1	0	0	1			$\overline{F}$	F-register
Q	12	1	0	1	0			$\overline{Q}$	Q-register
CAB	13	1	0	1	1			$\overline{CAB}$	A- or B-register
AAB	14	1	1	0	0			$\overline{AAB}$	A- or B-register
B	15	1	1	0	1			$\overline{B}$	B-register
A	16	1	1	1	0			$\overline{A}$	A-register
NOP	17	1	1	1	1				

* Refer to text for specific register selected if more than one is given.

3-412. F (1001). The microcode F in the store field causes data on the T-bus to be stored in the F-register. The STOF signal causes the F-register to accept the input data.

3-413. IOO (0000). The microcode IOO in the store field causes data on the S-bus to be transferred onto the I/O bus. The SIOB signal causes the data on the S-bus to transfer to the I/O bus.

3-414. IR (0011). The microcode IR in the store field causes data on the S-bus to be stored in the Instruction Register. The STI signal causes the Instruction Register to accept the input data at $\overline{CLK2}$ time.

3-415. M (0001). The microcode M in the store field causes data on the S-bus to be stored in the M-register. The S-bus data is also stored in the Violation register if the computer is in phase 1A, memory protect is set and no memory protect violation has been detected, and no parity error exists. The STORE signal generated by the store field decoder, along with the SELM signal causes the S-bus data to be stored in the M-register at $\overline{CLK3}$ time. The SELM signal is generated by the S-bus field decoder circuits.

3-416. P (1000). The microcode P in the store field causes data on the T-bus to be stored in the P-register. The STP signal causes the P-register to accept the input data.

3-417. Q (1010). The microcode Q in the store field causes data on the T-bus to be stored in the Q-register. The STQ signal causes the Q-register to accept the input data.

3-418. S1 (0111). The microcode S1 in the store field causes data on the T-bus to be stored in the Scratch Pad 1 register. The WSP1 signal causes Scratch Pad 1 register to accept the input data.

3-419. S2 (0110). The microcode S2 in the store field causes data on the T-bus to be stored in the Scratch Pad 2 register. The WSP2 signal causes Scratch Pad 2 register to accept the input data.

3-420. S3 (0101). The microcode S3 in the store field causes data on the T-bus to be stored in the Scratch Pad 3 register. The WSP3 signal causes Scratch Pad 3 register to accept the input data.

3-421. S4 (0100). The microcode S4 in the store field causes data on the T-bus to be stored in the Scratch Pad 4 register. The WSP4 signal causes Scratch Pad 4 register to accept the input data.

3-422. T (0010). The microcode T in the store field causes data on the S-bus to be stored in the T-register. The STORE signal generated by the store field decoder, along with the SELT signal causes the S-bus data to be stored in the T-register at $\overline{CLK3}$ time. The SELT signal is generated by the S-bus field decoder circuits.

3-423. NOP (1111). The microcode NOP in the store field causes all store functions to be disabled.

3-424. SPECIAL FIELD DECODER. The special field decoder monitors ROM Instruction register bits 4, 5, 6, and 7 and provides control signals required to execute special field microcodes. (See table 3-13.) These microcodes provide for several miscellaneous operations such as skip sense, addressable A/B, shift, counter, and memory. The microcodes also provide for special ASG and SRG functions.

3-425. The skip sense operation uses the microcode RSS in the special field and causes the micro-skip test logic to test for a condition which is the complement of that specified in the Skip field. For example, if the skip field specifies a microprogram skip on a cleared condition, the skip sense microcode RSS in the special field will cause the microprogram skip to occur on a set condition.

3-426. The addressable A/B operation uses the microcode RW in the special field. With this microcode, if the T-bus bits 1 through 14 are all "0", and the ALU0 signal is high or low, the B Addressable FF or A Addressable FF, respectively, will be set. The A or B Addressable FF being set indicates that the data to be accessed is in either the A- or B-register, not in a core memory location. A core memory fetch (and synchronization) is still executed though it is not necessary. The following microinstruction, which normally contains microcodes in AAB and COND in its R- and S-bus fields, respectively, determines where to get the data.

3-427. The shift operation uses the microcodes L1 or R1 for causing the data from the arithmetic function generator to be shifted one bit position to the left or one bit position to the right, respectively. These microcodes also enable long shifts of the higher order word. When this feature is used, the lower order word is shifted internally in the appropriate register.

3-428. The counter operation uses the microcode CNTR to load bits 0 through 3 of the S-bus into the Repeat Counter and clear bit 4 (the carry out bit) of the counter.

3-429. The memory operation uses the microcodes RW and CW. RW causes a read/write memory cycle to be executed and place memory data into the T-register. CW causes a clear/write memory cycle to be executed and place the contents of the T-register into the addressed memory location. The operation of the CW microcode requires a "true" skip condition (specified in the Skip field); if the skip condition is not specified or not "true" the CW operation will be inhibited.

3-430. AAB (0110). The microcode AAB in the special field enables the setting of the A Addressable FF or the B Addressable FF if T-bus bits 1 through 14 are all "0's" and depending upon the state of the ALU0 signal. If ALU0 is low, the A Addressable FF will be set. If ALU0 is high, the B Addressable FF will be set.

3-431. ASG1 (1010). The microcode ASG1 in the special field enables the skip and extend logic specified by Instruction Register bits 0 and 3 through 7. (Register handling is done by microprogram; see table 3-14.)

3-432. ASG2 (1011). The microcode ASG2 in the special field enables the skip and increment logic specified by Instruction Register bits 0, 1, and 2. (Register handling is done by microprogram; see table 3-14.)

3-433. CNTR (0011). The microcode CNTR in the special field causes S-bus bits 0 through 3 to be stored in the Repeat Counter and clears bit 4 (the carry out bit) of the Repeat Counter.

Table 3-13. Special Field Microcode Processing

MICRO CODE	OCTAL CODE	RIR BITS CONFIGURATION				DECODER USED	ENABLE SIGNAL	SIGNAL GENERATED
		RIR7	RIR6	RIR5	RIR4			
RSS	00	0	0	0	0	U35	ENSS	$\overline{RSS}$
L1	01	0	0	0	1			$\overline{L1}$
R1	02	0	0	1	0			$\overline{R1}$
CNTR	03	0	0	1	1			$\overline{CNTR}$
SRG1	04	0	1	0	0			$\overline{SRG1}$
SRG2	05	0	1	0	1			$\overline{SRG2}$
AAB	06	0	1	1	0			$\overline{AAB}$
LEP	07	0	1	1	1			
ECYZ	10	1	0	0	0	U36		$\overline{ECYZ}$
ECYN	11	1	0	0	1			$\overline{ECYN}$
ASG1	12	1	0	1	0			$\overline{ASG1}$
ASG2	13	1	0	1	1	U46B		ASG2
CW	14	1	1	0	0	U36, U46A		$\overline{CW}$, RWCW
IOG1	15	1	1	0	1	U64A		IOG1
RW	16	1	1	1	0	U36, U46A		$\overline{RW}$, RWCW
NOP	17	1	1	1	1			

Table 3-14. Alter-Skip Group Microroutines

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0021	47777657	ASGD	CAB	–	IOR	–	ASG1	–	Executes the ASG instructions where I-register bits 8:9 = 0.
0022	47525675		CAB	–	ADDO	CAB	ASG2	EOP	
0023	77777777			–	IOR	–	–	–	
0025	77775657	ASGA	–	–	IOR	CAB	ASG1	–	Executes the ASG instructions where I-register bits 8:9 indicate CLA/B.
0026	47525675		CAB	–	ADDO	CAB	ASG2	EOP	
0027	77777777		–	–	IOR	–	–	–	
0031	47555657	ASGB	CAB		NOR	CAB	ASG1		Executes the ASG instructions where I-register bits 8:9 indicate CMA/B.
0032	47525675		CAB		ADDO	CAB	ASG2	EOP	
0033	77777777				IOR				
0035	77555657	ASGC			NOR	CAB	ASG1		Executes the ASG instructions where I-register bits 8:9 indicate CCA/B.
0036	47525675		CAB		ADDO	CAB	ASG2	EOP	
0037	77777777				IOR				

3-434. CW (1100). The microcode CW in the special field causes a clear/write memory cycle to be generated, thereby causing the T-register data to be written into core memory at the end of the cycle. This microcode also causes the CPU to "freeze" until I/O time T6 prior to starting the clear/write memory cycle. CW is enabled by a skip microcode, normally NMPV or UNC, in the skip field. Microcode UNC is used if memory-protect testing is not desired.

3-435. ECYN (1001). The microcode ECYN in the special field causes the P-CARRY FF on Timing and Control Card A1 to be set at the end of $\overline{\text{CLK1}}$ time if the T-bus does not contain all "0's". The P-CARRY FF being set causes the P-register to be incremented upon exiting from the execute phase. The P-register being incremented at this time causes the next software program instruction to be skipped.

3-436. ECYZ (1000). The microcode ECYZ in the special field causes the P-CARRY FF on Timing and Control Card A1 to be set at the end of $\overline{\text{CLK1}}$ time if the T-bus contains all "0's". The P-CARRY FF being set causes the P-register to be incremented upon exiting from the execute phase. The P-register being incremented at this time causes the next software program instruction to be skipped.

3-437. IOG1 (1101). The microcode IOG1 in the special field causes the CPU to synchronize with I/O timing and enables the I/O group decoder.

3-438. L1 (0001). The microcode L1 in the special field causes the SL1 and TBS2 signals to be generated, enabling the left-shift-one logic on the Arithmetic/Logic Card A5. This causes the shifter multiplexer to shift the function generator output bits 0 through 14 to T-bus lines 1 through 15 and leaving a "0" on T-bus line 0' Microcode L1 is frequently used in combination with function field microcodes ARS, CRS, LGS, DIV, and MPY. Refer to the description of the function field decoder (paragraphs 3-364 through 3-405) for information on microcode L1 when used in this manner.

3-439. LEP (0111). The microcode LEP in the special field causes the microprocessor to execute NOPs until a legal entry point of a MAC code Extend Arithmetic Group instruction microprogram is detected or until EOP is detected in the skip field. The LEP microcode prevents illegal entry into an Extended Arithmetic Group instruction microprogram through the use of an incorrect MAC code. LEP cannot be used for anything other than enabling entry points to the 2100A Computer Extended Arithmetic Group instructions coded in ROM module 0 only.

3-440. R1 (0010). The microcode R1 in the special field causes the SR1 and TBS1 signals to be generated, enabling the right-shift-one logic on Arithmetic/Logic Card A5. This causes the shifter multiplexer to shift the function generator output bits 1 through 15 to T-bus lines 0 through 14 and leaving a "0" on T-bus line 15. Microcode R1 is frequently used in combination with function field microcodes ARS, CRS, LGS, DIV, and MPY. Refer to the description of the function field decoder (paragraphs 3-364 through 3-405) for information on microcode R1 when used in this manner.

3-441. RSS (0000). The microcode RSS in the special field causes the skip sense of the skip field microcode to be complemented (i.e., if the skip sense is testing for all zeros, RSS in the special field will cause the skip sense to test for not all zeros).

3-442. RW (1110). The microcode RW in the special field causes a read/write memory cycle to be generated, thereby causing the data in the addressed core memory location to be transferred to the T-register and written back into the same memory location from the T-register. Thus, the core memory data is made available for CPU use through the T-register. This microcode also causes the CPU to "freeze" until I/O time T6 prior to starting the read/write memory cycle and the shifter multiplexer output to be tested for address 0 or 1, setting the A Addressable FF or B Addressable FF accordingly.

3-443. SRG1 (0100). The microcode SRG1 in the special field along with Instruction Register bits 6 through 9 enables the shift-rotate functions within the CPU. This microcode also causes the SRG FF to be set at the end of $\overline{CLK2(B)}$ signal for 196 ns, thus causing the SCRY signal to be generated if bit 0 of the function generator output (ALU0) is a "0" and Instruction Register bit 3 is a "1". Also, this microcode sets or resets the EXTEND FF depending on the state of bits 0 and 15 from the function generator circuits (ALU0 and ALU15). (Register handling is done by microprogram; see table 3-15.)

3-444. SRG2 (1011). The microcode SRG2 in the special field along with Instruction Register bits 0 through 2 and bit 4 enables the shift-rotate functions within the CPU. This microcode also sets or resets the EXTEND FF depending on the state of bits 0 and 15 from the function generator circuits (ALU0 and ALU15). (Register handling is done by microprogram; see table 3-15.)

3-445. SKIP FIELD DECODER. The Skip Decoder monitors ROM Instruction Register bits 0, 1, 2, and 3 and provides control signals required to execute skip field microcodes. (See table 3-16.) Skip field operations permit one of several conditions to be specified for possible microinstruction skip decisions. Ten skip conditions can be specified as well as three special functions, a test for no memory-protect violation, and an unconditional skip microcode. The skip decoder circuits are located on Instruction Register Decoder Card A6.

3-446. The following paragraphs describe the operation of the skip decoder for each of the skip field microcodes.

Note: The term "skip", as used in the 2100A Computer microprocessor, is unconventional in that, if a skip condition is detected, the following microinstruction is not "jumped over". Instead, it is read from ROM but not decoded and therefore not executed. The store field microcodes are inhibited but the R-bus, S-bus, and the Function field microcodes that control the output of the function generator are not inhibited. Thus, the R- and S-bus data is transferred through the function generator onto the T-bus but is not stored in any register.

3-447. AAB (1011). The microcode AAB in the skip field causes the next microinstruction to be skipped if either the A Addressable FF or B Addressable FF is set.

3-448. COUT (0100). The microcode COUT in the skip field causes the next microinstruction to be skipped if the carry-out signal (COUT) from arithmetic function generator circuits is true.

3-449. CTR (1001). The microcode CTR in the skip field causes the next microinstruction to be skipped if the repeat counter bits 0 through 3 are all "1's". Bit 4 of the counter is ignored.

3-450. CTRI (1000). The microcode CTRI in the skip field causes the next microinstruction to be skipped if the repeat counter bits 0 through 3 are all "1's". Bit 4 of the counter is ignored. The microcode CTRI also causes the counter to be incremented after testing.

3-451. EOP (1101). The microcode EOP in the skip field causes the current operating phase to terminate, sets the correct next phase flip-flop and executes a hardware jump through the ROM mapper to the ROM address which begins the next phase. The microinstruction immediately following the microinstruction containing the EOP microcode is executed prior to jumping to the ROM starting address of the next phase. The EOP microcode also causes the JSB FF to be cleared. If the microinstruction preceding the microinstruction containing the EOP microcode contains the microcode UNC in its skip field, the microinstruction containing the EOP will be "skipped" except for the EOP microcode, which will be executed. But, if the microinstruction preceding the microinstruction containing the EOP microcode contains the microcode JMP in its function field, the microinstruction containing the EOP will be jumped over and the EOP microcode will not be executed.

Table 3-15. Shift-Rotate Group Microroutines

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0100	07777117	SRGA	A	–	IOR	A	SRG1	–	Executes the SRG instructions involving the A-register.
0101	07777777		A	–	IOR	–	–	–	
0102	07777135		A	–	IOR	A	SRG2	EOP	
0103	77777777		–	–	IOR	–	–	–	
0104	17776517	SRGB	B	–	IOR	B	SRG1	–	Executes the SRG instructions involving the B-register.
0105	17777777		B	–	IOR	–	–	–	
0106	17776535		B	–	IOR	B	SRG2	EOP	
0107	77777777		–	–	IOR	–	–	–	

Table 3-16. Skip Field Microcode Processing

MICRO CODE	OCTAL CODE	RIR BITS CONFIGURATION				DECODER USED	ENABLE SIGNAL	SIGNAL GENERATED
		RIR3	RIR2	RIR1	RIR0			
ICTR	00	0	0	0	0	U27	ENSS	$\overline{\text{ICTR}}$
RPT	01	0	0	0	1			$\overline{\text{RPT}}$
ODD	02	0	0	1	0			$\overline{\text{ODD}}$
NEG	03	0	0	1	1			$\overline{\text{NEG}}$
COUT	04	0	1	0	0			$\overline{\text{COUT}}$
OVF	05	0	1	0	1			$\overline{\text{OVF}}$
FLG	06	0	1	1	0			$\overline{\text{FLG}}$
TBZ	07	0	1	1	1			$\overline{\text{TBZ}}$
CTR1	10	1	0	0	0	U17		$\overline{\text{CTR1}}$
CTR	11	1	0	0	1			$\overline{\text{CTR}}$
NMPV	12	1	0	1	0			$\overline{\text{NMPV}}$
AAB	13	1	0	1	1			$\overline{\text{AAB}}$
NAAB	14	1	1	0	0			$\overline{\text{NAAB}}$
EOP	15	1	1	0	1			$\overline{\text{EOP}}$
UNC	16	1	1	1	0			$\overline{\text{UNC}}$
NOP	17	1	1	1	1			

3-452. FLG (0110). The microcode FLG in the skip field causes the CPU FLAG FF on Microinstruction Decoder 2 Card A4 to be tested and the next microinstruction to be skipped if the FLAG FF is set.

3-453. ICTR (0000). The microcode ICTR in the skip field causes the repeat counter to be incremented by one count.

3-454. NAAB (1100). The microcode NAAB in the skip field causes the next microinstruction to be skipped if T-bus bits 1 through 14 are not all "0's". Normally used to detect the addressing of the A- or B-register so that the A Addressable or B Addressable flip-flop can be set.

3-455. NEG (0011). The microcode NEG in the skip field causes the next microinstruction to be skipped if the output from the arithmetic function generator is negative (ALU15 signal is high).

3-456. NMPV (1010). The microcode NMPV in the skip field causes the next microinstruction to be skipped if memory protect is disabled (MPC signal is low) or the A Addressable and B Addressable flip-flops are clear. The skip is also generated if the A Addressable and B Addressable flip-flops are clear and the output from the arithmetic function generator is negative (ALU15 signal is high). If the A Addressable or B Addressable is set, no skip will occur.

3-457. ODD (0010). The microcode ODD in the skip field causes the next microinstruction to be skipped if the output from the arithmetic function generator is odd (ALU0 signal is high).

3-458. OVF (0101). The microcode OVF in the skip field causes the next microinstruction to be skipped if the Overflow flip-flop is set (OVFF signal is high).

3-459. RPT (0001). The microcode RPT in the skip field causes the next microinstruction to be repeated until the skip condition indicated in the skip field of the repeated microinstruction is met. The repeated microinstruction cannot contain microcode TBZ in its skip field or microcode RSS in its special field along with TBZ in the skip field. Also, the repeated microinstruction cannot contain an add-type microcode in its function field (ADD, INC, etc.) if microcodes NEG or ODD are in its skip field regardless of microcode RSS being in its special field.

3-460. TBZ (0111). The microcode TBZ in the skip field causes the next microinstruction to be skipped if the T-bus contains all "0's" (TBZ signal is high).

3-461. UNC (1110). The microcode UNC in the skip field causes the next microinstruction to be skipped unconditionally.

3-462. NOP (1111). The microcode NOP in the skip field results in the microinstruction not operating this field.

3-463. REPEAT COUNTER.

3-464. The repeat counter, located on Instruction Register Decoder Card A6, consists of a 4-bit counter (A6U55), the RCR FF, and gating circuits. The repeat counter is used during execution of the Extended Arithmetic Group instructions to perform a specified number of multiply and divide operations and to perform the number of shifts specified by IR0 through IR3.

3-465. The counter can be loaded, incremented, or cleared by detecting certain microcodes in the ROM microinstruction. The microcodes affecting the operation of the repeat counter are CNTR in the S-bus field, CNTR in the special field, and CTRI or ICTR in the skip field.

3-466. LOADING THE COUNTER. The counter is loaded by detecting CNTR in the special field. This causes the special field decoder circuits to apply a false CNTR signal to the parallel enable terminal of the 4-bit counter A6U55. When the $\overline{CLK2}$ signal goes false (which applies a true input to the clock terminal of A6U55), the counter is loaded with S-bus bits 0 through 3.

3-467. INCREMENTING THE COUNTER. The counter is incremented by detecting CTRI or ICTR in the skip field. This causes the skip field decoder circuits to apply a true input to the count terminal of A6U55 via the (ICTR + CTRI) signal line. When the $\overline{CLK2}$ signal goes false, the counter is incremented by one. When the $\overline{CLK2}$ signal becomes true (during the last half of the clock period), the new count is present on the output lines from A6U55.

3-468. The RCR FF stores the fifth bit (bit 4) of the counter. Bit 4 is generated by "anding" the carry output (CRY terminal) of A6U55 with the (ICTR + CTRI) signal line from the skip field decoder circuits. When the 4-bit counter contains all "1's", the carry output becomes true. If an increment condition is detected, the "anding" of the true carry output and the true (ICTR + CTRI) signal line provides a set condition for the RCR FF, thereby storing a true bit 4.

3-469. The carry output line is also used for generating a skip condition whenever CTRI or CTR is detected in the skip field.

3-470. CLEARING THE COUNTER. The counter is cleared by decoding a NOP in the S-bus field (results in all "0's" on the S-bus) and decoding CNTR in the special field to enable the parallel load function of the counter.

3-471. GATING ONTO THE S-BUS. The contents of the counter are gated onto the S-bus by decoding CNTR in the S-bus field. When CNTR is decoded, a true RCTR signal is applied to pin 81 of A6. Bit 0 through 4 from the counter is gated onto S-bus bits 0 through 4.

3-472. EAG DOUBLEWORD SHIFTS AND ROTATES. During execution of the microroutines for double word shifts and rotates, the repeat counter counts the number of times that the ROM microinstruction performing the shift (or rotate) is executed. A typical ROM operation affecting the repeat counter during these shifts (or rotates) is as follows:

a. Store the 2's complement of the shift count (IR0 through IR3) into Scratch Pad 2. (This is accomplished by decoding ADR in the S-bus field, SUB in the function field, and S2 in the store field.)

b. Read Scratch Pad 2 onto the S-bus and store into the repeat counter. Set the repeat mode. (This is accomplished by decoding S2 in the S-bus field, CNTR in the special field, and RPT in the skip field.)

c. Perform the shift (or rotate) and test the repeat counter contents (bits 0 through 3) for all "1's". Increment the counter after testing the contents. (Testing and incrementing the counter is accomplished by decoding CTRI in the skip field. The microcode contents of the other fields depends on the type of operation to be performed.) When the counter contains all "1's", the repeated microinstruction will be skipped.

3-473. EAG MULTIPLY AND DIVIDE OPERATIONS. During execution of the microroutines for the MPY and DIV instructions, the repeat counter causes the ROM microinstruction containing the multiply (or divide) function to be executed 16 times. The microinstruction must be executed 16 times to perform a complete multiply or divide operation. A typical ROM operation affecting the repeat counter during execution of these microroutines is as follows:

a. Clear the repeat counter and set the repeat mode. (This is accomplished by decoding NOP in the S-bus field, CNTR in the special field, and RPT in the skip field.)

b. Execute multiply (or divide) function and test the repeat counter contents (bits 0 through 3) for all "1's". Increment the counter after testing the contents. (Testing and incrementing the counter is accomplished by decoding CTRI in the skip field.) The multiply (or divide) function will be executed 16 times, which is the number of times the counter can be incremented before bits 0 through 3 of the counter are "1's".

3-474. ARITHMETIC AND LOGIC SECTION DETAILED THEORY.

3-475. The arithmetic and logic section of the 2100A Computer consists of the A-, B-, F-, Q-, P-, and SP1 through SP4 registers, the R-bus multiplexer, arithmetic function generator, and shifter circuits on Arithmetic/Logic Card A5. It also includes the A-Addressable and B Addressable flip-flop logic and Extend logic on Instruction Register Decoder Card A6, and the A/B Clear and A/B Select flip-flop logic, shift linkage, RFE logic, CPU flag logic, and overflow logic in Microinstruction Decoder 2 Card A4.

3-476. The function field decoding circuits on Microinstruction Decoder 2 Card A4 decode ROM bits 12 through 13 and generate the MC, $\overline{CIN}$, and FN0 through FN3 signals. These signals are used by the arithmetic function generator circuits to arithmetically or logically manipulate the data sent to the function generator circuits (see table 3-17) from the various above mentioned registers under microprogram control via the multiplexer circuits and the R- and S-buses. The data is relayed from the function generator circuits to the T-bus via the shifter.

Table 3-17. Function Generator Operation

FUNCTION SELECT				OUTPUT FUNCTION				
FN3	FN2	FN1	FN0	LOGIC FUNCTIONS (MC = H)	INC = H	ARITHMETIC OPERATIONS (MC = L)	INC = H	INC = L
S3	S2	S1	S0					
L	L	L	L	F = A		F = 1	RALU	
L	L	L	H	F = A+B	NOR	F = A+B		
L	L	H	L	F = AB		F = A+B		
L	L	H	H	F = Logical 0		F = minus 1 (2's complement)		
L	H	L	L	F = AB		F = A plus AB		
L	H	L	H	F = B		F = [A+B] plus AB		
L	H	H	L	F = A ⊕ B	XOR	F = A minus B minus 1	DEC	SUB
L	H	H	H	F = AB		F = AB minus 1		
H	L	L	L	F = A+B		F = A plus AB		
H	L	L	H	F = A ⊕ B		F = A plus B	ADD	INC
H	L	H	L	F = B		F = [A+B] plus AB		
H	L	H	H	F = AB	AND	F = AB minus 1		
H	H	L	L	F = Logical 1		F = A plus A 1		
H	H	L	H	F = A+B		F = [A+B] plus A		
H	H	H	L	F = A+B	IOR	F = [A+B] plus A		
H	H	H	H	F = A		F = A minus 1		

3-477. A-ADDRESSABLE AND B-ADDRESSABLE FF LOGIC.

3-478. The A-Addressable and B-Addressable Flip-Flop logic located on Instruction Register Decoder Card A6, contains two flip-flops (A ADDR FF and B ADDR FF) which direct the storing of data into A- or B-register, depending upon which addressable flip-flop is set. One or the other of these flip-flops may be set (or neither), but not both. If the A ADDR FF is set, it indicates that the A-register is being addressed as a memory location. Similarly, if the B ADDR FF is set, it indicates that the B-register is being addressed as a memory location. Either flip-flop is conditionally set by an AAB or RW signal from the special field of the microinstruction. Thus, AAB or RW will set the A ADDR FF if T-bus bits 1 through 14 are "0" and ALU0 is "0" (this is the address of the A-register), and will set the B ADDR FF if T-bus bits 1 through 14 are "0" and ALU0 is a "1" (this is the address of the B-register).

3-479. The A ADDR FF and B ADDR FF outputs are sent to the store field decoder circuits on Microinstruction Decoder 1 Card A3. If the conditional microcode AAB is present in the store field of the microinstruction, the false $\overline{\text{AAFF}}$ or $\overline{\text{BAFF}}$ signal (depending upon which addressable flip-flop is set) provides control signals to store the T-bus data into the addressed register.

3-480. The signals are also combined on card A3 to produce the ABF and $\overline{\text{ABF}}$ signals. These signals are used with the COND microcode in the S-bus field of the microinstruction to read the R-bus contents onto the S-bus (RRSB signal) if either flip-flop is set, or to read the T-register contents (SELT and READ signals) onto the S-bus if neither flip-flop is set.

3-481. The $\overline{\text{ABF}}$ signal from card A3 is applied to Microinstruction Decoder 2 Card A4 to set or clear the A/B CLR FF depending upon whether the A- or B-register is addressed, or not. The BAFF signal from card A6 is applied to card A4 to set or clear the A/B SEL FF depending upon whether the B-register is addressed, or not.

3-482. The clear outputs from the A ADDR and B ADDR FFs are "nanded" and applied to the skip field decoder logic and part of the memory protect logic on card A6. If either register is addressed, the "nanded" output from A6U21D will be true. The presence of an AAB microcode in the skip field of the microinstruction and either addressable flip-flop set will cause the next microinstruction to be "skipped". The presence of an NMPV microcode in the skip field of the microinstruction performs a check on the addressed memory location for violation of the protected area of memory. If either the A- or B-register is addressed, the false output from inverter A6U22A prevents the memory protect violation (a false MPV signal) from being generated. If the addressed memory location is outside the protected area, the true output from A6U22A, along with the decoded NMPV microcode and the true ALU15 bit, produces a ROM skip condition. If memory protect is not enabled (MPC signal at pin 13 of A6 is flase) and the addressed memory location is inside the protected area (but is not the A- or B-register), a ROM skip condition will also be generated.

3-483. A/B CLEAR AND A/B SELECT FLIP-FLOP LOGIC.

3-484. The A/B clear and A/B select flip-flop logic, located on Microinstruction Decoder 2 card A4, operates in conjunction with the A and B Addressable flip-flop logic located on Instruction Register Decoder card A6. The A/B clear and A/B select flip-flop logic selects the contents of the A- or B-register (when addressed) to be displayed by the operator panel when the computer enters the halt mode. This prevents the contents of memory location 000000 or 000001 from being displayed, since the operator panel normally provides the control signals necessary to select the contents of the T-register.

3-485. The A/B CLR FF enables the gated A/B SEL FF outputs to provide control signals for the R-bus multiplexer. If either the A Addressable FF or B Addressable FF is set, the A/B CLR FF clears which enables the flip-flop output gates. When the PNLT and CPEN signals become true (these signals become true when the computer enters the halt mode), the SELT signal is inhibited and the $\overline{\text{RBE}}$, RBS1, and RBS2 signals select the register determined by the A/B SEL FF.

3-486. A- AND B-REGISTERS.

3-487. The A- and B-registers, on the arithmetic/logic card, are 16-bit accumulators controlled by the STA, STB, and SAM signals. The STA and STB signals cause the data inputs from the T-bus to be stored in either the A-register or B-register, respectively. The SAM signal allows the data inputs from the T-bus to be stored in the A-register in a parallel manner, if high. If low, the A-register data is capable of being right shifted internally by the use of the SAM signal. The B-register does not have this feature. Any shifting of the B-register data must be done via the arithmetic function generator and shifter under control of signals generated by the microinstructions. Also, the B-register is capable of being loaded in only a parallel manner. These two registers are used as intermediate data storage areas for I/O data transfers and for data manipulations internal to the computer.

3-488. F- AND Q-REGISTERS.

3-489. The F- and Q-registers, on the arithmetic/logic card, are 16-bit accumulators controlled by the STQ, SQM, STOF, and SFM signals. The STQ and STOF signals cause the data inputs from the T-bus to be stored in either the F-register or Q-register, respectively. The SQM and SFM signals allow the data inputs from the T-bus to be stored in the F- and Q-registers, respectively, in a serial or parallel manner. If these signals are low, the data is stored serially. If they are high, the data is stored in parallel. These registers cannot be used directly by software programming methods. However, they are used by the firmware microprograms and can be shifted right or left by the microprograms. The F-register is used as a fence register by the memory protect feature of the computer. For this reason caution must be observed when using any microprogram that uses the F-register; the contents must be saved upon entering the microprogram and must be restored upon exiting the microprogram.

3-490. P-REGISTER.

3-491. The P-register, on the arithmetic/logic card, is a 16-bit program counter which contains the memory address of the next instruction to be fetched. It is initially loaded manually from the front panel. Thereafter, in run mode, its contents are incremented at the start of each execute phase by an INCP (Increment P) signal from the Phase Control logic on Timing and Control card A1. During the execute phase of skip instructions the register may be incremented a second time by an INCP signal from the Skip Carry logic on the timing and control card. During the execute phase of the JMP and JSB instructions, a different address is loaded into the P-register from the Scratch Pad 1 register (SP1). The address in SP1 is either a direct address obtained during the fetch phase or a final indirect address obtained from the T-register during an indirect phase. The transfer from SP1 to the P-register occurs via the S-bus, arithmetic function generator circuits, and the T-bus.

3-492. The control signals for the P-register are CLK, STP, and INCP. The CLK and STP signals are used to store the data from the T-bus into the P-register in a parallel manner. When the CLK signal goes negative (high to low transition) the data will be present at the P-register output lines. The INCP signal is used to increment the P-register. When the carry-in (C2) line is high and the INCP signal is high, the register will be incremented by one when the CLK signal goes high.

3-493. SCRATCH PAD REGISTERS.

3-494. These registers, on the arithmetic/logic card, are 16-bit registers normally used for temporary storage of information during the execution of a microprogram. As with the F- and Q-registers, the four scratch pad registers (SP1, SP2, SP3, and SP4) are accessible only through microprogramming. The T-bus provides the data inputs to these registers and their outputs are directed to the S-bus. Unlike the other registers mentioned, these registers are not capable of storing data from one execute phase to another. If data storage of this type is desired, another scratch pad register must be specified for storing from one execute phase to another.

3-495. The control signals for the Scratch Pad registers are WSP1-4 and RSP1-4. These signals cause the data on the T-bus to be written into the respective register or the data in the respective register to be read out onto the S-bus during the $\overline{\text{CLK1}}$ time of an execute phase.

3-496. R-BUS MULTIPLEXER.

3-497. The four-input R-bus multiplexer is used to select the outputs of one of four registers (A-, B-, F-, and Q-registers) and place this output data on the R-bus. The various registers to be transferred are selected by the configuration of the control signals $\overline{\text{RBE}}$, RBS1, and RBS2. Table 3-18 shows the configurations necessary for selection of the various registers. These control signals are active at the end of $\overline{\text{CLK2}}$ time and remain active until the beginning of the next $\overline{\text{CLK2}}$ time. Therefore, the output from any of the four mentioned registers is available on the R-bus lines for approximately 200 nanoseconds.

Table 3-18. R-Bus Multiplexer Truth Table

REGISTER SELECTED	CONTROL SIGNAL CONFIGURATION		
	RBS1	RBS2	RBE
A-Register	0	0	0
B-Register	0	1	0
Q-Register	1	0	0
F-Register	1	1	0

3-498. ARITHMETIC FUNCTION GENERATOR.

3-499. The arithmetic function generator performs one of eight arithmetic or logical functions on the combined R- and S-bus inputs. If nothing is read onto one of the buses, its state is all-zero, and the specified function essentially operates on only the remaining bus input. The function is specified by the control signals MC, $\overline{INC}$, FN0, FN1, FN2, and FN3. Table 3-19 is the function generator truth table which lists the various logic functions performed for the various control signal configurations.

Table 3-19. Function Generator Truth Table

	RALU	IOR	XOR	NOR	AND	ADD	SUB	DEC	INC
MC	0	1	1	1	1	0	0	0	0
FN0	0	0	0	1	1	1	0	0	1
FN1	0	1	1	0	1	0	1	1	0
FN2	0	1	1	0	0	0	1	1	0
FN3	0	1	0	0	1	1	0	0	1
INC	1	1	1	1	1	1	0	1	0

3-500. SHIFTER AND SHIFT LINKAGE.

3-501. The shifter is comprised of eight multiplexer packs, each controlling two bits of the T-bus. The 16 output bits from the arithmetic function generator are applied to the shifter, which routes each bit onto the numerically corresponding T-bus line unless a shift signal (TBS1 or TBS2) is applied. The various types of shifts (arithmetic, logical, etc.) are enabled by controlling the data bit that is inserted into either the high end (ALX16) or the low end (LSI) of the shifter. These bits constitute the shift linkage logic. This logic takes some combination of three input signals (Flag, Extend, and either ALX16 or LSI), and outputs one bit to either ALX16 or LSI depending on the direction of the shift. The direction of the shift is controlled by the configuration of the TBS1 and TBS2 signals. Table 3-20 is a truth table illustrating the resulting shifts for the various configurations of the TBS1 and TBS2 control signals.

3-502. RFE LOGIC.

3-503. The RFE (Rotate Flag and Extend bits) logic, located on Microinstruction Decoder 2 Card A4, exchanges the contents of the FLAG FF and EXTEND FF upon receiving an RFE signal from the function field decoder.

Table 3-20. Shifter Truth Table

CONTROL SIGNAL	NO SHIFT	RIGHT ONE	LEFT ONE	LEFT FOUR
TBS1	0	1	0	1
TBS2	0	0	1	1

3-504. CPU FLAG LOGIC.

3-505. The flag logic located on Microinstruction Decoder 2 Card A4, controls the state of the Flag FF, which is used by microprograms for temporary storage of a single data bit or status bit. This is not the same flag referred to in the I/O group. The state of the Flag bit may be tested by the skip field decoder logic and, as mentioned above, its content may be exchanged with the EXTEND FF content. (The Flag bit is also used in the shift linkage for implementing the shift and rotate instructions of the basic instruction set.) The Flag FF may be set or cleared by SFLG or CFLG signals from the function field decoder, or an LWF (Link with Flag) microcode may be used to cause the Flag FF to save the bit shifted off either end of a word by the shifter. That is, if shifting left (L1), the Flag will assume the state of ALU15 (which would be lost from the word shifted to the T-bus). Similarly, if shifting right (R1), the Flag will assume the state of ALU0. The LWF microcode also inserts the Flag content into the vacated bit position at the other end of the shifted word.

3-506. EXTEND LOGIC.

3-507. The extend logic, located on Instruction Register Decoder Card A6, controls the state of the EXTEND FF. The bit contained in this flip-flop is accessible to software by way of the shift-rotate and alter-skip groups of instructions. During execution of shift-rotate instructions, the SRG1 and SRG2 microcodes are detected in the special field of the microprogram. These signals, along with the appropriate I-register bits, enable the extend logic to set (or clear) the EXTEND FF depending upon the state of ALU15 or ALU0. The SRG FF in the special field decoder logic allows clearing the EXTEND FF when I-register bit 5 is true (CLE instruction). During execution of the alter-skip group instructions, the ASG1 and ASG2 microcodes are detected in the special field of the microprogram. These signals, along with the appropriate I-register bits, enable the extend logic to set (or clear) the EXTEND FF. The EXTEND FF will be set by a carry out (a false $\overline{COUT}$ signal) from the ALU on card A5, when enabled by an ADDO or INCO microcode in the function field. (These two microcodes cause a true ENOV signal to be applied to pin 83 of card A6.) Also, an ADA/B instruction must be present in the I-register. The microprogram cannot directly set or clear the EXTEND FF; indirectly it may be controlled by rotating with the CPU Flag FF, which is directly controllable (refer to paragraphs 3-503 and 3-505). The RFE and FLAG signals permit transferring the state of the flag bit to the EXTEND FF. In the halt mode, the state of the EXTEND FF may be altered by the EXTEND switch (CMEFF signal) on the operator panel.

3-508. OVERFLOW LOGIC.

3-509. The overflow logic, located on Microinstruction Decoder 2 Card A4, controls the state of the $\overline{\text{OVF}}$ FF. The state of the bit contained in this flip-flop can be controlled by software (STO and CLO instructions) and may be tested for skips (SOS and SOC instructions). The STO and CLO instructions result in true SC1 and STF signals or true SC1 and CLF signals, respectively, to be applied to the overflow logic from I/O Control Card A7 and I/O Buffer Card A8. The SOS and SOC instructions result in true SC1 and SFS signals or true SC1 and SFC signals, respectively, to be applied to the overflow logic from cards A7 and A8. During execution of the microprogram, the $\overline{\text{OVF}}$ FF may be cleared or set by CLO and SOV microcodes present in the function field. The overflow logic may be enabled by a true ENOV signal to check for possible ALU overflow by the ADDO and INCO microcodes present in the function field. ALU overflow normally is tested by comparing ALU15 with bit 15 of the R- and S-buses ("anded"); if a sign change occurs, the $\overline{\text{OVF}}$ FF will be cleared. The overflow bit (OVFF signal) is one of the conditions which may be tested by the skip field decoder logic on card A6. The state of the $\overline{\text{OVF}}$ FF may be altered in the halt mode by the OVF switch (CMOV signal) on the operator panel.

3-510. MEMORY SECTION, DETAILED THEORY.

3-511. FUNCTIONAL DESCRIPTION.

3-512. The 2100A Computer memory section employs core storage units of the conventional coincident-current parallel-readout type. Employment of a single wire for sensing and for write inhibiting permits the use of only three wires through each core, rather than the more usual four wires.

3-513. CORE STACK CONSTRUCTION. Each 4K or 8K core stack is made up of ferrite cores which provide 4,096 or 8,192 word-storage locations. Each word location consists of 17 ferrite cores numbered 0 through 16. Of these, 16 (bits 0 through 15) are used for storing a word, while the remaining core (bit 16) is reserved for the parity bit.

3-514. ORGANIZATION OF DATA. The word locations in each core stack are divided into 4K groups. These groups are referred to as modules. An 8K core stack has a lower module and an upper module. (The terms "lower" and "upper" refer to address assignments, rather than to the physical arrangement of word locations in each core stack.) The octal addresses in each module of each core stack are listed in table 3-21. In the table, core stacks are identified by the reference designation of the sense amplifier card on which they are installed. It will be noted that the lowest address in the table is 00002. Addresses 00000 and 00001 are used for addressing the A-register and B-register, respectively.

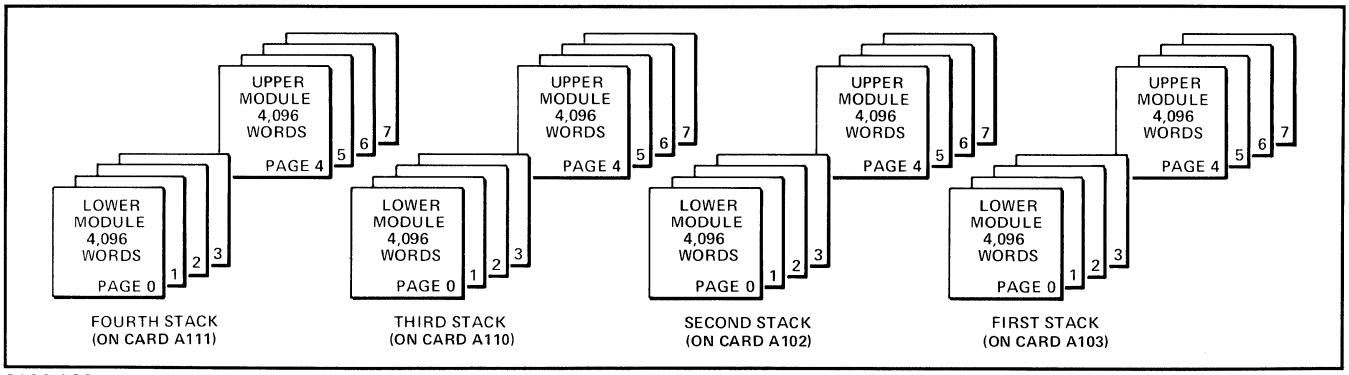
Table 3-21. Stack and Module Address Assignments

CORE STACK	MODULE	
	LOWER	UPPER
A103	00002 thru 07777	10000 thru 17777
A102	20000 thru 27777	30000 thru 37777
A110	40000 thru 47777	50000 thru 57777
A111	60000 thru 67777	70000 thru 77777

3-515. In each module word locations are divided into four pages, each containing 1,024 (decimal) words. The eight pages in each core stack are illustrated in figure 3-22.

3-516. ADDRESSING METHOD. Memory addressing utilizes two address formats. These are described in the following paragraphs.

3-517. Full Address Word. Figure 3-23 shows the address word used by the computer. Bit 15 is the direct/indirect (D/I) bit. The function of this bit is described in a later paragraph. Bits 14 and 13 designate the core stack to be used. Bits 12, 11, and 10 identify the page in the stack. Bits 9 through 0 specify the location within the page. Table 3-22 lists the address range (first and last address) of each page of the four core stacks.



2133-120

Figure 3-22. Core Stack Pages

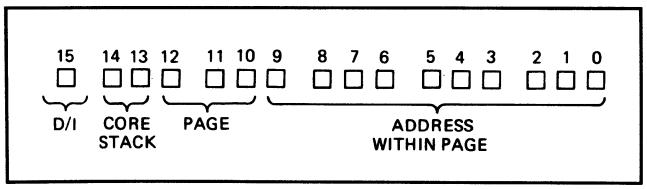


Figure 3-23. Format of Address Word

3-518. Addressing by Instruction Word. Memory reference instructions specify a partial core address. This permits the 16-bit instruction word to include in its structure an operation code as well as a memory address. The format is shown in figure 3-24. Bit 15 is the direct/indirect bit, and bits 14 through 11 constitute the operation code. Bits 9 through 0 identify the address within the page (see table 3-22). The page to be used can be specified in any of three ways, as described below:

a. In the first method, bit 10 of the instruction word (the zero/current bit) is logic 1, and the direct/indirect bit is logic 0. The instruction makes reference to a location in the current page. That is, to the page in which the instruction word itself is located.

b. In the second addressing method, the zero/current bit is logic 0, and the direct/indirect bit is logic 0. The instruction makes reference to page 0 of the core stack on card A103. The octal address is therefore in the range 00002 through 01777, with bits 9 through 0 of the instruction word specifying the low-order 10 bits of the address.

c. The third addressing method used by memory reference instructions is indirect addressing. In this type of operation the zero/current bit of the instruction word can be logic 0 or logic 1; the direct/indirect bit is logic 1. The instruction acquires a 16-bit word from page 0 or the current page, as determined by the zero/current bit. If bit 15 of the acquired word is logic 0, bits 14 through 0 of the word are used as a full address word for carrying out the memory reference operation specified by the instruction word. By this means any word-location in memory can be referenced. If bit 15 of the acquired word is logic 1, another 16-bit word is acquired, using the word-location specified by the first word read from memory. The new word, in turn, is used as an address word. This process continues until a 16-bit word is obtained in which bit 15 is logic 0. This full address word is then used by the instruction to carry out its particular memory reference operation.

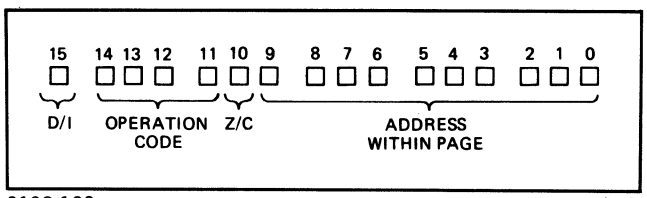


Figure 3-24. Format of Memory Reference Instruction Word

3-519. MEMORY READ OPERATIONS. When a word is to be read from the core stack assembly, its address is first transferred from the Scratch Pad 1 register and placed in the 15-bit M-register (refer to figure 3-2). The address is then forwarded to the memory circuits, the word is acquired from the specified word-location, and the T-register receives the word read. This operation is performed for each of the three basic types of readout operations, which are as follows:

a. Readout of a word for display by the operator panel DISPLAY REGISTER.

b. Readout of an instruction word to be executed by the computer.

c. Readout of an operand which will be used by an instruction.

3-520. The memory readout operation leaves "0's" in the 17 ferrite cores at the addressed location. (This is referred to as destructive readout.) Therefore, it is necessary to rewrite the word in these cores. This is done immediately after the memory readout has taken place, and occurs without manual intervention by the operator. Immediately after the readout operation the M-register still indicates the addressed location, and the memory timing circuits restore the word in memory by attempting to store logic 1 in each bit position of the addressed word-location. However, the inhibit circuits prevent this in the ferrite cores that originally contained logic 0. The word that was read out is in the T-register, and from this word the inhibit circuits determine the cores that must remain in the logic 0 state.

3-521. Readout for Display. When a word (memory data) is to be displayed in the DISPLAY REGISTER, the computer must be stopped because the controls which bring about readout for display are disabled when the computer is running. The readout for display is brought about by pressing the M switch, setting the address of the wanted memory data in the DISPLAY REGISTER switches, and pressing the MEMORY DATA switch. When the MEMORY DATA switch is pressed, the address of the memory data is loaded into the M-register and a memory cycle is initiated causing the memory data in the addressed location to be transferred through the T-register to the DISPLAY REGISTER and displayed.

3-522. When the MEMORY DATA switch is pressed, the memory address decoding circuits in the memory section decode the contents of the M-register, and select the appropriate driver/switch circuit to drive the specified core location. The word in the core location is sensed by the sense amplifiers, and placed in the T-register. The word in the T-register is then gated onto the S-bus lines and then to the I/O bus lines. Finally, the word is stored in the display register flip-flops, and the contents are available for visual inspection in the DISPLAY REGISTER lamps.

3-523. Instruction Word Readout. The second type of memory readout occurs when the computer acquires an instruction word to be performed. At the beginning of the execution of the previous instruction the P-register was incremented. When the previous instruction's execution was completed, and the fetch phase of the next instruction was set, the P-register contents were transferred to the M-register establishing the memory address of the next instruction. The fetch phase continues by transferring the memroy data of the addressed location into the T-register. The T-register data is then used as the next instruction. The T-register data is transferred to the I-register and thence to the ROM mapper to establish the starting address of the ROM microroutine for the instruction to be executed.

3-524. A word acquired from memory during the fetch phase is treated as an instruction word. Words acquired from memory during the other phases are not treated as instructions but as data or addresses. This is the distinguishing feature between words treated as data and words treated as instructions.

Table 3-22. Core Storage Addresses

STACK	MODULE	PAGE	ADDRESS RANGE (OCTAL)	ADDRESS WORD (BINARY)															
				D/I	ADDRESS RANGE (BINARY)														
					STACK		PAGE			ADDRESS WITHIN PAGE									
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A103	Lower	0	00002	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
			01777	0/1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
A103	Lower	1	02000	0/1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
			03777	0/1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
A103	Lower	2	04000	0/1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
			05777	0/1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
A103	Lower	3	06000	0/1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
			07777	0/1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
A103	Upper	4	10000	0/1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
			11777	0/1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
A103	Upper	5	12000	0/1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
			13777	0/1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
A103	Upper	6	14000	0/1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
			15777	0/1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
A103	Upper	7	16000	0/1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
			17777	0/1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A102	Lower	0	20000	0/1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
			21777	0/1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
A102	Lower	1	22000	0/1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
			23777	0/1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
A102	Lower	2	24000	0/1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
			25777	0/1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
A102	Lower	3	26000	0/1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
			27777	0/1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
A102	Upper	4	30000	0/1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
			31777	0/1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1
A102	Upper	5	32000	0/1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
			33777	0/1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
A102	Upper	6	34000	0/1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
			35777	0/1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
A102	Upper	7	36000	0/1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
			37777	0/1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 3-22. Core Storage Addresses (Continued)

STACK	MODULE	PAGE	ADDRESS RANGE (OCTAL)	ADDRESS WORD (BINARY)															
				D/I	ADDRESS RANGE (BINARY)														
					STACK		PAGE			ADDRESS WITHIN PAGE									
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A110	Lower	0	40000	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			41777	0/1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1
A110	Lower	1	42000	0/1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
			43777	0/1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
A110	Lower	2	44000	0/1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
			45777	0/1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
A110	Lower	3	46000	0/1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
			47777	0/1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
A110	Upper	4	50000	0/1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
			51777	0/1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
A110	Upper	5	52000	0/1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
			53777	0/1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
A110	Upper	6	54000	0/1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
			55777	0/1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
A110	Upper	7	56000	0/1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
			57777	0/1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A111	Lower	0	60000	0/1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
			61777	0/1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
A111	Lower	1	62000	0/1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
			63777	0/1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
A111	Lower	2	64000	0/1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
			65777	0/1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
A111	Lower	3	66000	0/1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
			67777	0/1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
A111	Upper	4	70000	0/1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
			71777	0/1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
A111	Upper	5	72000	0/1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
			73777	0/1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
A111	Upper	6	74000	0/1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
			75777	0/1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
A111	Upper	7	76000	0/1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
			77777	0/1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Core stacks are identified by the reference designation of the card on which they are mounted.

3-525. Operand Readout. The third method of addressing a core memory location is used by memory reference instructions. Instructions of this type acquired an operand from memory and perform an arithmetic or logic operation using the operand. The operand word is acquired either by direct addressing or by indirect addressing, as designated by bit 15 of the instruction word. If bit 15 is logic 0, the operand is acquired from memory by direct addressing. If the bit is logic 1, indirect addressing is employed.

3-526. When direct addressing is used, the computer enters the execute phase after acquiring the instruction word during the fetch phase. During the execute phase, the operand is acquired from memory and acted upon in accordance with the type of instruction being performed.

3-527. When direct addressing is used, the operand must be obtained either from page 0 of the first core stack, or

from the page in which the instruction word is located. Bit 10 of the instruction word identifies the page to be used, logic 0 indicating page 0 and logic 1 the current page.

3-528. When the instruction word is acquired from memory, it is placed in the T-register (figure 3-2). The T-register data is gated onto the S-bus, passed unchanged through the arithmetic logic, and loaded into the I-register. If it is determined that this instruction is a memory reference group instruction, bits 0 through 9 of the I-register are transferred to the Scratch Pad 1 register for future reference. This complete process takes place near the end of the fetch phase. Bits 14 through 10 of the instruction word remain unchanged and designate the core stack, module, and page to be referenced. The operand is thus obtained from the page designated by bit 10 of the instruction word. If bit 10 of the instruction word indicates page 0, bits 15 through 10 of the scratch pad 1 register will be cleared, the page 0 of the first core stack is referenced.

3-529. After the I-register is loaded and end-of-phase (EOP) is detected, the computer enters the execute phase and the P-register is incremented by one. The use then made of the scratch pad 1 data depends on the type of instruction being performed.

3-530. At the beginning of the fetch phase (PH1A), the M-register is loaded with the address of the next instruction. This is done by passing the P-register contents through the arithmetic logic (figure 3-1) into the M-register.

3-531. With indirect addressing, the instruction word is acquired from memory and placed in the T-register as before. However, because bit 15 of the instruction word is logic 1, the computer enters the indirect phase after the completion of the fetch phase. During the indirect phase the referenced word is acquired from page 0 or the current page and placed in the T-register as previously described. However, the word acquired is not treated as an operand to be operated on by the instruction, nor is it handled as an instruction word. Instead, it is forwarded to the M-register through the Scratch Pad 1 register and treated as an address word. This time, bits 14 through 0, rather than 9 through 0, are routed through the scratch pad 1 register to the M-register. Consequently, any address in any core stack can be referenced.

3-532. When the word is acquired from memory during the indirect phase, it is placed in the T-register in the normal way. Bit 15 of the word is then checked to determine whether or not another indirect addressing operation is to be performed. If bit 15 is logic 1, the new word is treated as an address word, and another indirect phase operation is performed. The computer continues to perform indirect phase operations until a word is acquired in which bit 15 is logic 0. The computer then enters the execute phase, and the word acquired during the last indirect phase is treated as an operand address.

3-533. MEMORY WRITE OPERATIONS. Memory write operations are very similar to memory read operations. During the processing of a memory reference instruction, such as Store the A-register (STA), bits 9 through 0 of the instruction word (brought from memory to the T-register during the fetch phase) are routed from the T-register to the M-register via scratch pad 1 register during the fetch phase (figure 3-2). This establishes the memory address of the data to be manipulated during the execute phase of the memory reference instruction. During the execute phase, the word to be written into memory is gated onto the T-bus and into the T-register. A clear-write memory cycle is initiated and during the read portion of this cycle the data in the addressed memory location is inhibited from being gated into the T-register. During the write portion of the memory cycle the new data currently in the T-register is gated into the addressed memory location via the inhibit driver circuits thus destroying the old data in that location and replacing it with new data. The same execute phase operations take place when new data is entered from the operator panel.

3-534. ADDRESSING BEYOND AVAILABLE MEMORY. If, in the course of operating a program, a reference is made to a location beyond the installed capacity of the computer there will be no parity error indication and a NOP instruction (000000) will be obtained from memory and processed. The M- and P-registers will be incremented in the usual manner and another NOP will be extracted and processed. This procedure will continue until the M- and P-registers finally indicate location zero (000000), at which time whatever is contained in the A-register will be used as an instruction word and processed. The results of this operation are unpredictable.

3-535. BLOCK DIAGRAM ANALYSIS.

3-536. ADDRESS SELECTION. When memory reading or writing is performed, the address decoding logic on the X-Y driver/switch card examine bits 11 through 0 of the M-register to determine the word-location to be referenced. These 12 bits can indicate any octal address from 0000 through 7777, corresponding to the 4,096 locations in the lower or upper module of a core stack assembly.

3-537. Bits 11 through 6 of the M-register indicate the Y drive-line to be used (see figure 3-25). These bits are decoded to yield their octal equivalent, in the form of two octal digits. Bits 11, 10, and 9 give the most-significant-digit (MSD), and bits 8, 7, and 6 give the least-significant-digit (LSD). Together, these two digits identify one of the 64 Y drive-lines in the core stack assembly.

3-538. Bits 5 through 0 of the M-register are decoded in a manner similar to that used for bits 11 through 6, to yield a 2-digit octal number identifying the X drive-line.

3-539. Bits 14 through 12 of the M-register are also examined in the memory section to identify completely the memory location to be referenced. Bit 12 identifies the module, logic 0 indicating the lower module and logic 1 the upper module. Bits 13 and 14 designate the core stack.

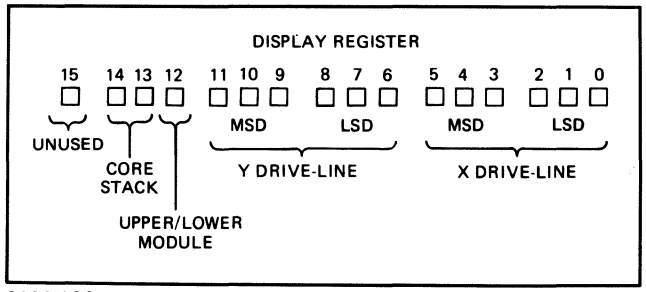


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Figure 3-25. Significance of M-Register Contents

3-540. Y-Line Selection. Figure 3-26 illustrates in block diagram form the selection of Y-lines in core stack A103A1, the basic core stack containing octal addresses 00002 through 17777. The decoders, drivers, and switches shown in the illustration are on card A104, and the core stack is on card A103. For other core stacks, different cards are used for the Y-line selection circuits and for the core stack itself.

3-541. The $\overline{\text{MOD0/1}}$ signal in figure 3-26 results from decoding bits 14 and 13 of the M-register (figure 3-25). If the two bits are both logic 0, indicating the basic core stack, the $\overline{\text{MOD0/1}}$ signal becomes false. This signal is furnished to X-Y driver/switch card A104, covering addresses 00002-17777. If bits 14 and 13 of the M-register are 01, 10, or 11 respectively, the $\overline{\text{MOD2/3}}$, $\overline{4/5}$, or $\overline{6/7}$ signal becomes false, and X-Y driver/switch card A101, A109, or A112 is selected. The $\overline{\text{MOD}}$ signal, when false, serves as an enable for the binary-to-octal decoders on the X-Y driver/switch card which receives the signal.

3-542. When Y-line current is required, the MRTY signal becomes true (for readout), or the MWTY signal becomes true (for writing). Upon occurrence of one of these signals, bits 11 through 9 of the M-register are decoded to furnish an octal equivalent, referred to as the Y most-significant-digit (MSD). (See figure 3-26.) As a result, one of the signals YD7 through YD0 becomes true (for readout), or one of the signals YC7 through YC0 becomes true (for writing). M-register bits 8 through 6 are similarly decoded to determine the Y least-significant-digit (LSD), resulting in one true signal in the group YB7 through YB0 (for readout), or one true signal in the group YA7 through YA0 (for writing).

3-543. As a result of the decoding process, a pulse is furnished to one of the eight drivers, and another pulse to one of the eight switches. A total of 64 combinations is possible. The selected driver furnishes a negative signal to the core location for readout, or a positive signal for writing. The selected switch provides a ground path.

3-544. When the selected driver and selected switch receive an input pulse, electron current flows from the driver to the switch (when reading), or from the switch to the driver (when writing). This current flows through the addressed Y-line, which is identified by a 2-digit octal number corresponding to the Y MSD and Y LSD. Current does not flow through other Y-lines because the remaining switches do not furnish a path to ground and the drivers do not furnish a voltage.

3-545. The Y-lines pass through the ring-shaped ferrite cores shown in figure 3-26. Each core in the illustration represents the 17 cores of a word location in the core stack. It will be noted that every Y-line in figure 3-26 is shown passing through two cores, representing two 17-bit storage locations. One of these locations is in the upper module of the core stack, and the other is in the lower module. An X-line (described later) passes through the same cores, and determines which of the two locations will be used. For one of the locations, the X-line current aids the Y-line current. For the second location, the X-line current opposes the Y-line current. The storage location used is the one in which the currents aid. By reversing the direction of the X-line current, the other 17-bit location can be selected. It is this technique which permits the use of an 8K core stack.

3-546. In addition to the two 17-bit words indicated by each core in figure 3-26, each Y-line also passes through the ferrite cores for other words. Because the cores for these words are not traversed by the selected X-line, readout or writing does not take place.

3-547. The diodes in figure 3-26 are near the core stack on card A103. During readout, the top diode in each pair permits electron flow from the driver to the switch, and the bottom diode offers a high-resistance path to minimize current flow through it. When writing is performed, the roles of the two diodes are reversed, and electron flow is from the switch to the driver.

3-548. Each switch in figure 3-26 has two outputs. These are designated CC (common cathode) and CA (common anode) in accordance with the diode electrodes to which they connect. Each CC or CA designation is followed by the identifying number of the associated switch, 7 through 0.

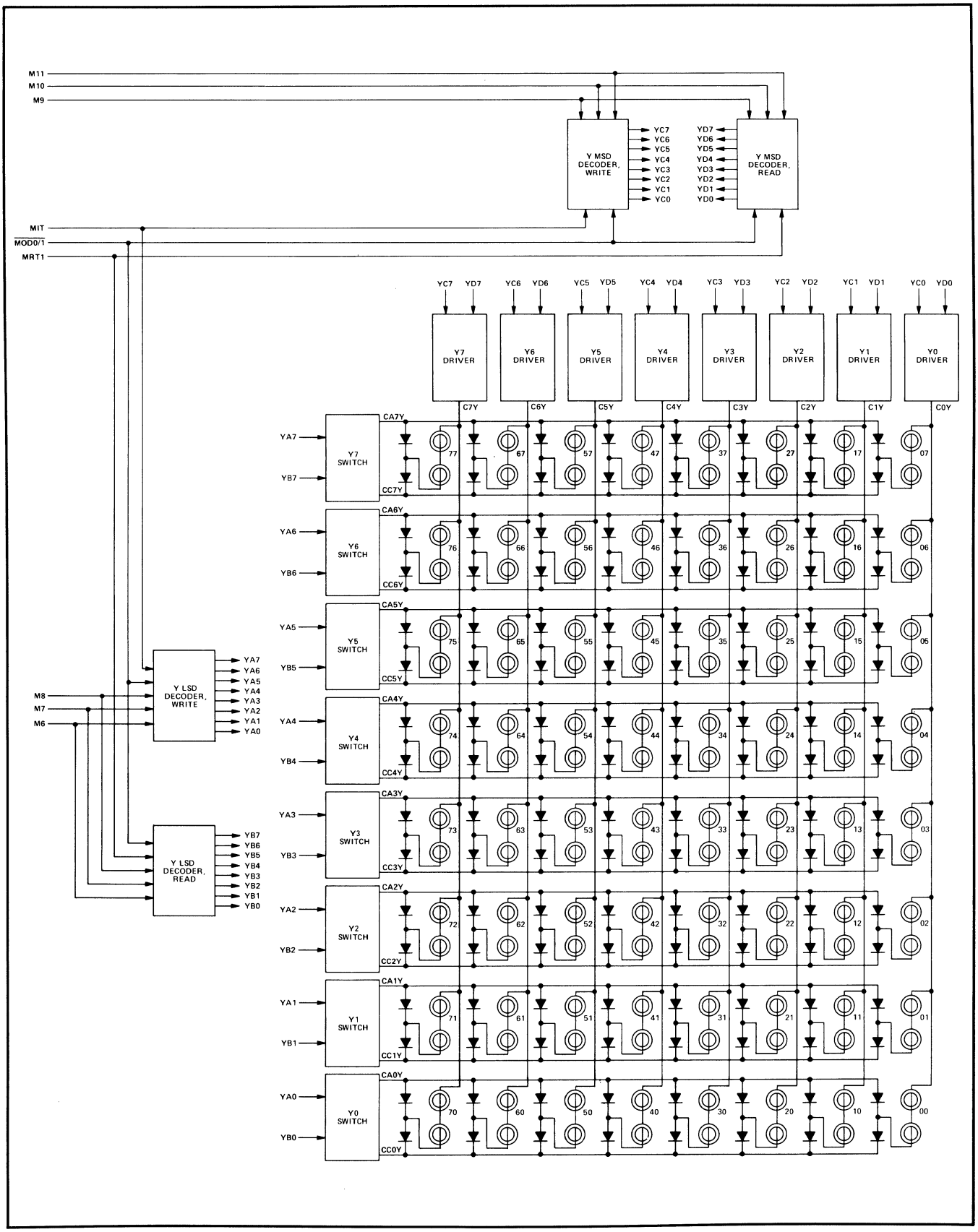
3-549. The drivers each have one output, identified by the letter C (core), followed by the identifying number of the driver.

3-550. It is important to note that the diode matrix shown in figure 3-26 does not represent a plane of the core stack. The matrix in figure 3-26 has an 8 x 8 configuration, while the core-plane matrix is 64 x 64. Figure 3-27 shows a core-plane matrix, and indicates the manner in which the Y- and X-lines are connected. The numbered Y-lines in figures 3-26 and 3-27 correspond.

3-551. X-Line Selection. The X-line circuits for core stack A103A1 are shown in figure 3-28. They differ from the Y-line circuits in the following respects:

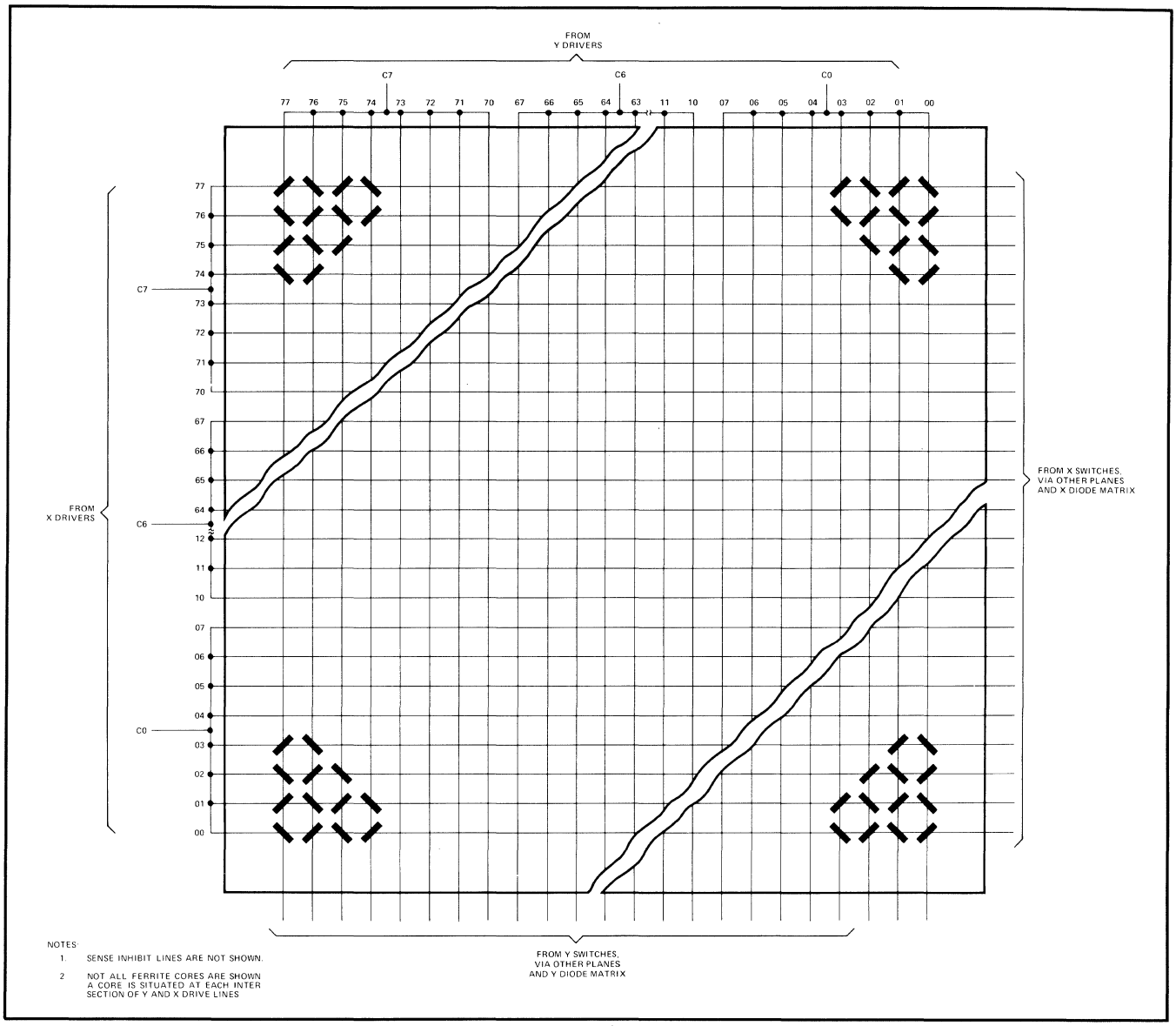
a. The binary-to-octal decoders receive bit 5 through 3, or 2 through 0, of the M-register.

b. Instead of the MRTY or MWTY strobe pulse, either an XT1 or an XT2 pulse is furnished to each decoder.



2107-105

Figure 3-26. Y-Line Selection Circuits, Core Stack A103A1, Block Diagram



2107-106

Figure 3-27. Core Plane

c. For the cores in the upper module, X-line read or write current is in the reverse direction from that in the lower module. For the Y-lines, read or write current is the same in both modules.

3-552. As pointed out earlier, a reversed-current technique with the X-lines permits the selection of a word in either the lower or upper module, using only a single pair of X and Y drive lines. The current reversal is brought about by the XT1 and XT2 pulses. If bit 12 of the M-register is logic 0, indicating the lower module, current flow for the X-lines, during readout or writing is the same as for the Y-lines. If bit 12 is logic 1, indicating the upper module, X-line current flow is reversed.

3-553. Table 3-23 shows the direction of current flow for all operating combinations. The table is applicable to all core stacks in the computer.

Table 3-23. Electron Flow for 8K Memory Configuration

MODULE	Y-LINE ELECTRON FLOW	
	READ	WRITE
Lower*	Driver to switch	Switch to driver
Upper	Driver to switch	Switch to driver
MODULE	**X-LINE ELECTRON FLOW**	
	READ	WRITE
Lower	Driver to switch	Switch to driver
Upper	Switch to driver	Driver to switch

* In a 4K memory configuration, this electron flow is reversed.

3-554. The X MSD and X LSD decoders in figure 3-28 are identified by the words "read/write" or "write/read". This terminology indicates the function of the decoders for lower and upper module operations, respectively. For example, the "X MSD decoder, read/write" is used for readout in the lower module, or for writing in the upper module.

3-555. OPERATION OF MEMORY SECTION. The following paragraphs explain the operation of the memory section, making use of the block diagram in figure 3-29. The discussion describes reading and writing in core storage location 05270, with general comments regarding operations in other storage locations. Of the 17-bit word read or written, only bit 0 is dealt with here. Reading and writing of other bits is identical, except that a separate inhibit driver and sense amplifier is used for each bit.

3-556. Core Stack. The core stack is made up of two sets of core planes, each set consisting of 17 planes and making up the lower or upper module. The core planes each contain 4,096 ferrite cores, and each plane stores one bit of a 17-bit word. The planes are numbered 0 through 16 in accordance with the bit position in the word, with bit 15 being the high-order bit. Bit 16 is the parity bit.

3-557. The core stack utilizes a folded construction, and has eight or nine core planes in each physical plane. Figure 3-29 illustrates this construction, with the core stack shown partly unfolded to reveal internal wiring in the core stack.

3-558. Lower Module Read Operations. The following paragraphs describe a typical memory read operation, using address 05270 (octal). Figure 3-29 illustrates the operation, and figure 3-30 shows the timing relationships.

3-559. The core stack and module to be used, and the Y-line and X-line employed, are identified by positions 14 through 0 of the M-register (figure 3-31). The number in this portion of the register is one of the following:

a. The address of the next instruction.

b. The address of an address word (if the next phase is indirect phase).

c. The address of an operand (if the next phase is execute phase).

3-560. As figure 3-31 indicates, the address within each page consists of part of the Y-line designation, and the entirety of the X-line designation. As explained earlier, this arrangement permits a memory reference instruction to specify an address in the current page or in page 0, using bits 9 through 0 of the instruction word. These bits, initially in the T-register, are transferred to the M-register (figure 3-2). The remainder of the M-register either remains unchanged (to obtain an operand from the current page), or is cleared (for page 0).

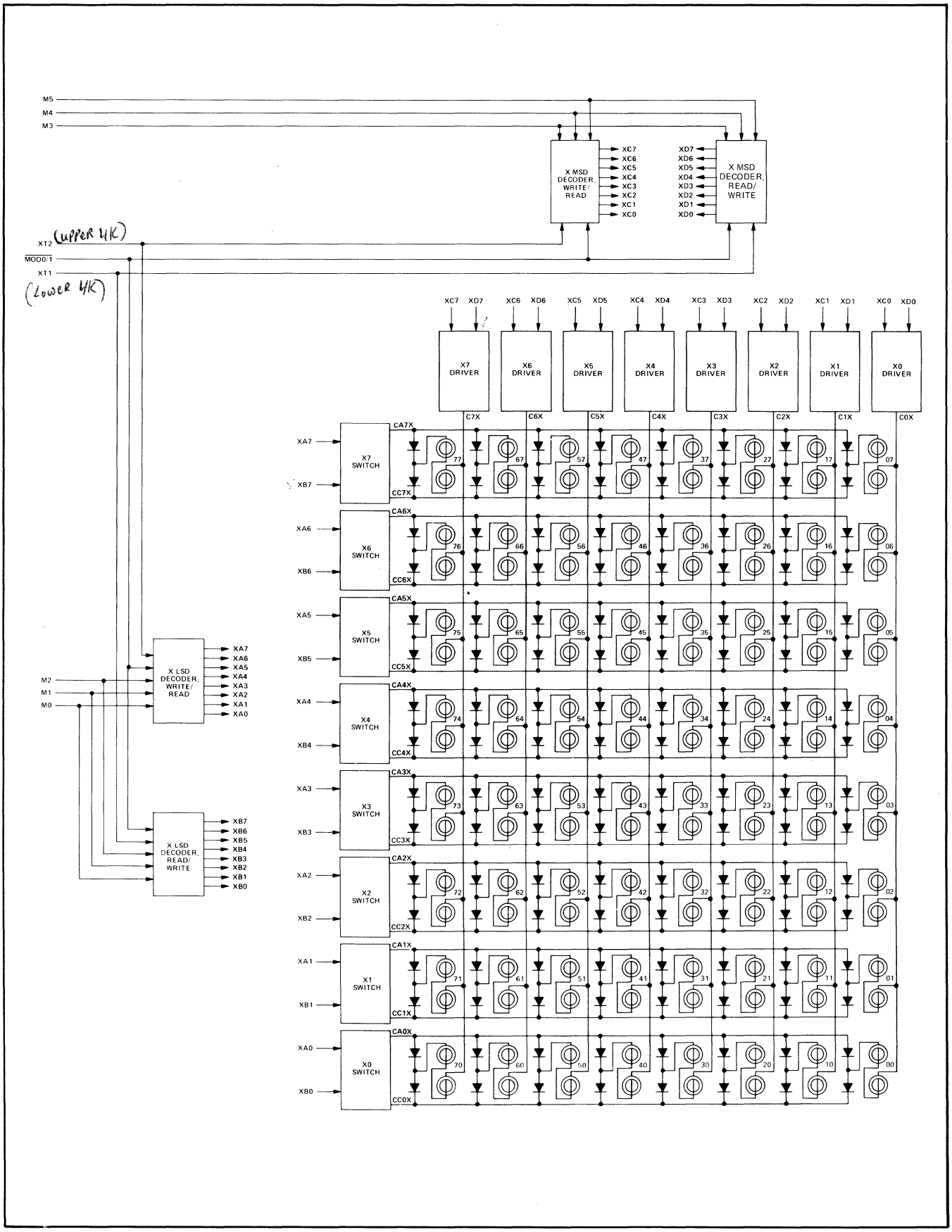
3-561. Bits 14, 13, and 12 of the M-register are examined to determine the stack and module to be used. This operation is dealt with in a later paragraph. Bits 11 through 0 are forwarded as bits MR11 through MR0 to the X and Y decoders (figure 3-29).

3-562. As table 3-22 shows, address 05270 is in the lower module of the core stack on card A103, and is therefore in module 0. (All locations within a core stack indicated by a 5-digit octal address. The MSD of that address indicates the core stack and module, two modules for each core stack. The modules in the four core stacks thus are numbered from 0 through 7.) Since the address being referred to is in module 0, the $\overline{\text{MOD0/1}}$ signal becomes false, and the X and Y decoders on X-Y driver/switch card A104 are enabled. The Y most-significant-digit (MSD) is 5 octal and the Y least-significant-digit (LSD) is 2 octal. Therefore, the Y MSD and Y LSD read decoders furnish a YD5 and YB2 pulse upon occurrence of the MRTY pulse (figure 3-29). As table 3-23 and figure 3-29 indicate, electron current flows through the Y-line from the Y2 switch to the Y5 driver. Approximately 100 nanoseconds later the XT1 signal becomes true, and X-line current flows from the X7 driver to the X0 switch. At this time the ferrite cores in the addressed location change magnetic state if they are storing logic 1. As a result, the sense/inhibit winding passing through each of these cores senses the change and generates a pulse, indicating readout of logic 1. After readout, all cores at the addressed location are in the logic 0 state.

3-563. The sense/inhibit windings are shown in figure 3-29 for bit-plane 0 in the lower module. For clarity, the sense/inhibit windings for other bit planes have been omitted from the illustration. It will be noted that each sense winding consists of two halves; this serves to minimize electrical noise induced in the winding by half-selected cores. An inhibit driver is connected to the junction of the two half windings. During readout this connection to the inhibit driver is essentially an open circuit, and therefore plays no part in the operation.

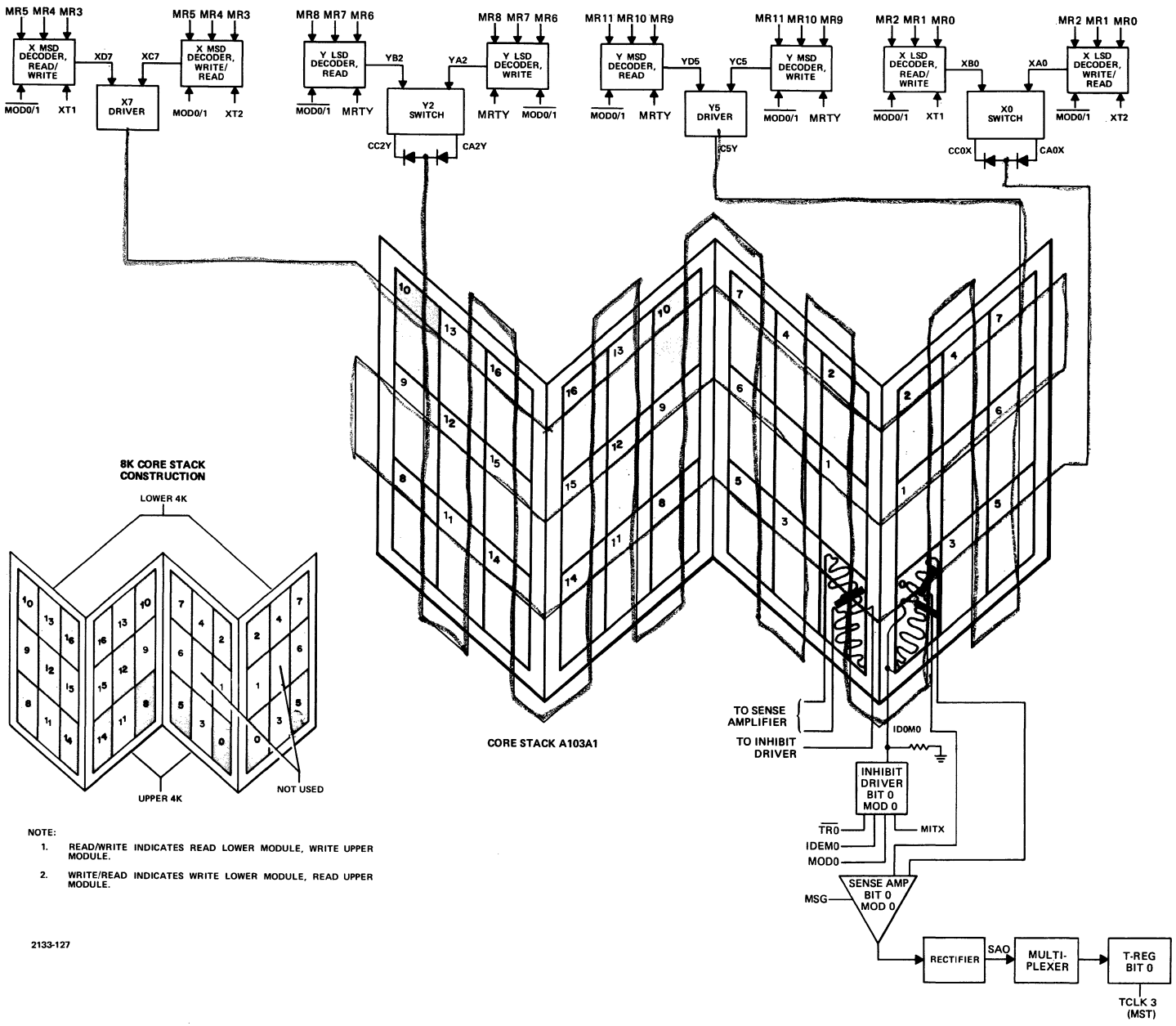
3-564. The two ends of the sense/inhibit winding for bit 0 in module 0 connect to the sense amplifier for bit 0 module 0. This amplifier consists of a differential amplifier. When logic 1 is read from the module, at least 20 millivolts appears across the two ends of the applicable sense/inhibit winding. This voltage is applied to the two inputs to the differential amplifier. For logic 0, the voltage is under 10 millivolts. The differential amplifier for the module not in use receives only a slight noise potential.

3-565. The output signal of the differential amplifier is rectified and furnished as the SA0 signal. Rectification is required because the sense/inhibit winding passes alternately across the bit plane in two directions, and therefore can traverse the selected ferrite core in either direction. As a result, the pulse induced in the sense/inhibit winding for logic 1 can be of either electrical polarity. The rectification process ensures that regardless of the polarity of the signal furnished to the differential amplifier, the SA0 signal is positive when a logic 1 is read. Essentially, the rectifier inverts the signal if it is of the wrong polarity.



2107-107A

Figure 3-28. X-Line Selection Circuits, Core Stack A103A1, Block Diagram



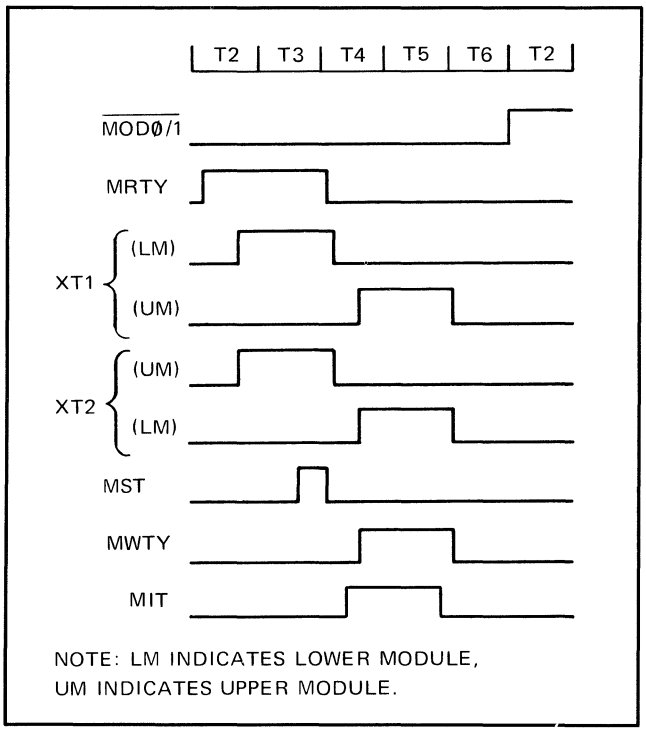
NOTE:

1. READ/WRITE INDICATES READ LOWER MODULE, WRITE UPPER MODULE.
2. WRITE/READ INDICATES WRITE LOWER MODULE, READ UPPER MODULE.

2133-127

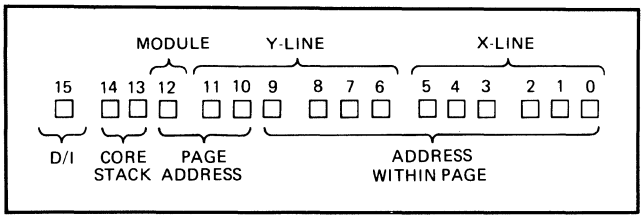
2133-127

Figure 3-29. Memory Section, Partial Block Diagram



2133-128

Figure 3-30. Y-Line and X-Line Current, Timing Diagram



2133-129

Figure 3-31. M-Register Contents 05270

3-566. Each core stack has its own sense amplifiers and bit rectifiers. The SA0 signal from each stack is "or" tied on the computer backplane with the corresponding signal from all other stacks.

3-567. The TCLK3 signal clocks the SA0 output into position 0 of the T-register. Figure 3-30 shows that the entire read operation takes approximately 360 nanoseconds.

3-568. Lower Module Write Operations. Memory section writing is similar to reading. Address selection is the same, except that the Y-line is activated by the MWTY signal rather than the MRTY signal (see figure 3-29). As a result, current flows in the opposite direction through the Y-line. Similarly, the X-line is activated by XT2 instead of XT1, and again the direction of current flow is reversed. The Y-line and X-line currents attempt to place each ferrite core at the addressed location to logic 1. However, the sense/inhibit winding prevents this for each bit position in which there is a logic 0 in the T-register. In figure 3-29 the $\overline{TR0}$ input to the inhibit driver controls this function for bit position 0. The center-tapped connection of the inhibit driver permits current flow in the correct direction through the two halves of the sense/inhibit winding, allowing cancellation of the Y-line currents if logic 0 is required.

3-569. The abbreviation ID0M0 in figure 3-29 stands for inhibit driver bit 0, module 0. Inhibit current flows only in the module being addressed.

3-570. Upper Module Read Operations. Upper module read operations are the same as for the lower module, except that the X-line current is reversed and a different sense amplifier is used. In figure 3-29 it can be seen that the XT2 signal activates the X MSD and X LSD decoders for reading. This results in current flow through the X-line in the direction used for writing in the lower module. Figure 3-30 shows that the timing of XT2 is changed during upper module read operations, resulting in readout during the first part of the memory cycle. This leaves the remainder of the memory cycle for writing.

3-571. Upper Module Write Operations. As with upper module reading, upper module writing employs reverse current (same direction of current flow as during lower module readout) in the X-line. The XT1 pulse activates the X MSD and LSD decoder and the timing of this pulse is delayed as shown in figure 3-30. Inhibit current is in the same direction as for the lower module.

3-572. LOGIC CIRCUIT ANALYSIS.

3-573. The following discussion makes use of the simplified logic diagram (figure 3-32) and the schematic diagrams in the 2100 Computer Diagrams Manual (part no. 02100-90003). Memory readout and write operations are described for a 4K memory configuration on Core Stack/Sense Amplifier Card A103. The reference designations used on figure 3-32 are not the same as those used for equivalent circuits on the schematic diagrams.

3-574. ADDRESSING CIRCUITS. The address to be referenced is indicated in bits 14 through 0 of the M-register, which is situated on Data Control Card A107. The output of this register is forwarded to the X- and Y-decoders on X-Y Driver/Switch Card A104 (M-register bits 11 through 0) and to the memory module decoder circuit on card A107 (M-register bits 14 through 12). The X- and Y-decoder circuits select the X-Y driver/switch circuits corresponding to the referenced address. The memory module decoder circuit selects the core stack and module (upper or lower) within the core stack. These decoder circuits are binary-to-octal decoders (one true output, 0 through 7 (octal), corresponding to the binary input received).

3-575. The $\overline{MOD0/1}$, $\overline{MOD2/3}$, $\overline{MOD4/5}$, or $\overline{MOD6/7}$ signal is furnished to the X-Y driver/switch cards. When one of these signals becomes false it activates the card to which it is furnished; the other X-Y driver/switch cards remain inoperative. The false input to the selected circuit card serves as an enable to the X-line and Y-line decoders A104U17 through A104U24.

3-576. The eight drive-line decoders on the selected card require, in addition to a false signal at the E2 ($\overline{\text{MOD0/1}}$) input, a true signal at E1 (MRTY or MWTY) in order to become operative. The E1 input is used to control the timing of the X-line and Y-line currents (figure 3-30), and to select the decoders required. For each memory read or write operation, two Y-line decoders and two X-line decoders are used. These decode the Y and X MSD and LSD. That is, they furnish the octal equivalent of a 3-bit binary input. Table 3-24 identifies the decoders for each core-stack module. The two MSD decoders in use select a driver each, and the two LSD decoders select a switch each.

3-577. To provide an output, binary-to-octal decoder A107U96 (memory Module Decoder) requires a true enable at pin 4 and a false enable at pin 3. Pin 4 is connected to the PON signal, which is true whenever the computer power is on and stable. Pin 3 is connected to the RESET signal, which is true whenever the INTERNAL PRESET switch on the operator panel is pressed.

3-578. Similarly, to provide an output, the X- and Y-decoders on the X-Y driver/switch card must have a true enable at pin 4 and a false enable at pin 3. Pin 4 is connected to a memory timing signal, which activates the circuits at the proper time. Pin 3 is connected to the module select signal, $\overline{\text{MOD0/1}}$, which activates the circuits that control the locations within the desired module.

3-579. The outputs from the memory module decoder circuit select the proper core stack and module by producing the MOD(X), MOD(X)/(X), and $\overline{\text{MOD(X)/(X)}}$ signals. The signal used for each core stack and module are routed to and activate the X-Y driver/switch, sense amplifier, and inhibit driver circuits which control the addressed core stack and module. In this way only the circuits for the addressed core stack and module are activated.

3-580. From table 3-24 it is seen that the Y decoders for readout of module 0 are integrated circuits U24 and U22 on circuit card A104. The next octal digits in the address, MR11 through MR9 and MR8 through MR6, are the Y MSD and Y LSD. Figure 3-32 indicates that for these inputs the YD(X) and YB(X) signals are furnished by the YD and YB decoders on card A104 when readout is performed. The YD(X) and YB(X) signals are true for the duration of the MRTY signal. When writing is conducted, the MWTY signal is produced rather than the MRTY signal. As a result, decoders YC and YA furnish signals YC(X) and YA(X).

3-581. The X-line decoders function in a manner similar to that of the Y-line decoders. However, for the lower module of a core stack the XT1 signal selects the two X decoders used for reading, and the XT2 signal selects the two X decoders for writing. In the upper module, the role of these two signals is reversed, as is their timing.

3-582. DRIVERS AND SWITCHES. The decoder outputs are applied to the drivers and switches. In the example illustrated in figure 3-32, the YA and YC decoder output signals YA(X) and YC(X) are applied to their respective switch and driver transformers during the read operation (signal MRTY is true). As a result, the corresponding transistors are driven from the cutoff condition into saturation. The C(X)Y output of the driver circuit then becomes positive and the CC(X)Y output of the switch circuit becomes negative causing current to flow from the switch circuit, through the core stack via the Y-axis line, to the driver

Table 3-24. Y-Line and X-Line Decoders

MODULE ADDRESSED	Y MSD DECODER		Y LSD DECODER		X MSD DECODER		X LSD DECODER	
	READOUT	WRITE	READOUT	WRITE	READOUT	WRITE	READOUT	WRITE
0	A104U24	A104U23	A104U22	A104U21	A104U18	A104U17	A104U20	A104U19
1	A104U24	A104U23	A104U22	A104U21	A104U17	A104U18	A104U19	A104U20
2	A101U24	A101U23	A101U22	A101U21	A101U18	A101U17	A101U20	A101U19
3	A101U24	A101U23	A101U22	A101U21	A101U17	A101U18	A101U19	A101U20
4	A109U24	A109U23	A109U22	A109U21	A109U18	A109U17	A109U20	A109U19
5	A109U24	A109U23	A109U22	A109U21	A109U17	A109U18	A109U19	A109U20
6	A112U24	A112U23	A112U22	A112U21	A112U18	A112U17	A112U20	A112U19
7	A112U24	A112U23	A112U22	A112U21	A112U17	A112U18	A112U19	A112U20

NOTES:

1. The module addressed is indicated by bits MR14, MR13, and MR12.
2. The Y MSD is indicated by bits MR11, MR10, and MR9.
3. The Y LSD is indicated by bits MR8, MR7, and MR6.
4. The X MSD is indicated by bits MR5, MR4, and MR3.
5. The X LSD is indicated by bits MR2, MR1, and MR0.

circuit. Each driver and switch consists or two halves, of which one-half is used at a time. The required direction of current determines the half to be utilized. Approximately 400 milliamperes of current will flow through the Y-axis line which is one-half of the current required to magnetize a core.

3-583. The XB and XD decoder output signals XB(X) and XD(X) are applied to their respective switch and driver transformers during the read operation (signal XT1 is true). The corresponding transistors are driven from cutoff condition into saturation. The C(X)X output of the driver circuit then becomes negative and the CA(X)X output of the switch circuit becomes positive causing current to flow from the driver circuit, through the core stack via the X-axis line, to the switch circuit. Approximately 400 milliamperes of current will flow through the X-axis line which constitutes the other one-half of the current required to magnetize a core.

3-584. By tracing the direction of current flow through the illustrated cores (see figure 3-32) it can be seen that the current through both the X-axis line and Y-axis line flows in the same direction through only one location (2 cores shown). This is known as "coincidence" of current. With 400 milliamperes of current flowing through both the X- and Y-lines there are 800 milliamperes flowing in the same direction through the cores of one location. The force of the flux generated by the 800 milliamperes of current is additive and sufficient to cause the cores of the "coincident" (referenced) location to be magnetized in one polarity. Since the read operation is being discussed, this polarity is the logic zero polarity.

3-585. During this read operation when the cores of the referenced location are magnetized, if a core does in fact change its polarity this change is sensed by the sense line and sense amplifier circuits and sets the T-register flip-flop for that core indicating a "one" was stored in that core. The output from the reset-side of the T-register flip-flop causes the inhibit driver circuit for the core to remain off when the timing signal MIT becomes true. (The action of the sense amplifier and inhibit driver circuits will be discussed later.)

3-586. For the write operation, the YB and YD decoders are activated by the write timing signal (MWTY) and produce signals YB(X) and YD(X). The write timing signal (XT2) activates the XA and XC decoders which produce the signals XA(X) and XC(X). These signals are applied to their respective switch and driver circuits turning them on and reversing the flow of current through the X- and Y-lines. This reversal of current flow causes the cores in the referenced location to reverse their magnetic polarity ("one" magnetic polarity) unless the inhibit line is active in which case the individual core will remain in its logic zero magnetic polarity.

3-587. SENSE AMPLIFIERS. The sense amplifiers, located on cards A103, A102, A110, and A111, amplify the output from the sense/inhibit lines, and produce a logic 1 or logic 0 signal of standard voltage level. Each card has thirty-four sense amplifiers, two sense amplifiers for each core (bit) plane. One amplifier senses the output from the sense/inhibit line in the lower module of the core stack and the other amplifier senses the output from the upper module. The outputs from the two sense amplifiers "or" together. The seventeen output bits from each card "or" with the corresponding outputs from the other cards.

3-588. Figure 3-32 shows a sense amplifier circuit for a core in a location in the lower module of a core stack. When the MOD0 and MSG signals become true the output of the "nand" gate to which these signals are connected becomes false. This false signal is connected to the base of transistor A103Q20, turning it on. When A103Q20 turns on it causes the base of the constant voltage source transistor A103Q19 to go less negative thus turning A103Q19 on. Truning A103Q19 on places a stable ground potential at the junction of the 562-ohm and 100-ohm resistors. This constant potential is connected to the base of transistor A103Q18 through the 100-ohm resistor and is sufficiently positive to turn A103Q18 on. This constant potential being applied to the base of A103Q18 causes it to conduct in a very stable manner and provide a stable current source to the emitters of differential amplifier transistors A103Q13 and A103Q16. This type of amplifier furnishes an output voltage determined by the potential differences between the two inputs to the amplifier. In the present instance, these inputs are the two extreme ends of the center-tapped sense/inhibit line. The inhibit driver circuit connected to the center tap is not turned on during the read operation when the sense amplifier is in use so it is essentially an open circuit. The 200-ohm resistor also connected to the center tap establishes a ground-oriented reference point at the center tap; the two extreme ends of the sense/inhibit line therefore exhibit opposite changes in polarity when a voltage is induced in the line by readout of one of the 4,096 ferrite cores in the bit plane. One end of the sense/inhibit line therefore becomes negative with respect to ground, and the other becomes positive. The peak of the voltage pulse is at least 20 millivolts if logic 1 is read, or less than 10 millivolts for logic 0.

3-589. The transformer and diodes in the balun module serve a purpose during the inhibit function, described later. These components are paralleled by two 100-ohm resistors, and have no significant effect during readout because current in the sense/inhibit line is relatively small.

3-590. If logic 0 is read out, the bases of transistors A103Q13 and A103Q16 experience only a slight change in potential. The voltage at the collectors of these two transistors remains almost unchanged, and transistors A103Q14 and A103Q17 maintain the cut-off condition resulting from the identical potential at the base and emitter of each transistor. Emitter-follower A103Q15 experiences no appreciable change in input, and the SAX output signal is

logic 0. The multiplexer output Q(X), activated by the $\overline{\text{READ}}$ signal, is also logic 0, and the T-register flip-flop for that bit is clocked to the clear condition by the T-register clock pulse TCLK(X) at MST time.

3-591. If logic 1 is read from the bit plane, transistors A103Q13 and A103Q16 experience a relatively large difference in potential between their bases. One transistor increases conduction, and the collectors of these transistors change potential. Depending on the direction in which the sense/inhibit line traverses the selected core in the bit plane, either A103Q13 or A103Q16 could conduct more heavily than the other transistor of the pair. It is the function of A103Q14 and A103Q17 to act as a rectifier to ensure that when logic 1 is read, the input to A103Q15 becomes more positive. Assuming A103Q13 increases conduction during readout, the collector of A103Q13 becomes less positive. As a result, the base of A103Q17 becomes less positive. Also, the emitter of A103Q17 becomes more positive as a result of decreased conduction through A103Q16 and its 1.6k ohm collector resistor. Transistor A103Q17 conducts and a positive voltage is applied to the base of A103Q15. On the other hand, if the bit plane output voltage is the reverse of that described, A103Q14 conducts, again applying a positive potential to A103Q15. In either case emitter-follower A103Q15 generates a true SA(X) signal and upon occurrence of the TCLK(X) signal, logic 1 is placed in the T-register flip-flop for that bit position.

3-592. Transistors A103Q13, A103Q16, and A103Q18 of figure 3-32 are part of a transistor array. On the schematic diagrams for the 4K and 8K configurations these transistors are presented in two different ways. The 8K configuration presents them as a differential amplifier logic symbol which include two differential amplifier circuits, one for the lower module and one for the upper module. The 4K configuration presents them as individual transistors connected as a differential amplifier. Again, there are two differential amplifier circuits per array. The circuits of all bit positions of the 16-bit word (bit 0 through 15) operate identically to that explained above except the parity bit (bit 16). The parity circuits is explained in paragraph 3-577.

3-593. INHIBIT DRIVERS. As noted earlier, the inhibit drivers prevent the writing of logic 1 in designated bit positions of a core storage location. In doing this, the inhibit driver causes an approximate 400-milliampere current to flow through the sense/inhibit line of the appropriate bit plane; this takes place when Y-line and X-line current flows during the write operation. The Y-line and X-line currents, each 400-milliamperes, flow through the addressed core in the opposite direction from that of the inhibit current. Thus the effective current through the core is 400-milliamperes, and since this is not sufficient to magnetize the core, the core remains in the logic 0 state in which it was placed during the read operation.

3-594. Figure 3-32 shows an inhibit driver circuit for a bit position in the lower module of core stack A103A1. In the illustrated example, a lower module operation is under consideration. When addressing a lower module, bit 12 of the M-register is logic 0 and as a result the MOD0 signal is true. With the occurrence of the MIT signal, the "and" gate on Inhibit Driver Card A105 furnishes a true output. If the bit position of the T-register contains logic 0, the $\overline{\text{TR(X)}}$ signal is true and the "nand" gate furnishes a negative-going signal to the pulse transformer, which causes a positive pulse to be felt at the base of transistor A105Q21 for the duration of the MIT signal. Current flows from the "nand" gate output through the primary of the pulse transformer and the 51.1-ohm current limiting resistor to +4.85 volts. The positive pulse transferred to the base of transistor A105Q21 turns it on thus allowing current to flow from the ground connection of the balun module on card A103, through the balun module diodes and the two portions of the transformer, through the two portions of the sense/inhibit line for the bit plane, through transistor A105Q21 on Inhibit Driver Card A105 and the 22-ohm resistor on Inhibit Driver Load Card A106, to +20 volts. The transformer in the balun module serves the equalize current in the two portions of the sense/inhibit line. The currents in the two circuits tend to differ because of the differing number of half-selected cores in each path. An increase or decrease of current in one winding of the balun transformer produces a like effect in the other winding, thereby minimizing current imbalance. The diodes in the balun module clip voltage spikes, preventing damage to the balun module transformer or the differential amplifier. The balun module resistors decrease the "Q" of the circuit to prevent oscillation and to furnish surge protection. The 200-ohm resistor connected between the inhibit driver line and ground serves as a termination resistor for the sense/inhibit line, which has transmission line characteristics.

3-595. The 22-ohm resistor on card A106 serves to limit current in the circuit. At the start of the inhibit signal, the 22-ohm resistor is bypassed by the 2000-picofarad capacitor; this allows rapid buildup of current in the circuit to overcome the inductance resulting from the cores and wires. The 100-microfarad and 1.0-microfarad capacitors perform a decoupling function to minimize the change in potential on the +20 volt line resulting from the increased voltage drop along the +20 volt line and in the +20 volt source, due to the increased current drawn by the inhibit circuit.

3-596. Inhibit current flows 100 nanoseconds longer than the duration of the MIT signal. This signal is active during the same time as the MWTY and XT2 signals but has a slightly shorter duration. The MWTY and XT2 signals control the Y-line and X-line currents, respectively, during the write operation. Thus, the inhibit current flows throughout the same time as, but in opposition to, the X- and Y-drive line currents.

3-597. The inhibit function does not affect the sense amplifier because the amplifier does not receive the MSG signal required to turn the amplifier on. As a result, during

the write operation, the inputs to the amplifier are essentially open circuits as far as loading the sense/inhibit line is concerned.

3-598. At the termination of the inhibit current pulse, transistor A105Q21 on the inhibit driver card is turned off. The 121-ohm resistor provides a path for the current caused by the changing magnetic field in the secondary on the inhibit driver transformer. The diode connected to the emitter of A105Q21 prevents the inhibit line from ever going more than 20 volts negative due to the collapsing field of the transformer and the inhibit line protecting Q21 from excess voltage.

3-599. If the output of the T-register bit position under discussion contained logic 1 when the write operation took place, the $\overline{TR(X)}$ signal would be false, the inhibit driver circuit would not be turned on, and no inhibit current would flow through the inhibit line for that core plane.

3-600. The circuits for all bit positions of the 16-bit word (bits 0 through 15) operates identically to that explained above except the parity bit circuits (bit 16) explained in paragraph 3-577.

3-601. PARITY. The condition of bit 16 (parity bit) of the computer word is monitored and stored by the parity circuits on Data Control Card A107. The operation of this bit is the same as all other bits within the memory circuits. Where the operation differs is from the output of the sense amplifier circuit for bit 16 (signal SA16) to the input of the inhibit driver circuit for bit 16 (signal $\overline{TR16}$). The SA16 signal, instead of being connected to the input of the multiplexer, is connected to another group of circuits. These circuits monitor the parity bit, and whether or not the number of logic 1 bits in the T-register (bits 0 through 15) is odd or even. The output signals generated by these circuits are the parity error signal (LPE) and the input signal ($\overline{TR16}$) to the bit 16 inhibit driver circuit.

3-602. The SA16 signal enters Data Control Card A107 at pin 71 and is passed through two inverters. The output of the first inverter is connected to reset-side of the parity bit flip-flop (PB FF). The output of the second inverter is connected to the set-side of the parity bit flip-flop. This connection causes the sense amplifier output, when applied to the parity bit flip-flop, to be in the proper time relationship with the other memory bits which must propagate through the multiplexer. If the SA16 signal is true, the parity bit flip-flop will be set when the TCLK1 signal goes false. When this flip-flop is set, its output pins 5 and 6 go true and false, respectively. The true output from pin 5 is connected to "and" gate A107U54B the output of which then goes true, causing light-emitting diode A107CR4 to be forward biased and turned on. The true output from pin 5 is also connected to "and" gate A107U82A where the T-register is checked for an even number of logic 1 bits.

3-603. If an even number of logic 1 bits does exist in the T-register, and parity bit flip-flop combination, the LPE signal at pin 78 of the data control card goes true. The LPE signal is connected to I/O Buffer Card A8 and causes the parity error interrupt and generates the PEH signal, which causes the parity error lamp on the operator panel to light. The false output from pin 6 of the parity bit flip-flop is connected to "and" gate A107U82B where the T-register and parity bit flip-flop combination are checked for an odd number of logic 1 bits. The false output from pin 6 is also connected to the input of "nand" gate A107U101B. This circuit generates the proper parity for each location in core memory. When data is read out of a memory location during a read-write ($\overline{READ}$ signal true) memory cycle, the condition of the parity bit is stored in the parity bit flip-flop and transferred to the "nand" gate A107U101B where it is tested. If the input signal to A107U101B is true, the $\overline{TR16}$ signal will be true at pin J1-31 of the data control card causing the inhibit driver circuit to be activated and cause a logic 0 to be written back into the parity core of the addressed location during the write operation of the memory cycle.

3-604. If the input signal to A107U101B is false, the $\overline{TR16}$ signal will be false and a logic 1 will be written into the parity core. When new data is to be written into a memory location from the operator panel or some I/O device, the new data is placed in the T-register and a check is made for an odd or even number of logic bits in this register. The result of this check is transferred to "nand" gate A107U101C as the Σ EVEN signal is false causing the $\overline{TR16}$ signal to go false. This keeps the inhibit driver circuit turned off and a logic 1 will be written into the parity core of the addressed location during the write operation of the memory cycle.

3-605. PROTECTIVE CIRCUITS. The PON signal applied to the memory module decoder circuit on the Memory Data Control card becomes true after all operating voltages are furnished to the computer circuits; the signal remains true until power shut-down. This signal is the enable signal for the memory module decoder. Therefore the memory module decoder remains disabled until the PON signal becomes true. This assures that the memory circuits will remain disabled until power is stable throughout the computer.

3-606. I/O SECTION DETAILED THEORY.

3-607. GENERAL.

3-608. The I/O structure (see figure 3-33) of the 2100A Computer system consists of the I/O devices, their respective interface cards and interconnecting cables, I/O control card A7 (which contains the interrupt system control and address logic), and I/O Buffer Card A8 (which contains the I/O instruction decoder, I/O buffers, and I/O time period generator). The I/O section of the computer card cage consists of 17 printed circuit card slots: 14 for I/O interface cards and one each for the I/O control card, I/O Buffer Card and the optional direct memory access (DMA) card. Some I/O devices require only one interface card, while other I/O devices require two interface cards to interface the external device to the computer.

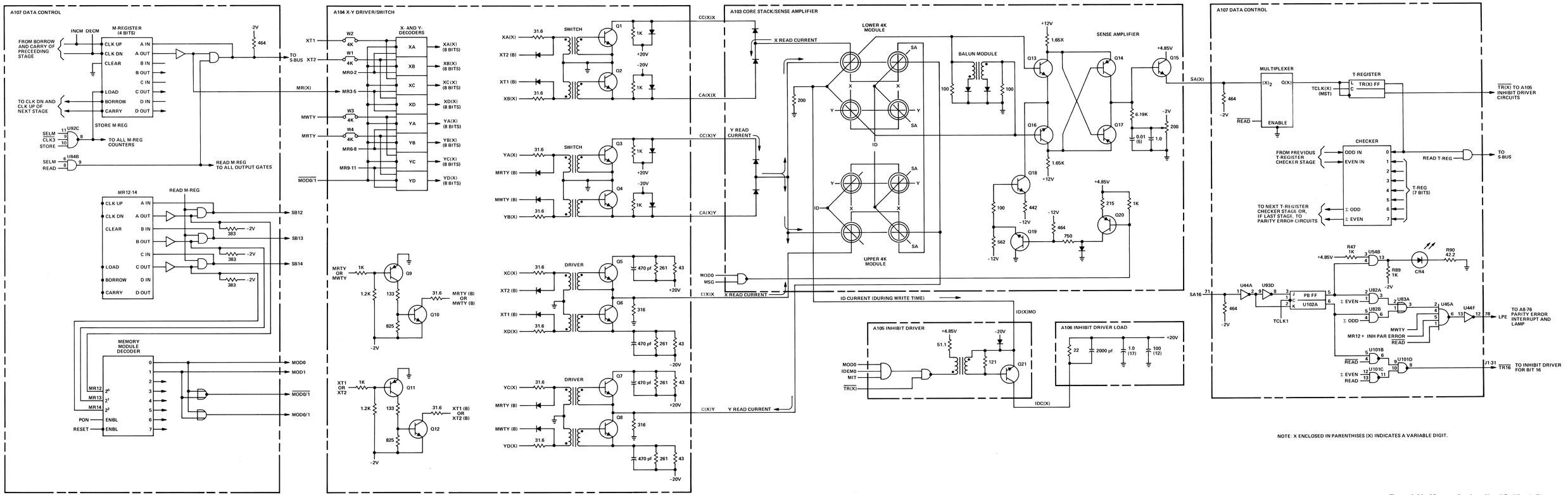


Figure 3-32. Memory Section, Simplified Logic Diagram

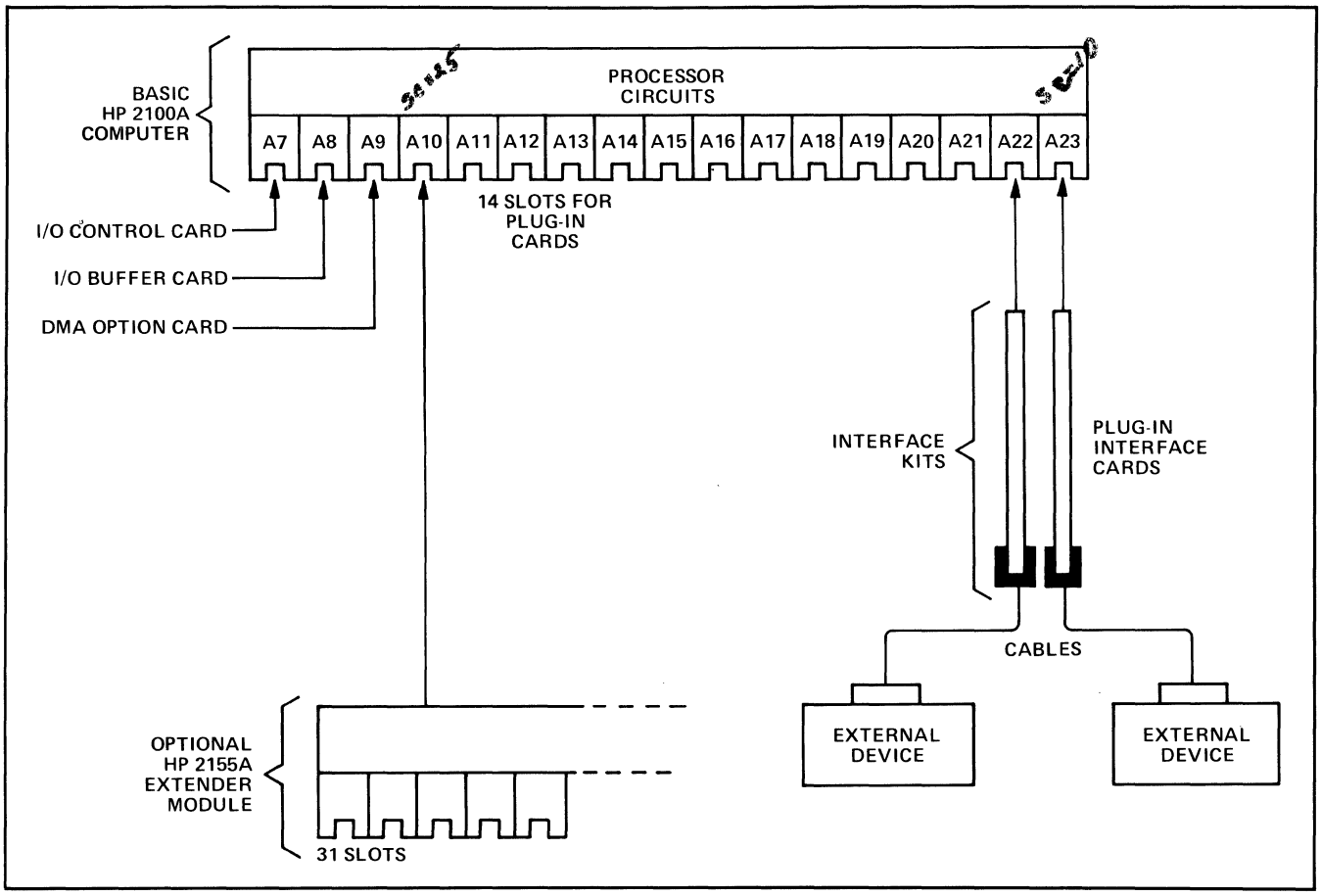


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Figure 3-33. Input/Output Structure

3-609. The I/O Buffer and I/O Control Cards also contain special functions which operate via the I/O section. These special functions are memory protect interrupt, parity error interrupt, power fail interrupt, and the flag and flag buffer logic of the DMA option. Functional operation of the special functions is discussed under "SPECIAL COMPUTER FUNCTIONS" (refer to paragraph 3-145).

3-610. Functionally, the I/O structure allows the computer to select and communicate with each of the interface cards through the I/O control and address logic and through direct bus wiring. The I/O structure also provides a means by which I/O devices can interrupt the computer program in order to be serviced by the computer. When more than one device requests an interrupt, the computer processes the requests on a priority basis.

3-611. The number of I/O interface cards in the system is expandable to 45 or to 56 with the use of the HP 2155A I/O Extender or the multiplexed I/O option, respectively. Interface cards and cables necessary for a complete hook-up of each I/O device are provided by respective HP interface kits. Interface kits and I/O devices are ordered separately.

3-612. I/O SECTION CONTROL ELEMENTS.

3-613. GENERAL. Figure 3-34 illustrates the main elements of the computer system concerned with the control of input/output operations. All elements shown are contained in the computer mainframe except for the external devices. Although the R-, S-, and T-buses are represented as single lines in figure 3-34, each bus is actually 16 individual lines. Also, interface arrangements are shown for only two external devices, one input and one output, where as many as 14 devices may be used with the standard model and up to 56 with the multiplexed I/O option. The elements illustrated process all input/output operations in two ways, as follows:

a. Process input/output instructions from the computer.

b. Process interrupt requests from the external devices.

3-614. INPUT/OUTPUT INSTRUCTIONS. Input/output instructions from memory via the T-register are first stored in the I-register and applied to the ROM CONTROL portion of the control section (see figure 3-34). The appropriate microroutine in the ROM program then sup-

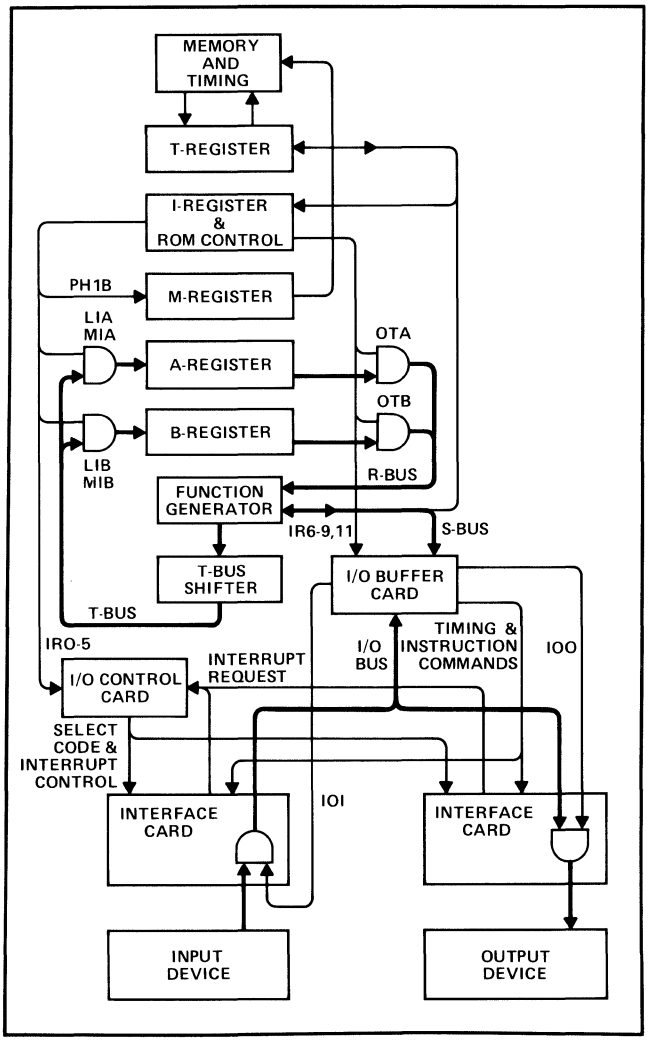

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Figure 3-34. Input/Output Operations Block Diagram

plies control signals to various elements of the arithmetic/logic and input/output sections to transfer data to, or from, the I/O device or to enable decoding of flag and control instructions by I/O Buffer Card A8. These instructions are also applied to the I/O group decoder logic (on the I/O buffer card) where they are translated into appropriate control and flag signals and to the I/O select code decoder logic where they are translated into appropriate select code control signals. The control and flag signals are routed to various interface cards as determined by the select code. The control and flag signals can be used to set or clear the control and flag FFs on the interface cards, and test their set and clear conditions. Each interface card slot has been permanently assigned to an individual select code through computer wiring. This allows the select code from the I-register to individually address each interface card, and its respective I/O device, on a priority basis.

3-615. The IOI (I/O input) signal strobes all interface cards for input data as a result of a load into A (LIA), load into B (LIB), merge into A (MIA), or a merge into B (MIB) instruction. Only the data from the interface card addressed by the select code is enabled. The data is strobed by the IOI signal onto the I/O bus, then onto S-bus. From there it is transferred via the function generator and T-bus shifter (to alter or combine the data) to the A- or B-register. The particular register which will receive the data is determined by the control signals generated by the ROM micro-instruction decoder circuits.

3-616. The IOO (I/O output) signal, which is the result of an OTA (output from A) or an OTB (output from B) instruction, is also applied to the interface cards. This signal, when combined with the select code from the I-register, strobes data from the I/O-bus into the appropriate interface card and I/O device. (Data had previously been placed on the I/O-bus from the A- or B-register as a result of the OTA or OTB instruction.)

3-617. INTERRUPT REQUESTS. If a specific instruction to the I/O control card has at some previous time enabled the interrupt system, an external device may then request an interrupt to the computer program at any time. To request an interrupt, an external device applies an interrupt request signal, via the interface card, to the I/O control card. The I/O control card determines the address of the interrupting device and causes an interrupt of the main computer program. This is done by forcing the M-register to be set (via the microroutine for phase 1B, the interrupt fetch phase) to a memory location corresponding to the address, or select code, of the interrupting device. (The memory locations corresponding to interrupt addresses are more commonly called "trap cells".) Following phase 1B, the phase 3 (the execute phase) is set and the computer executes the instruction contained in the "trap cell". Generally, this will be a jump to a service subroutine (JSB) instruction. The subroutine will prepare and/or accept input data from the external device or apply output data from the computer to the external device. Upon completion of service, the subroutine causes a return to the proper location in the main computer program. Refer to paragraphs 3-643 through 3-677 for a detailed description of the interrupt system.

3-618. INTERFACE CARDS.

3-619. PURPOSE. The interface cards provide channels through which data is transferred between the computer and the input/output devices, and provide control (via computer commands) of the input/output device operation. An interface card contains flip-flops for temporary storage of data that is transferred to or from the computer. The number of buffer flip-flops on a particular interface card depends on the type of device connected to it. Other logic circuitry on the interface card also depends on the device to which it is connected. Certain devices are capable of interrupting the computer program, while for others this capability is not necessary; certain devices require control signals for movement of tape while others do not, and timing requirements for some devices must be provided on the interface card. In some cases more than one interface card is required for an external device. Interface cards are

provided as part of each interface kit ordered. For detailed information on a particular interface card, refer to the applicable interface kit manual, which is also included in each interface kit.

3-620. LOGIC ELEMENTS. The typical logic elements found on most interface cards are shown in figure 3-38. Included are the standard interrupt logic and data buffer. A discussion of these logic elements is given with the discussion of the operation of the computer interrupt circuits in paragraphs 3-643 through 3-677.

3-621. PIN ASSIGNMENTS. One end of each interface card has 86 printed-circuit paths, 43 on each side of the card. This end of the card plugs into a computer slot connector to transfer signals to and from the computer. It is also keyed to prevent incorrect insertion. The circuit path positions correspond to the pin positions of the slot connector. Odd-numbered pins 1 through 85 are on one side of the card as shown in figure 3-35, and even-numbered pins 2 through 86 are on the other side of the card. Pins 1 and 2 are directly opposite each other on the card. Pin assignments for this end of the card are identical for all interface cards to permit the placement of any card in any of the input/output slots of the computer.

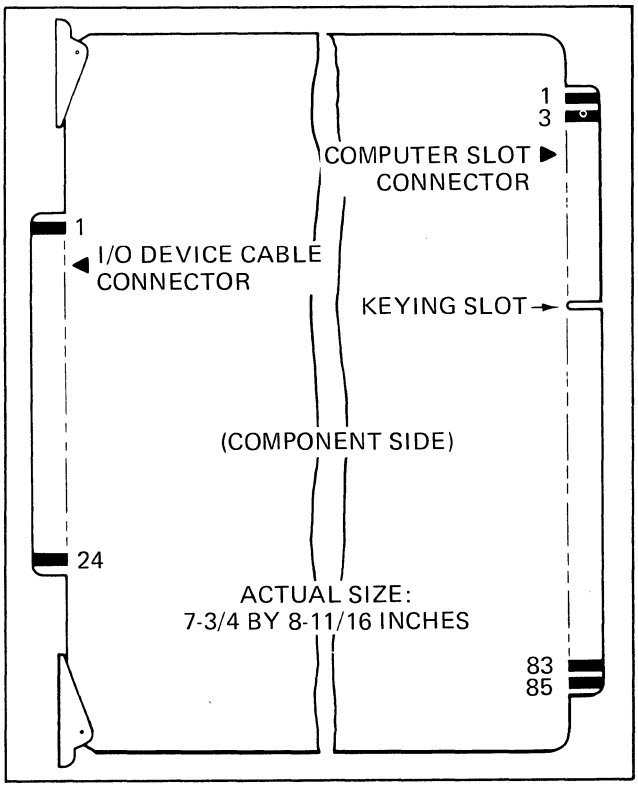

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Figure 3-35. Interface Card Connectors

3-622. The other end of the interface card has 48 printed-circuit paths, 24 on each side of the card. The plug connector of the interconnecting cable to the input/output device plugs onto this end of the card to transfer signals to and from the device. The circuit-path positions correspond to the pin positions of the plug connector. Pins 1 through 24 are on one side of the card as shown in figure 3-35, and consecutively-lettered pins A through BB (with letters G, I, O and Q intentionally omitted) are on the other side of the card. Pins 1 and A are directly opposite each other on the card. Also on this end of the card are two extractor handles to aid in the removal of the computer slot.

3-623. Refer to table 3-25 for a list of the pin connections and signals between the interface cards and the slot connectors. Although this table lists all of the pin assignments and signals between the cards and the slot connectors, an individual interface card may not necessarily use all signals. Pin assignments and signals between an interface card and its input/output device is provided in each interface kit manual.

3-624. I/O TERMINATOR CARD.

3-625. The I/O Terminator Card (A16), which plugs into I/O slot 16, is used to terminate the signal lines from the computer to the interface card slots when less than eight interface cards are installed. The card contains 34 resistors which are connector to the -2 volt line. The other end of each resistor is connected to a signal line to eliminate any transient noise generated by these lines in the backplane wiring of the computer.

3-626. I/O TIMING.

3-627. I/O TIME PERIOD GENERATOR. The I/O time period generator, located on I/O Control Card A7, is a five-stage ring counter which generates I/O time periods T2 through T6. Since the ring counter is clocked by the CLK3 signal, it is not affected by "freeze" conditions. Not only are the I/O time period signals used for gating the I/O signals, they are also used to initiate the memory timing sequence, and to synchronize CPU timing with I/O timing.

3-628. I/O INSTRUCTION TIMING. When I/O instructions are encountered in the user program, a "freeze" is initiated to synchronize CPU timing with I/O timing. The first microinstruction in the microroutine for the particular I/O instruction being executed contains an IOG1 microcode in the special field. When IOG1 is detected by the special field decoder circuits on Instruction Register Decoder Card A6, the resulting IOG1 signal causes a freeze until I/O time T2. This holds the first microinstruction in the ROM Instruction Register until the end of time T2. The remaining three microinstructions are executed during times T3, T4, and T5, respectively.

3-629. The IOG1 signal also sets the IOGM FF on I/O Control Card A7 at the end of time T2, generating a true IOGE signal from time T3 until the end of time T6. The IOGE signal enables the I/O group decoder and I/O violation circuits on I/O Buffer Card A8 and the addressed interface card (if no I/O violation is present). The I/O group decoder circuits decode certain Instruction Register bits during this time and the resulting I/O signals are gated, as necessary, by the appropriate I/O time period.

Table 3-25. Interface Card-to-Computer Pin Connections

PIN	SIGNAL MNEMONIC AND DEFINITION	PIN	SIGNAL MNEMONIC AND DEFINITION
1	GND: Ground	2	GND: Ground
3	PRL: Priority Low	4	FLGL: Flag signal, Lower Select Code
5	SFC: Skip Flag Clear (Skip next instruction if Flag FF is reset)	6	IRQL: Interrupt Request, Lower Select Code
7	CLF: Clear (reset) Flag FF	8	IEN: Interrupt Enable
9	STF: Set Flag FF	10	IAK: Interrupt Acknowledge
11	T3: Machine phase time T3 to I/O	12	SKF: Skip Flag (Skip next instruction if SFS or SFC test is true)
13	CRS: Control Reset	14	SCM: Select Code Most Significant Digit (Lower Address)
15	IOG: I/O Group instruction	16	SCL: Select Code Least Significant Digit (Lower Address)
17	POPIO: Power On Pulse I/O	18	IOBI 16: I/O Bus Input, Bit 16
19	SRQ: Service Request	20	IOO: I/O Output instruction
21	CLC: Clear (reset) Control FF	22	STC: Set Control FF
23	PRH: Priority High	24	IOI: I/O Input instruction
25	SFS: Skip Flag Set (Skip next instruction if Flag FF is set)	26	IOBI 0: I/O Bus Input, Bit 0
27	IOBI 8: I/O Bus Input, Bit 8	28	IOBI 9: I/O Bus Input, Bit 9
29	IOBI 1: I/O Bus Input, Bit 1	30	IOBI 2: I/O Bus Input, Bit 2
31	IOBI 10: I/O Bus Input, Bit 10	32	SIR: Set Interrupt Request
33	IRQH: Interrupt Request, Higher Select Code	34	SCL: Select Code Least Significant Digit (Higher Address)
35	IOBO 0: I/O Bus Output, Bit 0	36	+30 volts, unregulated
37	SCM: Select Code Most Significant Digit (Higher Address)	38	IOBO 1: I/O Bus Output, Bit 1
39	+4.85 volts	40	+4.85 volts
41	IOBO 2: I/O Bus Output, Bit 2	42	IOBO 4: I/O Bus Output, Bit 4
43	+12 volts	44	+12 volts
45	IOBO 3: I/O Bus Output, Bit 3	46	ENF: Enable Flag
47	-2 volts	48	-2 volts
49	FLGH: Flag Signal, Higher Select Code	50	RUN
51	IOBO 5: I/O Bus Output, Bit 5	52	IOBO 7: I/O Bus Output, Bit 7
53	IOBO 6: I/O Bus Output, Bit 6	54	IOBO 8: I/O Bus Output, Bit 8
55	IOBO 11: I/O Bus Output, Bit 11	56	IOBO 9: I/O Bus Output, Bit 9
57	IOBO 12: I/O Bus Output, Bit 12	58	IOBO 10: I/O Bus Output, Bit 10
59	(Not Used)	60	IOBO 11: I/O Bus Output, Bit 11
61	IOBO 13: I/O Bus Output, Bit 13	62	EDT: End Data Transfer
63	(Not Used)	64	IOBI 3: I/O Bus Input, Bit 3
65	IOBO 14: I/O Bus Output, Bit 14	66	PON: Power On Normal
67	(Not Used)	68	(Not Used)
69	-12 volts	70	-12 volts
71	(Not Used)	72	(Not Used)
73	SFSB: Skip Flag Set Buffered	74	IOBO 15: I/O Bus Output, Bit 15
75	(Not Used)	76	(Not Used)
77	IOBI 4: I/O Bus Input, Bit 4	78	IOBI 12: I/O Bus Input, Bit 12
79	IOBI 13: I/O Bus Input, Bit 13	80	IOBI 5: I/O Bus Input, Bit 5
81	IOBI 6: I/O Bus Input, Bit 6	82	IOBI 14: I/O Bus Input, Bit 15
83	IOBI 15: I/O Bus Input, Bit 15	84	IOBI 7: I/O Bus Input, Bit 7
85	GND: Ground	86	GND: Ground

NOTES: 1. Pins 1 & 2 are connected together on slot connector and on interface card. Pins 39 & 40, 43, & 44, 47 & 48, 69 & 70, and 85 & 86 are also connected together.

2. Corresponding IOBO and IOBI bit lines are connected together on the slot connector.

3-630. I/O CONTROL SIGNALS TIMING. The I/O time period generator provides the gating signals for the I/O signals resulting from decoding the I/O instructions and the I/O signals used during interrupt processing. The timing of these I/O signals in relation to the I/O time periods is shown in figure 4-60 of the Troubleshooting Section. Two of the I/O time period signals are buffered to provide control signals for interrupt processing.

3-631. ENF Signal. Time T2 signal is buffered to form the Enable Flag (ENF) signal which is routed to all of the I/O slots. The ENF signal is used during I/O operations to time the setting of the Flag FF on the interface card.

3-632. SIR Signal. Time T5 signal is buffered to form the Set Interrupt Request (SIR) signal which is routed to all of the I/O slots. The SIR signal is used during interrupt processing to time the setting of the Interrupt Request (IRQ) FF on the interface card.

3-633. I/O ADDRESSING.

3-634. Communication between the interface cards, special computer functions, and Switch (S-) Register is accomplished by specific I/O addresses called "select codes" as described briefly in the Computer Reference Manual. The select code encoder and decoder logic circuits on I/O Control Card A7 perform the generation and detection of the select codes for I/O addressing.

3-635. Bits 0 through 5 of the input/output instruction form a select code to specify one of 64 possible input/output devices or functions. The select code is applied to the select code decoder located on the I/O control card. These circuits decode the 6-bit code and provide a two-digit octal code output. This output is transferred to the interface card slot of the selected input/output device to permit program control of the device. Table 3-26 lists the select codes and their assignments, and indicates the corresponding interrupt location (i.e., the memory location containing the instruction to be executed when an interrupt occurs). Select code 00 gives addess to the master interrupt system enable flip-flop (IEN5 FF) on the I/O control card. Select code 01 allows access to either the overflow or switch registers. Codes 02 through 07 are reserved for processor input/output functions or options, as listed. Codes 10 through 77 (octal) are used for selection of 56 possible input/output devices (with the multiplexed I/O option installed), each capable of causing an interrupt.

3-636. Figure 5-1 illustrates the slots in the computer for the plug-in cards associated with input/output operation. Each of the interface card slots actually has two select codes assigned to it. This provides for I/O devices which contain both input and output logic circuits (e.g., magnetic tape input/output which requires two interface cards). The input portion and the output portion of the interface card may require separate select codes. When an interface card contains addressable input and output logic on the same card the slot connector must provide both select codes to a single I/O slot. The second interface card maintains priority continuity as described in paragraph 3-658. Since the slot connector wiring determines the select codes of the slots and interface cards can be plugged into any slot, the interface card assumes the select codes of the slot it is plugged into. (Interface cards are assigned to particular slot positions before shipment of a computer system and may vary from system to system.)

3-637. DECODING FUNCTION. When an I/O instruction is encountered in the user program, the 6-bit select code portion (IR0 through IR5) of the instruction is received by the I/O control card. The three least significant bits (0, 1, 2) are applied to the binary-to-octal decoder

Table 3-26. Select Code Assignments

SELECT CODE (OCTAL)	INTERRUPT LOCATION	ASSIGNMENT
00	None	Interrupt System Enable/Disable
01	None	Switch Register or Overflow
02	None	Direct Memory Access Initialization Channel 1
03	None	Direct Memory Access Initialization Channel 2
04	00004	Power Fail Interrupt/Central Interrupt Register
05	00005	Parity Error Interrupt/Memory Protect Interrupt
06	00006	Direct Memory Access Channel 1 Completion Interrupt
07	00007	Direct Memory Access Channel 2 Completion Interrupt
10	00010	I/O Device, Highest Priority
thru 25	00025	I/O Device (Mainframe)
thru 65	00065	I/O Device (Extender)
thru 77	00077	I/O Device (Multiplexer)

A7U97. The octal output of A7U97 forms the lower octal digit of the select code. The three most significant bits (3, 4, 5) are applied to the binary-to-octal decoder A7U106. The octal output of A7U106 forms the upper octal digit of the select code.

3-638. As an example, with a select code of 11 (001 001 binary) applied to the decoders, only IR0 and IR3 are true input signals. Each select code digit is produced as follows. The outputs of both decoders are false except for the "octal digit 1" of each decoder which is true, only the select code most significant digit (SCM) "1" and select code least significant digit (SCL) "1" are true. These signals are then routed to the interface cards via pins 15 and 70, respectively.

3-639. The SCM and SCL signal combination determines the slot connector containing the interface card to which the instruction portion of the I/O instruction word is directed. Each slot connector, and therefore each interface card, contains two octal select codes as described previously. Figure 3-36 illustrates the SCM and SCL signal paths to basic computer interface card slot connectors. Note that the SCM(1) signal is applied to the most-significant-digit input pins on the interface card slot connectors with select codes of 10 through 17. The SCM(2) signal is applied to the interface card slot connectors in the basic computer with select codes 20 through 25.

3-640. When either the 2155A I/O Extender or the 12894A Multiplexed I/O Accessory Kit is connected to the basic computer, jumpers W1 through W16 are installed on I/O Control Card A7. This provides both true and false Select Code Most (SCM) and Select Code Least (SCL) signals to the extender, or multiplexer, via the 48-pin edge connector at the top of the I/O control card.

3-641. The SCM(0) and SCL0, 1, 4, 5, 6, 7 signals are used on the I/O control card to form select code address signals SC0, SC1, SC4, SC5, SC6, and SC7. The function of these select codes are as follows:

a. SC0 is used to address the master interrupt system (IEN5 FF and skip flag logic).

b. SC1 is used to address the Switch (S-) register when used with data transfer instructions (OTA/B, LIA/B, and MIA/B), and to address the Overflow Register when used with flag and control instructions (STF, CLF, STC, CLC, SFC, and SFS).

c. SC4 is used to address the Central Interrupt Register when used LIA/B and MIA/B data transfer instructions, and to address the power fail logic when used with STC, CLC, and SFC.

d. SC5 is used to address memory protect when used with OTA/B (loading the Fence Register), MIA/B, LIA/B (reading the Violation Register); and to address parity error when used with STF and CLF.

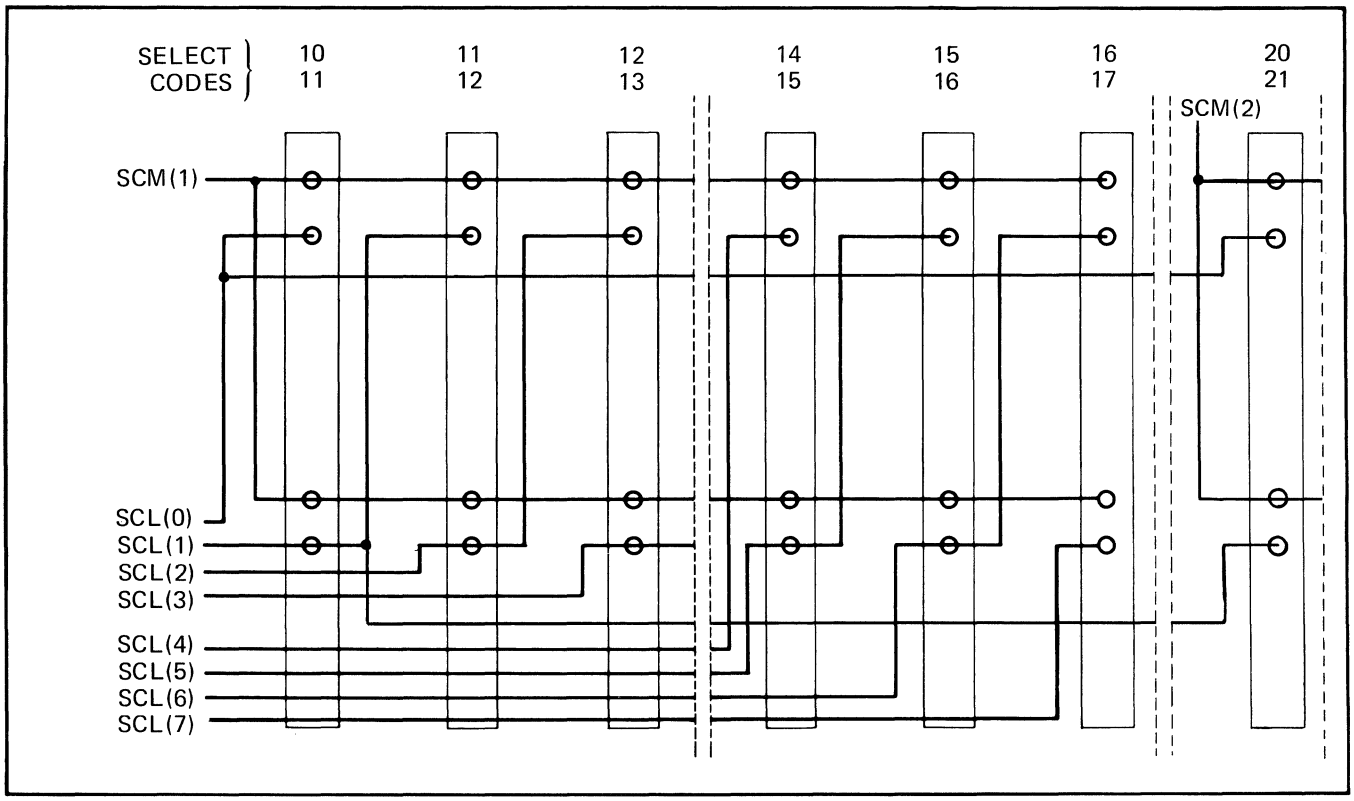

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Figure 3-36. I/O Slot Connector Select Code Wiring

e. SC6 and SC7 are used to address DMA Channels 1 and 2, respectively.

3-642. The SCM and SCL signals are applied to the same-numbered pins on all interface card slot connectors as follows:

a. Pin 14 lower select code, most significant digit.

b. Pin 16 lower select code, least significant digit.

c. Pin 37 higher select code, most significant digit.

d. Pin 34 higher select code, least significant digit.

3-643. ENCODING FUNCTION. When an input/output device requests in interrupt of a computer program, the IRQ flip-flop on the interface card for the device is set. The set-side output of the IRQ flip-flop applies a true FLG (flag) signal to the select code encoder logic on the I/O control card; the clear-side output of the flip-flop is inverted by an inverting "or" gate to apply a true IRQ signal to the select code encoder logic. These two signals are used to form the interrupt signal and the service request address to be transferred to the computer.

3-644. CENTRAL INTERRUPT REGISTER. The central interrupt register, located on I/O Control Card A7, consists of CI0 through CI5 FFs and associated clocking and output gating circuits. This register stores the service request address, which is encoded from the FLG and IRQ signals from the interface card or special computer function.

3-645. Loading. A valid address is present at the input to the register from the time that the interrupting function IRQ FF sets until it is cleared during the last 100 nanoseconds of phase 1B. The register is loaded by a true clock level from the clocking circuits which clears the respective FFs corresponding to the true bits of the select code.

3-646. Clocking. The register clocking circuits consist of "and" gates A7U75B and A7U75D. These gates provide a true clock signal to the register FFs during time T6 of the interrupt fetch phase (phase 1B), which is the first I/O clock period of the interrupt fetch phase. The register contents are also gated onto the S-bus during this time period.

3-647. Output Gating. The first microinstruction in the microroutine for phase 1B (which is executed during I/O time T6) contains a CIR microcode in the S-bus field. When this microcode is detected by the S-bus field decoding circuits on Microinstruction Decoder 1 Card A3, the Read Central Interrupt Register (RCIR) signal at pin 54 of I/O Control Card A7 becomes true. This enables the central interrupt register output gates and the service request address (select code) strobed onto the S-bus to be stored into the M-register.

3-648. The contents of the central interrupt register is also available through programmed instruction. An LIA 04 or LIB 04 instruction will put the address of the last device that interrupted into the A- or B-register. (The address is held in the central interrupt register until the next interrupt is processed.) During execution of an LIA/B instruction, the IOI signal at pin 53 of the I/O control card becomes true during times T4 and T5. The IOI signal is "anded" with the true SC4 (select code 04) signal from the select code encoder circuits to gate the contents of the central interrupt register onto the S-bus. During time T5, the interrupt address is stored in the A- or B-register.

3-649. I/O INSTRUCTION PROCESSING.

3-650. ROM PROGRAM CONTROL. The I/O instructions are executable by the five microroutines stored at addresses 0040 through 0077 of the ROM microprogram (refer to table 4-9 in the Troubleshooting Section). The data transfer instructions (LIA/B, MIA/B, and OTA/B) each have their own microroutines for their execution. The other I/O group instructions are executable by the remaining two microroutines labeled FLAG and CTRL (control). The FLAG microroutine is used to execute HLT, STF, CLF, SFS, SFC, SOS, and SOC. The CTRL microroutine is used to execute STC, CLC, SOV, and CLO. These two mircoroutines are used in conjunction with the I/O group decoder circuits on I/O Buffer Card A8 to provide the necessary control signals for execution of the flag and control group instructions.

3-651. The first microinstruction in each microroutine contains IOG1 coded in the special field to synchronize the CPU timing with the I/O timing and to enable the I/O group decoder. When IOG1 is detected by the special field decoder circuits on Instruction Register Decoder Card A6, the IOG1 signal is sent to the clock generator circuits on Timing and Control Card A1 and to the IOGM FF on I/O Control Card A7. The clock generator circuits inhibit the $\overline{CLK1}$, $\overline{CLK2}$, CLK, and STCLK signals until I/O time T2. This holds the microinstruction containing the IOG1 microcode in the ROM instruction register until its execution during time T2. Also, the set output from the IOGM FF (the IOGE signal) becomes true at time T3 and remains true until the end of time T6. The IOGE signal enables the I/O group decoder, the I/O violation circuits in the memory protect logic, and the addressed interface card (if no I/O violation is present).

3-652. I/O GROUP DECODER CIRCUITS. The I/O group decoder circuits, located on I/O Buffer Card A8, perform decoding of the flag and control I/O group instructions in conjunction with the FLAG and CTRL microroutines at ROM addresses 0040 through 0043, and 0074 through 0077. The OTA/B instructions are also decoded to provide the IOO signal to the interface cards and special computer functions.

3-653. Binary-to-octal decoder A8U65 decodes instruction register bits IR6 through IR8 to provide a false output on one of the octal output lines depending upon which I/O group instruction is being decoded. The outputs of the decoder are applied to inverters to provide true signals to the gating circuits. Instruction register bits IR9 and IR11 are also applied to the gating circuits to further discriminate the instruction being decoded. The operation of the I/O group decoder circuits for each I/O group instruction is as follows:

a. STC CLC. The inverted decimal 7 output of A8U65 is true when either STC or CLC is being executed. The output is gated with time T4 signal and "anded" with IR11 and $\overline{IR11}$ to generate STC, or CLC, depending upon the state of IR11. The STC and CLC signals are routed to I/O Control Card A7 to direct clear the INC FF, to set the Control 4 (power fail) FF when used with select code 04, to set (or clear) the Control 6 and Control 7 (DMA Channel 1 and 2) FFs when used with select codes 06 and 07, respectively. The CLC signal, when used with select code 01, sends a CRS (Control Reset) signal to all the interface cards to clear the control FFs. The STC and CLC signals are also routed to Direct Memory Access (DMA) Card A9 and to all interface cards to set, or clear, the Control FF addressed by the select code.

b. SFS, SOS. The inverted decimal 3 output of A8U65 is true when either SFS or SOS is being executed. Since the output is ungated, it is true from time T3 through time T6. The resulting SFS signal is routed to Microinstruction Decoder 2 Card A4 to test the state of the OVF ("not" Overflow) FF when used with select code 01. Also, the SFS signal is routed to I/O Control Card A7 to test the state of the DMA Channel 1 Flag (F6 FF), DMA Channel 2 Flag (F7 FF), or interrupt system IEN5 FF) when used with select codes 06, 07, and 00, respectively. It is also routed to all interface cards to test the state of the FLAG FF addressed by the select code.

c. SFC, SOC. The inverted decimal 2 output of A8U65 is true when either SFC or SOC is being executed. Since the output is ungated, it is true from time T3 through time T6. The resulting SFC signal is routed to Microinstruction Decoder 2 Card A4 to test the state of the OVF ("not" Overflow) FF when used with select code 01. Also, the SFC signal is routed to I/O Control Card A7 to test the state of the DMA Channel 1 Flag (F6 FF), DMA Channel 2 Flag (F7 FF), interrupt system (IEN5 FF), or power fail direction (DIR FF) when used with select codes 06, 07, 00, and 04, respectively. It also is routed to all the interface cards to test the state of the FLAG FF addressed by the select code.

d. STF, CLF, STO, CLO. The inverted decimal 1 output of A8U65 is true when either STF, CLF, STO, and CLO is being executed. The output is gated with time T3 signal to form the STF signal. The STF signal is routed to the Microinstruction Decoder 2 Card A4 to set the OVF ("not" Overflow) FF when used with select code 01. Also, the STF signal is routed to I/O Control Card A7 to direct-clear the INC FF, to direct-set the IEN5 FF when used with select code 00 (which enables the interrupt system), and to set the FB6 FF (DMA Channel 1 Flag Buffer) or FB7 FF (DMA Channel 2 Flag Buffer) when used with select code 06 or 97, respectively. It is also routed to all interface cards to set the Flag Buffer FF addressed by the select code.

e. CLF. As explained in step "d" above, when the CLF instruction is decoded by A8U65, it generates a true STF signal. However, the STF function (which is the opposite of CLF) is nulled by gating the true I-register bit 9 (IR9) during time T4 to form a true CLF signal. Therefore, the Flag FF that was set by the true STF signal during time T3 is cleared by the true CLF signal during time T4.

f. OTA/B. The decimal 6 output of A8U65 is used to generate a true IOO signal during time T3T4 whenever an OTA/B instruction is executed. The IOO signal is used to load the upper boundary address of the protected area of memory into the Fence (F-) Register when used with select code 05, is used to load control data into DMA during initialization when used with select codes 06 and 07, is used to display data in the DISPLAY REGISTER when used with select code 01, and is used to load data from the computer into a data buffer register on any interface card addressed by the select code.

3-654. DATA TRANSFER INSTRUCTIONS. Data transfer instructions MIA/B, LIA/B, and OTA/B are processed mainly by ROM program control. When any data transfer instruction is placed in the I-register and the execute phase (phase 3) is set, the ROM mapper on ROM Control Card A2 directs the CPU to the starting address of the appropriate microroutine (MI*, LI*, or OT*).

3-655. MIA/B. The first microinstruction in the MI* microroutine freezes the CPU until time T2 and enables the IOG signal (from time T3 to the end of time T6). The CPU then executes the four microinstructions at times T2, T3, T4, and T5, respectively. The IOI microcode in the S-bus field of the last two microinstructions causes a true RIOB signal to be applied to the I/O buffer logic on I/O Buffer Card A8. The RIOB signal causes a true IOI signal to be applied to the addressed interface card which causes the data from the device to be placed on the IOB lines to the I/O buffers during times T4 and T5. The RIOB signal also enables the I/O buffers to transfer data from the IOB lines onto the S-bus during this time and the data is applied to the function generator on Arithmetic/Logic Card A5.

3-656. The last microinstruction in the MI* microroutine actually performs the "merge" into the A- or B-register. The CAB microcode in the R-bus field causes the R-bus multiplexer on card A5 to read either the A- or B-register onto the R-bus, depending upon the state of IR11. The function generator inclusive "ors" (merges) the R-bus and S-bus by the IOR microcode in the function

field. The results are placed on the T-bus, and the CAB microcode in the store field stores the results in the A- or B-register, depending upon the state of IR11.

3-657. LIA/B. The microroutine for the LIA/B instruction is identical to the MI* microroutine, except that the CAB microcode is not present in the R-bus field. Therefore, the A- or B-register is not read onto the R-bus during execution of the last microinstruction.

3-658. OTA/B. The first microinstruction in the OT* microroutine freezes the CPU until time T2 and enables the IOG signal and I/O group decoder for the duration of the I/O cycle (times T3 through T6). The resulting true OT* signal from the I/O group decoder circuits is gated with I/O time T3T4 to provide a true IOO signal during that time.

3-659. The next three microinstructions contain CAB in the R-bus field and RRS in the S-bus field. These cause the contents of the A- or B-register, depending upon the state of IR11, to be read onto the R-bus then onto the S-bus during times T3 through T5. The last two microinstructions also contain IOO microcodes in the store field which cause a true SIOB signal to be applied to the I/O buffers during times T4 and T5. The S-bus data is gated onto the I/O bus during this time.

3-660. The true IOO signal at time T3T4 and the data available on the I/O bus during time T4T5 makes the data available to the I/O device during time T4.

3-661. CONTROL INSTRUCTIONS. Control instructions STC, CLC, STO, and CLO are processed mainly by the I/O group decoder circuits on I/O Buffer Card A8. However, the CTRL microroutine is executed to synchronize the CPU with the I/O cycle and to enable the I/O group decoder. Processing of these control instructions has been discussed previously with the operation of the I/O group decoder circuits (refer to paragraph 3-629).

3-662. FLAG INSTRUCTIONS. Flag instructions STF and CLF are processed mainly by the I/O group decoder circuits on I/O Buffer Card A8. However, the FLAG microroutine is executed to synchronize the CPU with the I/O cycle and to enable the I/O group decoder. Processing of these flag instructions has been discussed previously with the operation of the I/O group decoder circuits (refer to paragraph 3-629).

3-663. PROGRAM SKIP INSTRUCTIONS. Program skip instructions SFS, SFC, SOS, and SOC are processed mainly by the I/O group decoder circuits on I/O Buffer Card A8. However, the FLAG microroutine is executed to synchronize the CPU with the I/O cycle and to enable the I/O group decoder. The decoding of these instructions and their destinations are discussed with the operation of the I/O group decoder circuits (refer to paragraph 3-629). If the skip condition is met, a true Skip Flag (SKF) signal is sent to the increment P-register logic on Timing and Control Card A1. The increment P-register logic, in turn, applies a true INCP signal to the P-register which increments the register.

3-664. HALT INSTRUCTION. The HLT instruction is processed mainly by the I/O group decoder circuits on I/O Buffer Card A8. However, the FLAG microroutine is executed to synchronize the CPU with the I/O cycle and to enable the I/O group decoder. The inverted octal 0 output of the binary-to-octal decoder A8U65 is true when HLT is being executed (times T3 through T6). The true HLT signal is applied to "and" gate A8U63B and to the I/O violation circuits in the memory protect logic.

3-665. If memory protect is on ($\overline{\text{MPC}}$ FF is cleared), and the HLT instruction was not fetched from the trap cell during the interrupt fetch phase (phase 1B), the (HLT) signal is inhibited by the false signal applied to pins 10 and 12 of A8U63B from the I/O violation circuits. Memory protect logic will also cause an interrupt.

3-666. If memory protect is on and the HLT instruction was fetched from the trap cell during phase 1B, or memory protect is off, gate A8U63B is enabled and the true (HLT) signal is gated by signal T3, providing a true HIN signal. The HIN signal is applied to the run logic on Timing and Control Card A1 to set the halt mode, and to Operator Panel Card A24 to initiate the control signals for obtaining and displaying the contents of the T-register (memory data) in the DISPLAY REGISTER.

3-667. INTERRUPT SYSTEM.

3-668. The interrupt system provides the means for an external device to interrupt the program in progress when data is available or when additional output data can be accepted. Figures 3-37 and 3-38 illustrate the relationship between the computer, the I/O control and buffer cards, and typical interrupt logic on a particular interface card. (Figure 3-38 is for interrupt-logic explanatory purposes only.) Refer to figure 4-61 in the Troubleshooting Section for a chart of typical interrupt system timing.

3-669. An interrupt request from an external device occurs when the following conditions are met:

a. The interrupt system is enabled.

b. The flag flip-flop of the specific device interface card is set.

c. The control flip-flop of the specific device interface card is set.

d. No priority-affecting instruction (STF, CLF, STC or CLC) is in progress.

e. No higher-priority devices satisfy the conditions expressed in steps "a" through "d".

3-670. INTERRUPT SYSTEM ENABLE/DISABLE. The computer program determines if interrupt requests from the external devices will be recognized. This is accomplished by enabling or disabling the interrupt system enable flip-flop (IEN5 FF) on the I/O control card. A set flag

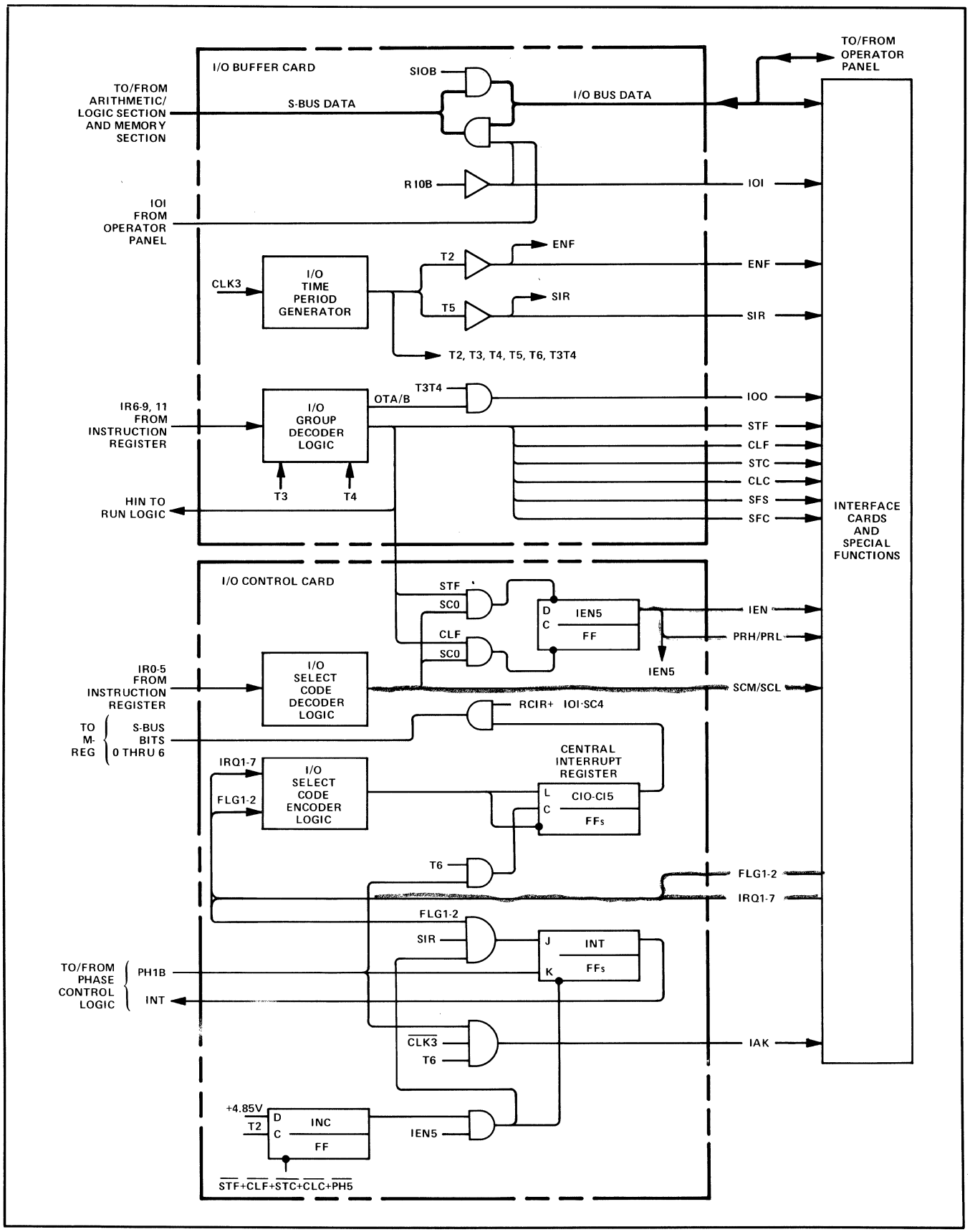

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Figure 3-37. I/O Section, Functional Diagram

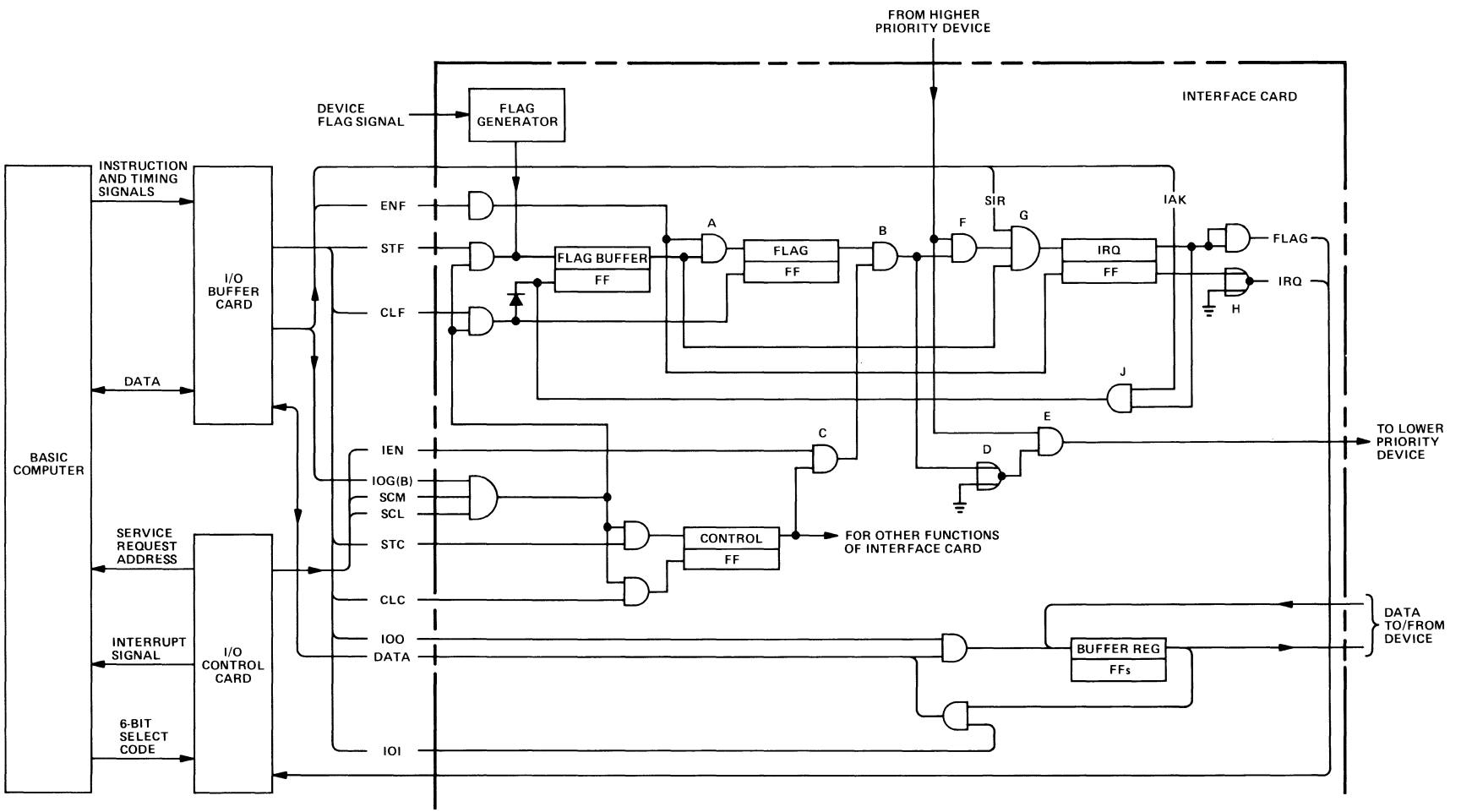


Figure 3-38 Typical Interface Card

(STF) instruction with a select code of 00 (octal) sets the flip-flop and enables the interrupt system. A clear flag (CLF) instruction with a select code of 00 (octal) clears the flip-flop and disables the interrupt system.

3-671. When computer power is initially turned on, the IEN5 FF is automatically cleared, disabling the interrupt system. Initial turn-on also clears all control flip-flops on the interface cards to prevent input/output devices from running when power is applied, and sets all flag buffer and flag flip-flops on the interface cards. Therefore, to operate any device under interrupt system control it is first necessary to set the IEN5 FF, clear the individual flag buffer and flag flip-flops, and set the individual control flip-flop.

3-672. In the halt mode, the IEN5 FF can be toggled by pressing the INTERRUPT SYSTEM switch on the operator panel. Each time the INTERRUPT SYSTEM switch is pressed, a true clock signal is applied to the IEN5 FF, changing its state. The true set output from the IEN5 FF (IEN5 signal) lights the INTERRUPT SYSTEM indicator in the switch assembly.

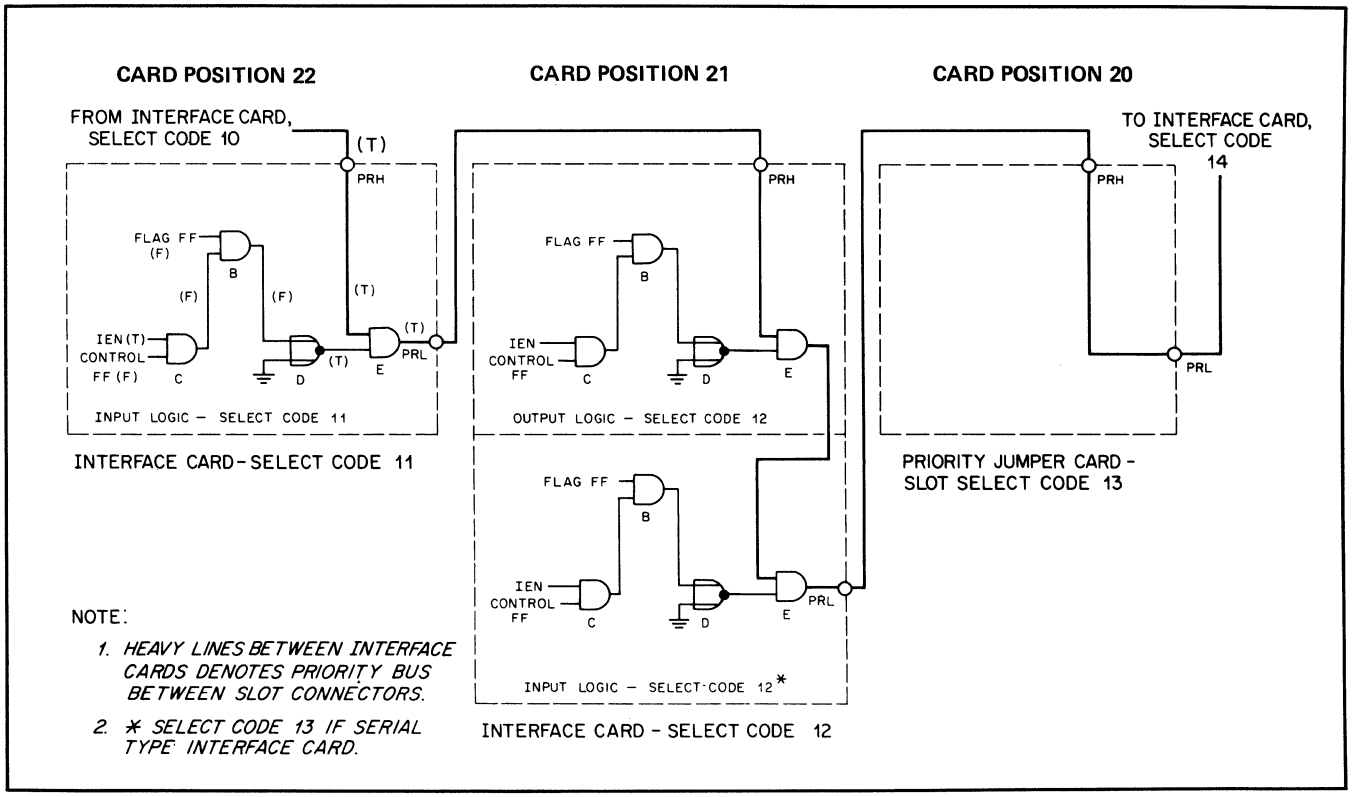
3-673. Figure 4-62 in the Troubleshooting section shows the circuits involved in enabling the interrupt system and priority structure. The set-side output from the IEN5 FF and the set-side output from the CONTROL 4 (power fail) FF provide the enabling signals for the interrupt system. Power fail (select code 04) and parity error (select code 05) are the only functions that can interrupt without the IEN5 FF being set.

3-674. INTERRUPT PRIORITY. The priority chain establishes an orderly sequence for granting interrupts.

3-675. Priority Assignments. A priority network on the interface cards allow only one external device to interrupt the computer program regardless of the number of devices requesting an interrupt. The priority network gives highest priority to select code 04, reserved for power failure interrupt, and decreasing priority to select codes in order from 05 through 77 (see table 3-26).

3-676. As shown in figure 5-1, each of the interface card slots in the computer is assigned two interrupt priorities corresponding to the two select codes assigned each slot. This provides an interrupt priority for both the input and output portions of an interface card, if they are separately addressable. The interrupt priority assignments of each slot remain fixed but since any interface card can be plugged into any slot, the interrupt priority of a given device can be easily changed by plugging the device interface card into another slot.

3-677. Priority Network Operation. As shown in figure 3-38, priority is established by a hardware-implemented priority chain. The gates illustrated in figure 3-39 are identified by letters and correspond to those used in figure 3-38. The true-false logic levels for an interface card which is not requesting an interrupt are illustrated in parenthesis (T), (F) on the first interface card (Select Code 11) with the Interrupt System enabled (IEN input is true).



2133-136

Figure 3-39. Interrupt Priority

Also, the PRH (Priority High) signal is true, indicating that a device of higher priority is not requesting an interrupt. In this case, the "chain" is not broken and a true PRL (Priority Low) signal is available to the next interface card (Select Code 12) as a true PRH signal to that card.

3-678. When the interface card contains both input and output logic, each type of logic may have a separate select code and corresponding interrupt priority, with the priority chain connected internally. The output logic (controls data output transfers) of the interface card is usually of higher priority than the input logic (controls data input transfers) on cards containing both types of logic. Since this interface card uses both select codes assigned to its slot, the second interface card for the I/O device (if required) must provide continuity for the priority network. There can be no gaps in the network for it to function properly. If only one interface card (which operates from two select codes) is required for a device, a priority jumper card would be required to maintain priority continuity to the lower-priority devices.

3-679. If the output logic portion of the interface card requests an interrupt, the PRL signal to the input logic portion of the interface card is then false, breaking the "chain", and preventing any interface card of lower priority from interrupting the computer program. A service subroutine can then be entered to process the interrupt of the output logic.

3-680. A service subroutine of any device can be interrupted by a higher priority device; then after the higher priority interrupt subroutine is completed, the lower priority subroutine may continue. In this way, several service subroutines may be in a state of interruption at one time. Each will be permitted to continue when the next higher priority subroutine is completed.

3-681. Interrupt priority can also be program controlled. Since an interrupt cannot occur unless the control flip-flop of the interface card is set, all control flip-flops on the interface cards of higher priority than the one desired can be cleared by a clear control (CLC) instruction. This prevents those interface cards from requesting an interrupt and establishes the desired device as the highest-priority device. However, these devices must then be serviced by testing the flag and/or setting the control flip-flop again.

3-682. Priority Continuity. Figure 4-61, in the Troubleshooting Section, illustrates the continuity of the interrupt priority network for special processor functions (power fail, parity error, memory protect, and DMA) and input/output interface cards plugged into the computer mainframe.

3-683. Since the power failure interrupt function (select code 04) is on at all times, it can interrupt the computer regardless of the state of the IEN5 FF. For all other special processor functions and interface cards, (with the exception of the parity error) the flip-flop must be set before an interrupt can occur. When an interface card requests an interrupt, its false PRL signal is applied to the next interface card as a false PRH signal to prevent it from requesting an interrupt. This sequence continues from card to card until the last interface card receives a false PRH signal.

3-684. Priority-Affecting Instructions. Four instructions, STC, CLC, STF, and CLF, affect the priority structure of the input/output devices. Whether a device can request an interrupt or not depends upon whether its interface-card control flip-flop is set or cleared (STC, CLC) and its flag flip-flop is set or cleared (STF, CLF). If a device cannot request an interrupt, all succeeding lower priority devices assume a priority of one higher in the priority chain, and vice versa.

3-685. The four instructions also inhibit all interrupts during the machine phase in which they occur by direct-clearing the ICN (Interrupt Control) FF, on I/O Control Card A7, which in turn direct-sets the $\overline{\text{INT 1}}$ ("not" Interrupt 1) FF. The false set output from the INC FF holds the $\overline{\text{INT 1}}$ FF direct-set until the following time T2, at which time the INC FF is clocked and set. This prevents interrupts during entry and exit from subroutines. Also, a combination of two of the four instructions are normally the next-to-last instruction in a service subroutine processing an interrupt (the last being a JMP,I instruction to cause return to the main program or to an address in another service subroutine). If another input/output device could interrupt immediately after execution of these instructions (and before the JMP,I instruction), the possibility would exist that the first device may interrupt a second time before the JMP,I instruction is performed. In this event, the first main-program address (or the other service-subroutine would be destroyed, preventing a return to the main program or to the other service subroutine.

3-686. INTERRUPT GENERATION.

3-687. When the external device has completed its operation, it generates a device flag signal to the interface card flag generator which sets the flag buffer flip-flop (see figure 3-38). The output of the flag buffer flip-flop in conjunction with the ENF (enable flag) signal from I/O Buffer Card A8 at time T2 causes "and" gate A to set the flag flip-flop. The flag flip-flop output is "anded" at gate B with the output of "and" gate C. The gate C output is true when the control flip-flop is set and when the IEN (interrupt enable) signal is received from the I/O control card at time T3. Unless the control flip-flop is set by a set control (STC) instruction, an interrupt request cannot occur.

3-688. The control flip-flop is set under program control and therefore, may be set at any T4 time of a machine cycle, depending on the type of operation being performed. The STC instruction is enabled to the control flip-flop by the SCM (select code most significant digit) and SCL (select code least significant digit) signals and the IOG (I/O group instruction) signal from the I/O control card. The SCM and SCL signals are enabled on the individual interface card by the IOG signal which occurs when the instruction to be performed is an I/O group instruction. When the control flip-flop sets, a true input is applied to "and" gate C. The inputs to "and" gates B and C are then true and gate B

applies a true output to inverting "or" gate D. The false output of gate D disables "and" gate E, making the priority network bus to the lower-priority devices false. This prevents any device of lower priority from requesting an interrupt.

3-689. At the same time that gate B applied a true output to gate D, it also applied a true output to "and" gate F. The priority network signal to gate F will be true if an interface card (device) of higher priority than the one represented in figure 3-38 is not requesting an interrupt. In this case, the true output of gate F is combined with the SIR (Set Interrupt Request) signal from I/O Buffer Card at time T5 and the output of the set flag buffer flip-flop to provide a true output from "and" gate G. The gate G output sets the IRQ (interrupt request) flip-flop.

3-690. The IRQ flip-flop outputs provide the flag signal and the IRQ signal to the I/O select code encoder circuits on I/O Control Card A7. (The IRQ signal is obtained by the inversion of the false clear side output of the IRQ flip-flop by inverting "or" gate H.) The flag signal is "anded" with the set outputs from the IEN5 and INC FFs, and the SIR signal to clear the $\overline{\text{INT 1}}$ FF and form an interrupt (INT) signal. However, the set output from the INC FF is false for the remainder of the machine cycle during which an instruction occurs that affects device priorities (STC in figure 4-60). At time T2, the IRQ flip-flop is cleared by the ENF signal to allow a higher-priority device to request an interrupt. If the control flip-flop is still set and no higher-priority devices have requested an interrupt, the IRQ flip-flop will again be set at time T5 (SIR). The flag and IRQ signals are again sent to the I/O select code encoder circuits. The signals are used to form a 6-bit service request address to be sent to the computer at time T6 of the interrupt fetch phase (phase 1B). The flag signal and the now true set output from the INC FF clear the $\overline{\text{INT 1}}$ FF. The true clear output from the $\overline{\text{INT 1}}$ FF forms the interrupt (INT) signal which is sent to the phase control logic in the computer. This signal causes an interrupt at the end of the current machine phase, switching the computer into the interrupt fetch phase, except when any of the following conditions occur:

a. A jump indirect (JMP,I) or a jump to subroutine indirect (JSB,I) instruction is not fully executed. (These instructions inhibit all interrupts until fully executed for three indirect levels of addressing. An interrupt request will be granted at the end of the machine phase immediately following the complete execution of the JMP,I or JSB,I instruction or the third indirect reference.)

3-691. INTERRUPT PROCESSING.

3-692. FUNCTIONAL DESCRIPTION. During this interrupt fetch phase (phase 1B), the computer decrements the P-register by one to ensure that the proper location in the main program will be returned to after the interrupt is processed. (The P-register was incremented by one when the execute phase (phase 3) was set, or during the execute phase if a program skip was executed.) Also, the computer places the service request address (which is always equal to the select code of the interrupting device) from the I/O select code encoder logic circuits into the M-register. This addresses the memory location having the same number as the service request address (select code). This location in memory is referred to as the "interrupt location" or "trap cell" and is reserved for that particular device. For example, a device specified by a select code of 10 will interrupt to (i.e., causes execution of the contents of) memory location 00010. The computer fetches the instruction in the interrupt location which will usually be a jump to a subroutine (JSB,I) instruction, although any legal instruction may be placed in the interrupt location.

3-693. The contents of the P-register plus one are stored in the first location (X) of the subroutine. (Since the previous contents of the first memory location are destroyed when P + 1 is stored, the first instruction of the subroutine should always be a no-operation (NOP) instruction or equivalent.) The location of the subroutine (X + 1) is placed in the P- and M-registers, and the computer resumes operation in the subroutine. Thus, the instruction at location X + 1 is the first instruction of the subroutine to be executed. The contents of the working registers that were in use in the main program should be stored when entering the subroutine and restored before exit from the subroutine. The exit from the subroutine is made with a JMP,I to location X. This places the address of the interrupted program instruction in the P- and M-registers and normal program operation resumes.

3-694. DETAILED DESCRIPTION. When the interrupt fetch phase (phase 1B) is set, the interrupt is acknowledged by a true PH1B (phase 1B) signal and processed by ROM microprogram control. The microroutine for phase 1B, which consists of the six microinstructions at addresses 004 through 010 in the ROM microprogram, processes the interrupt request. The effects of the PH1B signal and the execution of the microroutine start at I/O time T6.

3-695. PH1B Signal. The true PH1B (phase 1B) signal from the phase control logic on Timing and Control Card A1 sets the INT 1 FF at the end of the present clock period to remove the request for phase 1B (making the INT signal flase) to the phase control logic. (If the interrupt request had been derived from power fail, parity error, or memory protect functions, the INT 2 FF would have been cleared to request the interrupt fetch phase (phase 1B) and the PH1B signal would set the INT 2 FF to remove the request.)

3-696. The true PH1B signal is also applied to the I/O violation circuits in the memory protect logic on I/O Buffer Card A8 to check for a possible I/O violation (refer to paragraph 3-685). During I/O time T6, the true PH1B signal clocks the service request address from the I/O select code encoder circuits into the central interrupt register. During the last 100 nanoseconds of T6, the true PH1B signal causes a true IAK (Interrupt Acknowledge) signal to be applied to all the I/O slots and special computer functions.

3-697. IAK Signal. The true IAK signal from I/O Control Card A7 and the set-side output from the IRQ FF clears the FLAG BUFFER FF through "and" gate J (see figure 3-38). Since the set-side output of the FLAG BUFFER FF is applied to "and" gate G, clearing the flip-flop prevents the setting of the IRQ FF which would cause another interrupt from the same flag signal at time T5 of phase 1B when the true SIR signal is again applied to gate G. The FLAG BUFFER FF can also be cleared by a programmed CLF (Clear Flag) instruction. At time T2, the ENF signal clears the IRQ FF.

3-698. ROM Address 004. This microinstruction is not executed until I/O time T6 because of the RW microcode present in the special field, which causes a freeze until time T6. The CIR microcode in the S-bus field causes a true RCIR signal which gates the contents of the central interrupt register (service request address) in the M-register. Valid data (the contents of the trap cell) will not be available until I/O time T4.

3-699. ROM Addresses 005 and 006. During I/O times T2 and T3 the microinstructions at ROM addresses 005 and 006 are executed to decrement the P-register. First, the contents of the P-register are processed by the function generator logic in the arithmetic/logic section which performs a 2's complement substract, then stores the results back into the P-register. Secondly, the contents of the P-register are again processed by the function generator logic which "nor's" the P-register contents with the R-bus contents (all zeros) then stores the results back into the P-register.

3-700. ROM Address 007. During I/O time T4, the microinstruction at ROM address 007 is executed which puts the contents of the trap cell into the I-register and sets the next phase. The AAB and COND microcodes in the R-bus and S-bus fields causes the T-register contents to be read out onto the S-bus. The IOR and IR microcodes in the function and store fields place the S-bus contents in the I-register via the T-bus. The EOP microcode in the skip field causes the phase control logic to generate the appropriate set phase signal to set the next machine phase.

3-701. ROM Address 010. During I/O time T5, the microinstruction at ROM address 010 is executed if the user instruction in the I-register is a memory reference group instruction. Otherwise, a NOP occurs. The purpose of this microinstruction is to read the operand address into Scratch Pad 1. The ADR microcode in the S-bus field reads I-register bits 0 through 9 and, depending upon whether bit 10 (the zero/current page bit) is a "0" or a "1", six "0"s or P-register bits 10 through 15 are read onto the S-bus, respectively. The IOR microcode in the function field passes the contents of the S-bus through to the T-bus, and the S1 microcode in the store field stores the operand address in Scratch Pad 1. The AAB microcode in the special field checks for A- or B-register addressing.

3-702. I/O SYSTEM RESET.

3-703. The I/O System can be reset either by the PON signal at power turn-on, or by the INTERNAL PRESET switch on the operator panel (or the PRESET switch on the controller panel, if installed), or partially reset by a CLC instruction to select code 00.

3-704. PON SIGNAL. The PON signal can be considered as master reset signal for the entire computer. in addition to performing the same functions as the INTERNAL PRESET and EXTERNAL PRESET switches on the operator panel, it established the initial conditions for the operator panel to prevent operator panel generated signals from randomly controlling the computer.

3-705. When power is applied to the computer, the PON signal remains false for approximately 25 milliseconds after dc operating power is applied to the computer circuits. The false PON signal in turn generates POPIO and CRS signals on I/O Control Card A7 and the RESET signal on Timing and Control Card A1. The PON, POPIO, CRS, and RESET signals are routed throughout the computer to establish initial conditions for proper operation. By referring to the INTERNAL PRESET and EXTERNAL PRESET switches servicing and timing diagrams in the Troubleshooting Section, the computer circuits affected become more apparent (see figures 4-90 through 4-93).

3-706. POPIO AND CRS SIGNALS. Either the false PON signal or the true PRSE signal (caused by pressing the EXTERNAL PRESET switch on the operator panel, or the PRESET switch on the controller panel) will generate true POPIO and CRS signals during I/O time T5. The POPIO signal directly sets the FLAG BUFFER FF on all interface cards and Channels 1 and 2 of DMA on the I/O control card. At time T2, the T2 signal clears the IRQ FF and together with the set output from the FLAG BUFFER FF sets the FLAG FF on all interface cards and DMA. The CRS signal resets the CONTROL FF on all interface cards and DMA. (The CRS signal can also be programmed by a CLC instruction to select code 00.) Resetting the CONTROL FFs prevents an interrupt from occurring when the interrupt system is initially enabled.

3-707. RESET SIGNAL. The RESET signal generated on Timing and Control Card A1 is applied to I/O Control Card A7 which clears the IEN5 FF, ensuring that the interrupt system is turned off. This prevents an interrupt signal from being sent to the phase control logic which would place the computer in the interrupt fetch phase.

3-708. I/O VIOLATION CIRCUITS.

3-709. The I/O violation circuits located on I/O Buffer Card A8 form part of the memory protect logic. The function of the I/O violation circuits is to inhibit I/O group instructions not associated with select code 01 (switch and overflow registers) and cause a memory protect interrupt when the memory protect function is enabled. Also, the I/O violation circuits disable memory protect when an

interrupt occurs to allow I/O group instructions contained in the driver routine to be processed, thereby servicing the interrupting device.

3-710. Each time an I/O Group instruction is encountered in the user program, the IOG signal from I/O Buffer Card A8 must be true to enable the I/O interface card to respond to the I/O Group instruction.

3-711. The IOG1 code in the SPECIAL field of the ROM microprogram is used for I/O Group instructions which causes the IOG1 signal to be true. The IOG1 signal from the special field decoder circuits on Instruction Register Decoder Card A6 is applied to I/O Control Card A7 and "anded" with the ENF signal to set the IOGM FF. The set output from the IOGM FF (IOGE signal) is true at time T3 and remains true until the end of time T6. The IOGE signal is applied to I/O Buffer Card A8 to enable the I/O group decoder and to enable gate A8U105A.

3-712. If memory protect is disabled ($\overline{\text{MPC}}$ FF set), the IOGE signal is "anded" with the true set output from the $\overline{\text{MPC}}$ FF by gate A8U73C which provides a true input to the other input to gate A8U105A, forming a true IOG signal. The IOG signal is true from the beginning of time T3 until the end of time T6.

3-713. If memory protect is enabled ($\overline{\text{MPC}}$ FF cleared), only those I/O Group instructions associated with select code 01 (switch and overflow registers) will provide a true IOG signal. The true IOGE signal with the true SC1 signal at gate A8U73A in the I/O violation circuits provide a true input to gate A8U105A to form a true IOG signal.

3-714. The I/O instructions associated with other select codes are inhibited and cause a memory protect interrupt. The false output from gate A8U72A in the I/O violation circuits inhibits gate A8U105A from forming a true IOG signal when IOGE is true. The true IOGE signal is applied to gate A8U66B and at time T3 the output from A8U66B sets the MPV FF.

3-715. Interrupts disable memory protect to allow I/O Group instructions contained in the driver routine to be processed, thereby servicing the interrupting device.

3-716. When the interrupt fetch phase (phase 1B) is set, the PH1B signal from the phase control logic on Timing and Control Card A1 clears the PH3B FF. At the end of phase 1B, the PH1B signal goes false which provides a true output from gate A8U55D. The output remains true until one clock period after the normal fetch phase (phase 1A) is set (PH1A signal true). The true output from gate A8U55D enables gates A8U73D and A8U92A.

3-717. If the instruction contained in the "trap cell" is not an I/O group instruction, the IOGE signal will be false which causes the output from gate A8U72A to be false which, in turn, provides a true input to pin 13 of gate A8U92A. At time T3 the output of gate A8U92A is true which sets the $\overline{\text{MPC}}$ FF and memory protect is disabled.

3-718. If an I/O group instruction (other than HLT) is contained in the "trap cell", the IOGE signal is true which causes a false output from gate A8U73D and, in turn, provides a false output from gate A8U81A. The set input to the $\overline{\text{MPC}}$ FF remains false and memory protect is not disabled.

3-719. If the HLT instruction is contained in the "trap cell", the false output from gate A8U81C causes a true output from gate A8U92A at time T3. This in turn sets the $\overline{\text{MPC}}$ FF and memory protect is disabled.

SECTION IV TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. This section of the manual provides information for troubleshooting the 2100A Computer. A thorough knowledge of the organization of this section is essential for the effective use of its contents. The following is a list of the information presented in this section:

a. General servicing information.

(1) Program instruction formats
(2) Absolute binary loader listings and loading procedures
(3) List of diagnostic programs
(4) Diagnostic operating procedures
(5) Use of internal maintenance switches
(6) Basic troubleshooting procedures
(7) Overall computer servicing diagram

b. Central processor servicing information.

(1) Central processor clock signals timing
(2) ROM microinstruction coding
(3) ROM microinstruction descriptions
(4) Cross reference of basic instruction to ROM address
(5) ROM program listing
(6) ROM microprogram servicing data

c. Memory servicing information.

(1) Memory section servicing diagram
(2) Memory addressing index
(3) Memory timing specifications

d. I/O section servicing information.

(1) Parity error halt troubleshooting information
(2) I/O control and interrupt signals timing diagrams
(3) Interrupt priority servicing diagram
(4) Interrupt flowchart
(5) DMA servicing and timing diagrams

e. Operator panel servicing information.

(1) Operator panel timing diagrams
(2) Operator panel servicing diagrams

f. Controller panel servicing information.

(1) Controller panel timing diagrams
(2) Controller panel servicing diagrams

4-3. GENERAL SERVICING INFORMATION.

4-4. General servicing information consists of general reference information required for troubleshooting and testing information for basic checkout of the computer. Paragraphs 4-5 through 4-31 give details of the reference information and basic troubleshooting procedures.

4-5. PROGRAM INSTRUCTION FORMATS.

4-6. Program instruction formats are shown in figure 4-1. This figure summarizes information needed for using machine language to program the computer. Bit patterns are shown for the basic instruction set which is comprised of memory reference instructions, input/output instructions, register reference instructions in the shift-rotate group (SRG), register reference instructions in the alter-skip group (ASG), and extended arithmetic instructions (EAG).

4-7. For additional information pertaining to computer machine-language, refer to the 2100A Computer Reference Manual, part no. 02100-90001.

4-8. LOADING ABSOLUTE LOADER PROGRAMS.

4-9. Loading absolute programs into the computer from paper tape requires that a properly configured loader program be stored into the protected area of memory. Two methods are given below for loading the Basic Binary Loader (BBL) program or the Basic Binary Disc Loader (BBDL) program into the protected area of memory.

Note: Either the BBL or the BBDL loader program can be used for loading diagnostic programs. However, the loader program used must also be compatible with the software system used with the computer. Refer to the applicable software and system manuals provided with the computer to determine which loader program should be stored in the protected area of memory.

4-10. LOADING FROM PAPER TAPE. Loading the BBL or BBDL program from paper tape requires that a bootstrap loader program be entered from the operator panel and that a BBL or BBDL program tape be available for reading into core.

4-11. A BBL or BBDL program tape can be generated by using a Bootstrap Loader Generator program tape, which can be ordered from Hewlett-Packard Company. The Bootstrap Loader Generator produces a punched tape containing the computer instructions constituting either the BBL or BBDL program. Also furnished by the program is a typed

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D/I	AND		001	0	Z/C	← Memory Address →									
D/I	XOR		010	0	Z/C										
D/I	IOR		011	0	Z/C										
D/I	JSB		001	1	Z/C										
D/I	JMP		010	1	Z/C										
D/I	ISZ		011	1	Z/C										
D/I	AD*		100	A/B	Z/C										
D/I	CP*		101	A/B	Z/C										
D/I	LD*		110	A/B	Z/C										
D/I	ST*		111	A/B	Z/C										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SRG		000	A/B	0	D/E	*LS		000	†CLE	D/E	‡SL*	*LS		000
				A/B	0	D/E	*RS		001		D/E		*RS		001
				A/B	0	D/E	R*L		010		D/E		R*L		010
				A/B	0	D/E	R*R		011		D/E		R*R		011
				A/B	0	D/E	*LR		100		D/E		*LR		100
				A/B	0	D/E	ER*		101		D/E		ER*		101
				A/B	0	D/E	EL*		110		D/E		EL*		110
				A/B	0	D/E	*LF		111		D/E		*LF		111
				NOP	000				000		000				000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ASG		000	A/B	1	CL*	01	CLE	01	SEZ	SS*	SL*	IN*	SZ*	RSS
				A/B		CM*	10	CME	10						
				A/B		CC*	11	CCE	11						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	IOG		000		1	H/C	HLT		000	← Select Code →					
					1	0	STF		001						
					1	1	CLF		001						
					1	0	SFC		010						
					1	0	SFS		011						
				A/B	1	H/C	MI*		100						
				A/B	1	H/C	LI*		101						
				A/B	1	H/C	OT*		110						
				0	1	H/C	STC		111						
				1	1	H/C	CLC		111						
					1	0	STO		001		000			001	
					1	1	CLO		001		000			001	
					1	H/C	SOC		010		000			001	
					1	H/C	SOS		011		000			001	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	EAG		000	MPY**		000		010			000			000	
				DIV**		000		100			000			000	
				DLD**		100		010			000			000	
				DST**		100		100			000			000	
				ASR		001		000		0	1				
				ASL		000		000		0	1				
				LSR		001		000		1	0	number			
				LSL		000		000		1	0	← of →			
				RRR		001		001		0	0	shifts			
				RRL		000		001		0	0				

Notes: * = A or B, according to bit 11.
D/I, A/B, Z/C, D/E, H/C coded: 0/1.
**Second word is Memory Address.

†CLE: Only this bit is required.
‡SL*: Only this bit and bit 11 (A/B as applicable) are required.

Figure 4-1. Program Instruction Formats

set of instructions for using the tape produced. By employing a bootstrap loader program, the BBL or BBDL tape can be read into the required core locations.

4-12. The bootstrap loader is entered through the DISPLAY REGISTER on the operator panel. It contains the minimum instructions required to read and store the data contained on the BBL and BBDL program tapes. Table 4-1 lists the bootstrap loader and contains a procedure for loading the BBL or BBDL program tapes into memory.

4-13. LOADING FROM THE OPERATOR PANEL. The BBL or BBDL program can be entered through the DISPLAY REGISTER on the operator panel if a BBL or BBDL program tape is not available. Table 4-2 presents octal listings for both the BBL and BBDL programs and contains procedures for loading the programs and verifying the contents in core.

4-14. DIAGNOSTIC OPERATING PROCEDURES.

4-15. GENERAL. Diagnostic checkout consists of running a series of test programs that automatically perform a dynamic test of computer operation by exercising major portions of the circuit functions in the control, arithmetic, memory, and input/output sections. The diagnostic checkout test procedure should be conducted immediately after the computer is installed, as required thereafter as part of a regularly scheduled preventive maintenance program, during troubleshooting, and after making repairs or modifications to the computer. Information and instructions pertinent to performing the diagnostic checkout are presented in paragraphs 4-16 through 4-25 following.

4-16. REQUIRED DIAGNOSTIC PROGRAM TAPES AND PROCEDURES. Diagnostic test programs are stored in absolute form on punched paper tapes. Tapes required for testing are referenced by name and part number in diagnostic program procedures contained in the Manual of Diagnostics. For ease of identification, lables specifying program name and part number are affixed to the storage box containing the tape, and to the beginning of the tape itself.

4-17. The diagnostic program procedures in the Manual of Diagnostics also provide instructions for running the diagnostic test programs. Each procedure within the Manual of Diagnostics is identified by a part number printed on the title page of the document. The names and part numbers of the procedures used for running the test programs that check the basic circuits of the computer are listed in table 4-3.

Note: Diagnostic test procedures for test programs used in testing optional interfacing circuits are referenced in the Operating and Service Manuals furnished with the options.

Table 4-1. Bootstrap Loader Listing

```
000020  1037cc      STC   RDR,C  }
000021  1023cc      SFS   RDR    }  Read first character
000022  024021      JMP   *-1     }
000023  1025cc      LIA   RDR    }
000024  001727      ALF,  ALF    Pack
000025  1037cc      STC   RDR,C  }
000026  1023cc      SFS   RDR    }  Read second character
000027  024026      JMP   *-1     }
000030  1024cc      MIA   RDR    }
000031  170001      STA   1,I
000032  006004      INB
000033  024020      JMP   20B
                RDR EQU   cc
```

LOADING PROCEDURE

To load the Basic Binary Loader (BBL) program tape, or the Basic Binary Disc Loader (BBDL) program tape, using the bootstrap loader program, proceed as follows:

a. Toggle in bootstrap loader program.

b. Load B-register with 0m7700 (octal).

c. Load P-register with 000020 (octal).

d. Place Basic Binary Loader program tape (or Basic Binary Disc Loader program tape) in reader.

e. Press LOADER ENABLE switch on operator panel.

f. Press RUN switch on operator panel.

g. After tape has been read, press HALT/CYCLE switch.

Variables: cc = punched tape reader or teleprinter select code.
m = 0 for 4K, 1 for 8K, 2 for 12K, 3 for 16K, 5 for 24K, 7 for 32K.

4-18. TEST SEQUENCE. The diagnostic checkout procedure for the basic computer is performed using the diagnostic program procedures listed in table 4-3. Using these procedures, and the applicable tape loading procedure presented in paragraphs 4-20 through 4-24, load and run in sequence the alter-skip, memory reference, and shift-rotate test programs. Then load and run in any desired order the remaining test programs listed in table 4-3, followed by the test programs for all optional processing and interfacing circuits installed in the computer. If all test programs run without error, the computer is ready for normal operation.

4-19. ERROR HALTS. If an error halt is encountered in the course of running a diagnostic test program, use the information presented in the diagnostic program procedure to determine which instruction or sequence of instructions in the program the computer failed to process. Then refer to table 4-8 and troubleshoot the circuits associated with the improperly processed instruction.

Table 4-2. Loader Listings and Procedures

Absolute Listing for Basic Binary Loader (BBL) Program

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	063770	106501	004010	002400	006020	063771	073736
0m7710:	006401	067773	006006	027717	107700	102077	027700	017762
0m7720:	002003	027712	003104	073774	017762	017753	070001	073775
0m7730:	063775	043772	002040	027751	017753	044000	dddddd	002101
0m7740:	102000	037775	037774	027730	017753	054000	027711	102011
0m7750:	027700	102055	027700	dddddd	017762	001727	073776	017762
0m7760:	033776	127753	dddddd	1037cc	1023cc	027764	1025cc	127762
0m7770:	173775	153775	1n0100	177765	dddddd	dddddd	dddddd	dddddd

Absolute Listing for Basic Binary Disc Loader (BBDL) Program

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	002401	063726	006700	017742	007306	027713	002006
0m7710:	027703	102077	027700	077754	017742	017742	074000	077757
0m7720:	067757	047755	002040	027740	017742	040001	177757	037757
0m7730:	000040	037754	027720	017742	054000	027702	102011	027700
0m7740:	102055	027700	dddddd	006600	1037cc	1023cc	027745	1074cc
0m7750:	002041	127742	005767	027744	dddddd	1n0100	0200zz	dddddd
0m7760:	107700	063756	102606	002700	1026qq	001500	102602	063777
0m7770:	102702	102602	103706	1027zz	067776	074077	Q24077	177700

Variables

- cc = punched tape reader or teleprinter address
- dddddd = indeterminable (Load all zeros in memory locations designated "indeterminable" when loading. Disregard as insignificant the content of memory locations designated as "indeterminable" when verifying.)
- m = 0 for 4K, 1 for 8K, 2 for 12K, 3 for 16K, 5 for 24K, 7 for 32K
- n = 7 for 4K, 6 for 8K, 5 for 12K, 4 for 16K, 2 for 24K, 0 for 32K
- zz = first disc channel
- qq = second disc channel

LOADING PROCEDURE

To load the protected area of memory, refer to the applicable listing and proceed as follows:

Note

Be sure to use proper values for all variables specified in the listing.

a. Press LOADER ENABLE switch.

b. Press M switch and enter the address of the word to be loaded into the DISPLAY REGISTER.

c. Press MEMORY DATA switch.

d. Enter the instruction into the DISPLAY REGISTER.

e. Press INCREMENT M switch.

f. Enter next instruction into the DISPLAY REGISTER.

g. Repeat steps "e" and "f" for each instruction loaded.

VERIFICATION PROCEDURE

To verify the contents of the protected area in memory, refer to the applicable listing and proceed as follows:

a. Press M switch and enter address of location to be verified into the DISPLAY REGISTER.

b. Press LOADER ENABLE switch.

c. Press MEMORY DATA switch. The content of the memory location selected in step "a" is now indicated by the DISPLAY REGISTER. Each time the INCREMENT M switch is pressed, the content of the next consecutive memory location is displayed.

Table 4-3. Diagnostic Program Tapes and Procedures for Testing the Computer

TEST	PROGRAM PROCEDURE PART NO.
Alter-Skip Instruction Test	02100-90019
Memory Reference Instruction Test	02100-90018
Shift-Rotate Instruction Test	02100-90017
High Memory Address Test	02100-90008
Low Memory Address Test	
High Memory Pattern Test	02100-90023
Low Memory Pattern Test	
Input/Output Interrupt Test	02100-90025
Extended Arithmetic Test	02100-90007
Memory Protect Test	02100-90006
Memory Parity Test	02100-90021
Power Fail with Automatic Restart Test	02100-90020
Direct Memory Access (DMA) Test	12578-90014
Floating-Point Test	02100-90064

4-20. PROCEDURES FOR LOADING DIAGNOSTIC TAPES. Typical input devices that can be used to read test programs from punched paper tapes and transfer them into computer memory include the HP 2748A Punched Tape Reader, the HP 2758A Punched Tape Reader-Reroller, and the HP 2752A Teleprinter.

4-21. Procedures for using these devices are presented in the following paragraphs. For procedures using other devices, refer to the specific manual for the device, or the appropriate system documentation.

4-22. Loading Diagnostic Tapes Using the HP 2748A Tape Reader. The procedure for using the 2748A to load programs from punched paper tapes is as follows:

a. At the tape reader, press the POWER switch to energize the unit.

b. Press the LOAD switch to release the reader pinch roller.

c. Thread the tape through the tape reader as instructed in the 2748A Tape Reader Operating and Service Manual (manual part no. 02748-90023).

d. Press the READ switch. (The tape reader is now ready to read the tape.)

Note: To configure the address specified in step "e" following, replace the variable "m" in the starting address with the number corresponding to the size of computer memory (i.e., 0 for 4K, 1 for 8K, 2 for 12K, 3 for 16K, 5 for 24K, or 7 for 32K).

e. At the operator panel, press the HALT/CYCLE switch if the computer is in the run mode. (The HALT/CYCLE indicator should now be on, and the RUN indicator off.) Press the P switch and enter 0m7700 (the starting address of the loader program stored in the protected area of memory) into the DISPLAY REGISTER.

f. Select the desired tape reading option from table 4-4. Then press the S switch and set DISPLAY REGISTER switches 0 and 15 accordingly. (For the program to be read from the tape and loaded into memory, the "load tape" option must be selected by setting switches 0 and 15 to "0" (off). If the verify checksum or compare options are selected, the program on the tape will be read, but will not be loaded into memory. Note that the BBDL loader program is not capable of performing the "verify checksum" and "compare" options. Therefore, if the BBDL loader program rather than the BBL loader program is residing in the protected area of memory, the "load tape" option is the only option available and must be selected.)

g. Press the LOADER ENABLE switch. Then, in turn, press the INTERNAL PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) while the program tape processes through the tape reader. When the computer halts (RUN indicator off; HALT/CYCLE indicator on), check the DISPLAY REGISTER indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to paragraph 4-25 and table 4-5.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-5 and proceed as directed.

Note: If the paper tape is ejected from the tape reader and the computer does not halt after the tape is read, press and release the HALT/CYCLE switch. Then check the loader program in the protected area

Table 4-4. Tape Reading Options

OPTION	SWITCH REGISTER SETTING	
	BIT 15	BIT 0
Load tape (reads tape and loads contents into memory)	0	0
*Verify checksum (reads tape without loading)	0	1
*Compare the contents of the tape with the contents of memory (reads tape without loading)	1	0/1

* Selectable only in configurations using the HP 2748A or 2758A Punched Tape Reader in conjunction with the BBL loader program.

Table 4-5. Loading Halts

DISPLAY REGISTER CONTENTS	EXPLANATION	REQUIRED ACTION
102077	End-of-tape. Ten consecutive feed frames have been detected and interpreted as an end-of-tape condition.	This indication is normal. Proceed with the applicable procedure for running the program which was loaded into the computer memory.
102011	Checksum error. The A-register contains the checksum from the tape. The B-register contains the computed checksum.	Using the procedures given in paragraphs 4-21 through 4-24, as applicable, reload the program into computer memory. Then execute the checksum option again. If a checksum error still occurs, check the program and/or the computer for the cause of the error.
102055	Address error. An attempt has been made to destroy the loader program, or to load outside the memory limits.	Using the procedures given in paragraphs 4-21 through 4-24, as applicable, recheck all steps and attempt to load the program again. If an address error still occurs, check the program and/or the computer for the cause of the error.
102000	Compare error. The tape being read does not compare with memory. The A-register contains the word from the tape which did not agree.	To find the address of the word in memory which did not compare with the word in the A-register, press the HALT/CYCLE switch twice. The contents of the T-register, minus one, is the address of the word. Using the procedures given in paragraphs 4-21 through 4-24, as applicable, reload the program into computer memory. Then execute the compare option again. If a compare error still occurs, check the program and/or the computer for the cause of the error.

of memory according to the procedure given in table 4-2. If the contents of the protected memory locations are correct, refer to the central processor servicing information and troubleshoot the circuits associated with the halt instruction. If the halt circuits are not the cause of the trouble, refer to the manuals for tape reader and the tape-reader interface and troubleshoot accordingly.

h. At the tape reader, press the LOAD switch to remove the tape from the unit. Then rewind the tape and return it to its storage box.

4-23. Loading Diagnostic Tapes with the HP 2758A Tape Reader-Reroller. The procedure for using the tape reader-reroller to load programs from punched paper tapes is as follows:

a. At the tape reader-reroller, press the POWER switch to energize the unit.

b. Press the LOAD switch to release the reader pinch roller.

c. Thread the tape through the tape reader as instructed in the 2758A Tape Reader-Reroller Operating and Service Manual (manual part no. 02758-90173).

d. Press the READ switch. (The tape reader is now ready to read the tape.)

Note: To configure the address specified in step "e" following, replace the variable "m" in the starting address with the number corresponding to the size of computer memory (i.e., 0 for 4K, 1 for 8K, 2 for 12K, 3 for 16K, 5 for 24K, or 7 for 32K).

e. At the operator panel, press the HALT/CYCLE switch. (The HALT/CYCLE indicator should now be on, and the RUN indicator off.) Press the P switch and enter 0m7700 (the starting address of the loader program stored in the protected area of memory) into the DISPLAY REGISTER.

f. Select the desired tape reading option from table 4-4. Then press the S switch and set DISPLAY REGISTER switches 0 and 15 accordingly. (For the program to be read from the tape and loaded into memory, the "load tape" option must be selected by setting switches 0 and 15 to "0" (off). If the verify checksum or compare options are selected, the program on the tape will be read, but will not be loaded into memory. Note that the BBDL loader program is not capable of performing the "verify checksum" and "compare" options. Therefore, if the BBDL loader program rather than the BBL loader program is residing in the protected area of memory, the "load tape" option is the only option available and must be selected.)

g. Press the LOADER ENABLE switch. Then, in turn, press the INTERNAL PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) while the program tape processes through the tape reader. When the computer halts (RUN indicator off; HALT/CYCLE indicator on), check the DISPLAY REGISTER indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to paragraph 4-25 and table 4-5.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-5 and proceed as directed.

Note: If the paper tape is ejected from the tape reader and the computer does not halt after the tape is read, press and release the HALT/CYCLE switch. Then check the loader program in the protected area of memory according to the procedure given in table 4-2. If the contents of the protected memory locations are correct, refer to the central processor servicing information and troubleshoot the circuits associated with the halt instruction. If the halt circuits are not the cause of the trouble, refer to the manuals for tape reader and the tape-reader interface and troubleshoot accordingly.

h. At the tape reader, press the LOAD switch to remove the tape from the unit. Then rewind the tape and return it to its storage box.

4-24. Loading Diagnostic Tapes Using the HP 2752A Teleprinter. The procedure for using the teleprinter tape reader to load programs from punched paper tapes is as follows:

a. At the teleprinter, set the LINE/OFF/LOCAL switch to LINE.

b. Carefully position the program tape in the teleprinter tape reader.

c. Set the START/STOP/FREE switch to START. (The tape reader is now ready to read the tape.)

Note: To configure the address specified in step "d" following, replace the variable "m" in the starting address with the number corresponding to the size of the computer memory (i.e., 0 for 4K, 1 for 8K, 2 for 12K, 3 for 16K, 5 for 24K, or 7 for 32K).

d. At the operator panel, press the HALT/CYCLE switch. (The HALT/CYCLE indicator should now be on, and the RUN indicator off.) Press the P switch and enter 0m7700 (the starting address of the loader program stored in the protected area of memory) into the DISPLAY REGISTER.

e. Select the desired tape reading option from table 4-4. Then press the S switch and set DISPLAY REGISTER switches 0 and 15 accordingly. (For the program to be read from the tape and loaded into memory, the "load tape" option must be selected by setting switches 0 and 15 to "0" (off). If the verify checksum or compare options are selected, the program on the tape will be read, but will not be loaded into memory. Note that the BBDL loader program is not capable of performing the "verify checksum" and "compare" options. Therefore, if the BBDL loader program rather than the BBL loader program is residing in the protected area of memory, the "load tape" option is the only option available and must be selected.)

f. Press the LOADER ENABLE switch. Then, in turn, press the INTERNAL PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) while the program tape processes through the tape reader. When the computer halts (RUN indicator off; HALT/CYCLE indicator on), check the DISPLAY REGISTER indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to paragraph 4-25 and table 4-5.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-5 and proceed as directed.

Note: If the paper tape is ejected from the tape reader and the computer does not halt after the tape is read, press and release the HALT/CYCLE switch. Then check the loader program in the protected area of memory according to the procedure given in table 4-2. If the contents of the protected memory locations are correct, refer to the central processor servicing

information and troubleshoot the circuits associated with the halt instruction. If the halt circuits are not the cause of the trouble, refer to the manuals for tape reader and the tape-reader interface and troubleshoot accordingly.

g. At the teleprinter, set the START/STOP/FREE switch to STOP, remove the tape from the reader, rewind, and return it to its storage box.

4-25. Loading Halts. After all program data is read from a test tape and transferred into memory, the associated tape reader and the computer will halt with a normal indication of 102077 (end of tape condition) displayed by the DISPLAY REGISTER indicators. This signals the operator to continue with the applicable procedure for running the program now stored in memory. If a halt occurs while a tape is being loaded and an indication other than 102077 is displayed, refer to table 4-5 and proceed as directed.

4-26. MAINTENANCE FEATURES.

4-27. Maintenance features installed at various points in the computer are shown in figure 1-11 and described in table 1-7. Of the maintenance features shown, only six switches are of use for dynamically troubleshooting the computer in a field environment. These switches are the phase loop switch and instruction loop switch on Timing and Control Card A1, the memory test switch and operation loop switch on Operator Panel Card A24, and the HALT/CYCLE (single cycle) switch and INSTRUCTION STEP switch on the operator panel. The various uses of these switches are: to test a particular phase of a specific instruction, to test a specific instruction, to step through an instruction or a series of instructions cycle-by-cycle, to step through a series of instructions one instruction at a time, to repeatedly cycle an operator panel switch operation, and to enter a given data pattern throughout memory (except the protected area). The methods for affecting these various uses are as follows:

a. To test a particular phase of a specific instruction:

(1) Enter the instruction into a memory location.

(2) Set the M- and P-registers to the address of the instruction.

(3) Press the INTERNAL PRESET and EXTERNAL PRESET switches.

(4) If the fetch phase is to be examined, set the phase loop switch on card A1 to the loop position, and press and release the RUN switch.

(5) If a phase other than the fetch phase is to be examined, press and release the HALT/CYCLE switch on the operator panel (this causes the instruction to be processed one cycle at a time) until the phase wanted is indicated by the operator panel indicators FETCH, INDIRECT, or EXECUTE. Then set the phase loop switch to the loop position and press and release the RUN switch.

b. To test a specific instruction:

(1) Enter the instruction into a memory location.

(2) Set the M- and P-registers to the address of the instruction.

(3) Set the instruction loop switch on card A1 to the loop position.

(4) Press and release the RUN switch.

(5) If the results of the operation of the test instruction are to be examined, do not press and release the RUN switch. Press and release the INSTRUCTION STEP switch on the operator panel. Then examine the results via the operator panel register switches and DISPLAY REGISTER indicators.

c. To step through an instruction or a series of instructions cycle-by-cycle:

(1) Set the M- and P-registers to the address of the first instruction of the series.

(2) Press and release the HALT/CYCLE switch on the operator panel. Each time the switch is pressed and released one machine cycle will be processed. An examination of the various registers can be made after the completion of each cycle.

d. To step through a series of instructions one instruction at a time:

(1) Set the M- and P-registers to the address of the first instruction of the series.

(2) Press and release the INSTRUCTION STEP switch on the operator panel. Each time the switch is pressed and released one instruction will be processed. An examination of the various registers can be made after the completion of each instruction.

e. To repeatedly cycle an operator panel switch operation:

(1) Set the operation loop switch on the operator panel card to the loop position.

(2) Press and hold the operator panel switch. The signals generated by the operator panel switch can now be examined.

f. To enter a given data pattern throughout memory (except the protected area):

(1) Press and release the MEMORY DATA switch on the operator panel.

(2) Set the memory test switch on the operator panel card to the inhibit position.

(3) Set the operation loop switch on the operator panel card to the loop position.

(4) Press and hold the operator panel INCREMENT M switch. After approximately one second the pattern loaded into the DISPLAY REGISTER will be contained throughout memory. To check this, set the memory test and operation loop switches back to the normal position, press and release the M-register and MEMORY DATA switches on the operator panel. Then repeatedly press and release the INCREMENT M or DECREMENT M switches on the operator panel and observe the pattern displayed in the DISPLAY REGISTER. The pattern should not change.

4-28. BASIC TROUBLESHOOTING PROCEDURES.

4-29. The following procedures may be used to determine trouble symptoms for fault isolation. The procedures presented here are intended only as a guide for less-experienced maintenance personnel; more-experienced personnel may use their own techniques for troubleshooting. The procedures consist of verifying that the operator panel functions correctly, then loading and running each diagnostic program, in turn, and noting any error halts that may occur while the programs are being run. To perform the basic troubleshooting procedure, proceed as follows:

a. Verify correct operation of the front panel switches. (Refer to table 1-4 for a description of the panel controls and indicators.) If the operation of any switch does not give the proper indication, refer to the operator panel servicing information contained in paragraph 4-168.

b. Try to load the Alter-Skip Diagnostic. If the diagnostic does not load, proceed to step "c". If the diagnostic loads, run the diagnostic and observe any error halts that may occur while the program is being run. An error halt will give the instruction (or group of instructions) that failed. Refer to the central processor servicing information in paragraph 4-32 for troubleshooting any failed instruction. If the program runs without error, proceed to step "d".

c. Try to load the Basic Binary Loader (BBL) or Basic Binary Disc Loader (BBDL) program tape (refer to paragraph 4-8) using the bootstrap loader program listed in table 4-1 as follows:

(1) Starting at address 20, toggle in the bootstrap loader program.

(2) Load 0m7700 into the B-register. Set starting address to 000020.

(3) Load the BBL program tape, or the BBDL program tape, in tape reader. Press LOADER ENABLE switch on operator panel, then press RUN. If the loader program runs, proceed to step "d". If program does not run, verify that the bootstrap loader program is stored correctly. If not, refer to memory section servicing information contained in paragraph 4-122. If bootstrap loader is stored correctly, repeat substep (2) and reload basic binary loader program in tape reader. Press LOADER ENABLE switch and single-cycle through the program to determine which instruction in the bootstrap loader program is failing. After determining which instruction failed, refer to the central processor servicing information in paragraph 4-32 for troubleshooting the failed instruction.

d. Load and run, in sequence, the Memory Reference Diagnostic and the Shift-Rotate Diagnostic, then load and run in any desired order the remaining diagnostic programs listed in table 4-3. Note any error halts that are obtained while the diagnostic is being run, then refer to the central processor servicing information in paragraph 4-32 for troubleshooting failed instructions.

4-30. OVERALL COMPUTER SERVICING DIAGRAM.

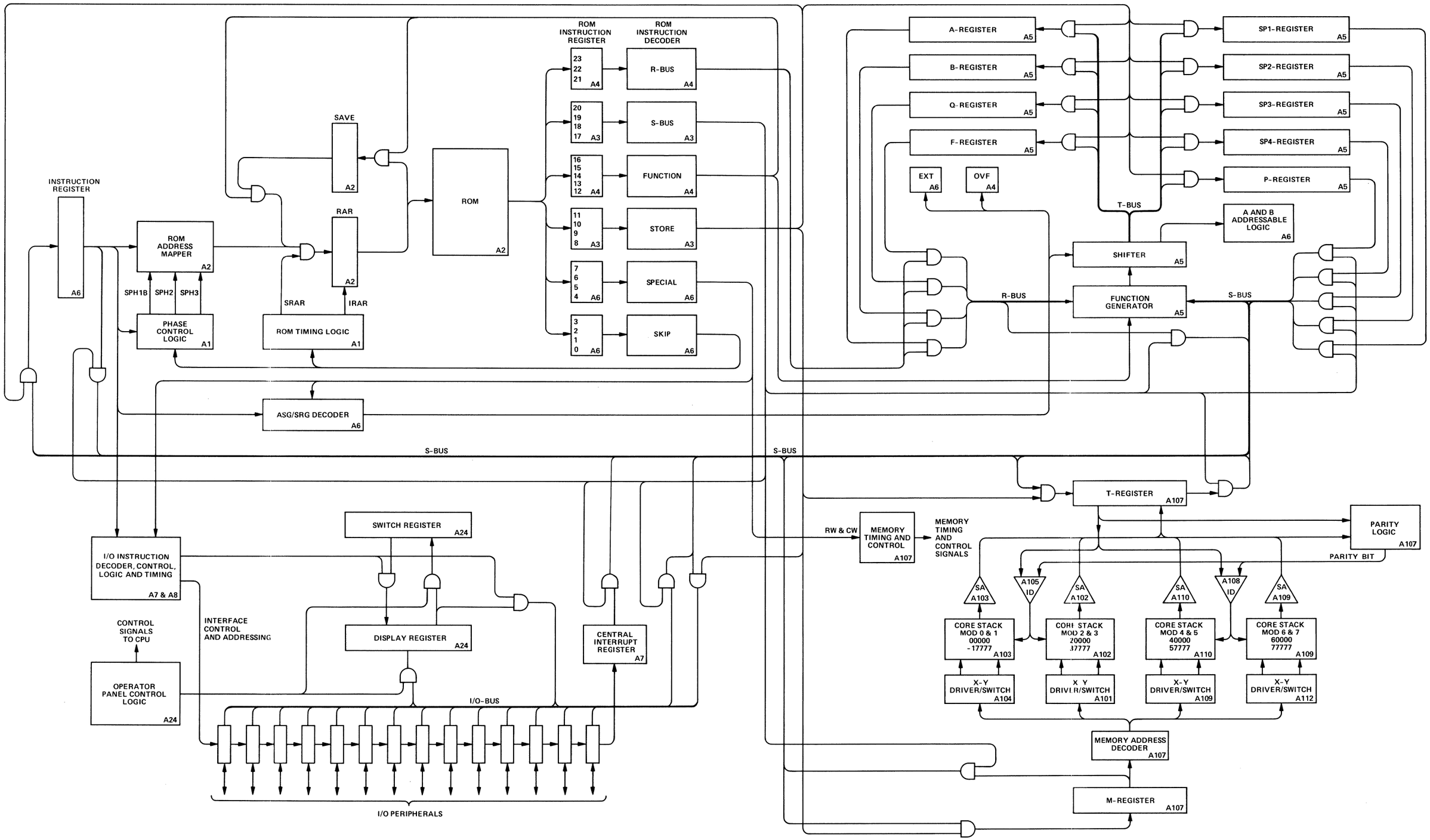
4-31. Figure 4-2 is a servicing diagram representing the major functions of the 2100A Computer and providing card number references for each function. Using figure 4-2, most computer malfunctions can be isolated to a specific function and a card number within the computer card cage.

4-32. CENTRAL PROCESSOR SERVICING.

4-33. The central processor servicing information comprises reference data for fault isolation of failed instructions encountered while performing the diagnostic tests or loading the absolute loader programs. A description of central processor timing specifications is given in paragraph 4-35 and shown in figure 4-3. ROM information, cross-reference from program instruction to ROM address, and the signals necessary to implement the program instructions are given in tables 4-6 through 4-9.

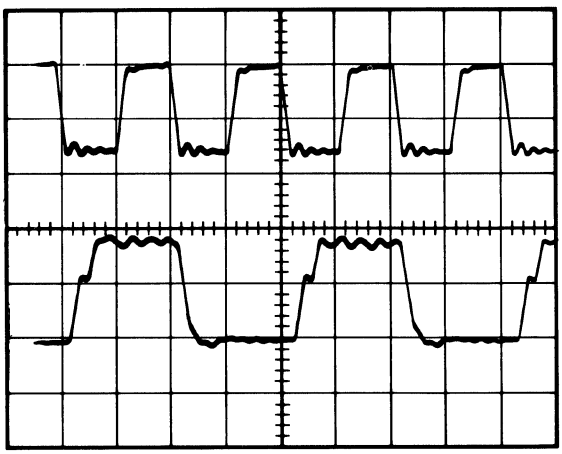
4-34. CENTRAL PROCESSOR TIMING SPECIFICATIONS.

4-35. The central processor contains a 10.204 MHz crystal-controlled oscillator which provides the time base for the entire computer. Synchronization of the central processor with the I/O and memory sections is accomplished by inhibiting the clock signals that operate the central processor while allowing the I/O and memory sections to "catch up". This operation is referred to as a central processor freeze. Figure 4-3 provides details on the five clock signals used throughout the computer. The clock signals designated CLK, CLK1, CLK2, and STCLK are the freezable clocks and appear as shown by figure 4-3 during a central processor freeze. (Paragraph 4-155 gives the oscilloscope settings used to obtain these waveforms. Trace A is the top trace.



2133-21

Figure 4-2. 2100A Computer, Overall Servicing Diagram



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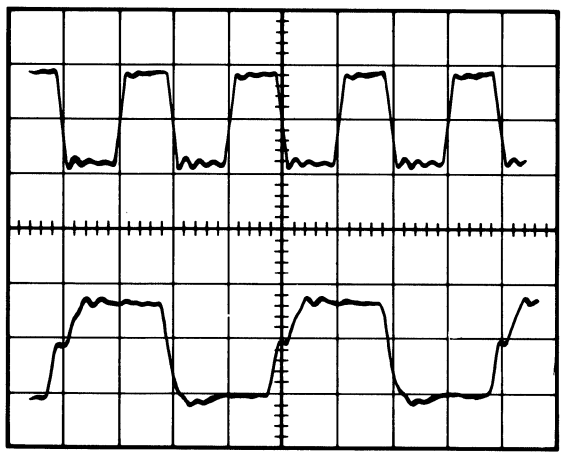
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (10.204 MHz OSC.):
Input . . . . . Test Point A1-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (CLK):
Input . . . . . Test Point A1-E1
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

10.204 MHz Oscillator Output and Signal CLK Waveform



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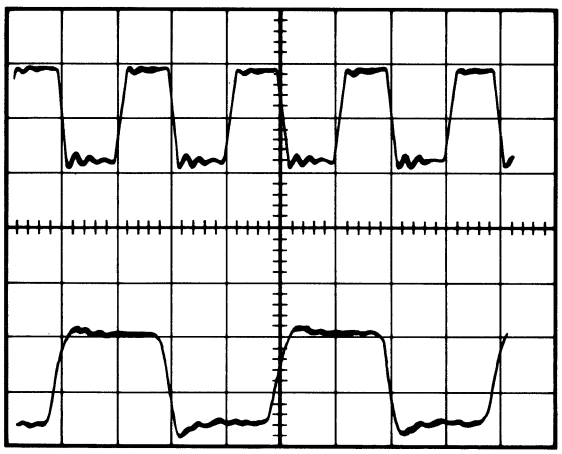
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (10.204 MHz OSC.):
Input . . . . . Test Point A1-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{CLK2}}$):
Input A1-84
Volts/cm . . . . . (if using 10:1 probe)

Time/cm . . . . . 0.05 us

10.204 MHz Oscillator Output and Signal $\overline{\text{CLK2}}$ Waveforms



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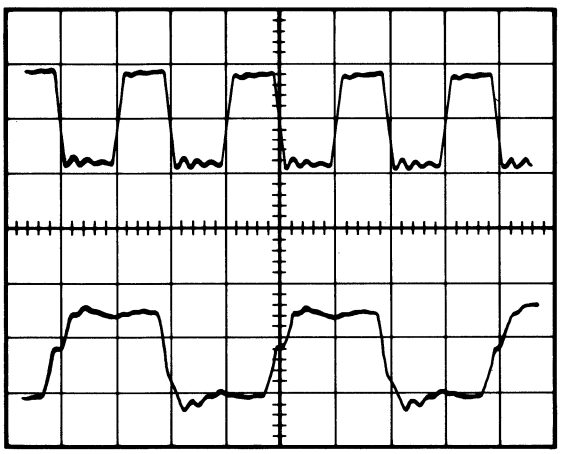
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (10.204 MHz OSC.):
Input . . . . . Test Point A1-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{CLK1}}$):
Input A1-72
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

20.204 MHz Oscillator Output and Signal $\overline{\text{CLK1}}$ Waveforms



2133-145

OSCILLOSOCPE CONNECTIONS & SETTINGS

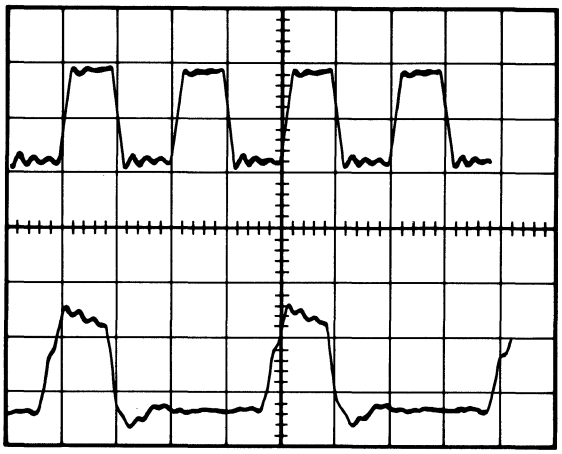
Channel A (10.204 MHz OSC.):
Input . . . . . Test Point A1-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{CLK3}}$):
Input A1-78
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

10.204 MHz Oscillator Output and Signal $\overline{\text{CLK3}}$ Waveforms

Figure 4-3. Central Processor Clock Signals Timing (Sheet 1 of 2)

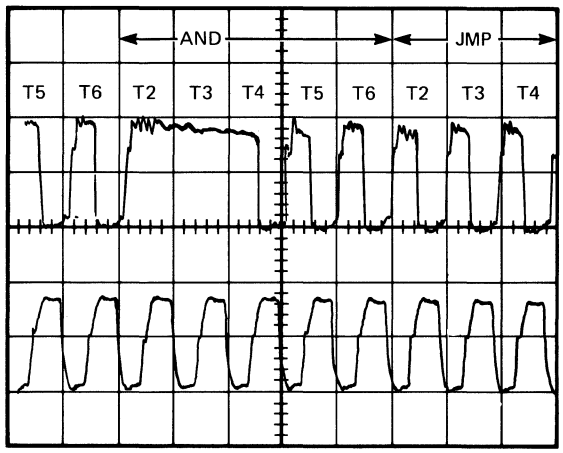


2133-146

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (10.204 MHz OSC.):
Input . . . . . Test Point A1-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (STCLK):
Input A1-36
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.05 us

10.204 MHz Oscillator Output and Signal STCLK Waveforms

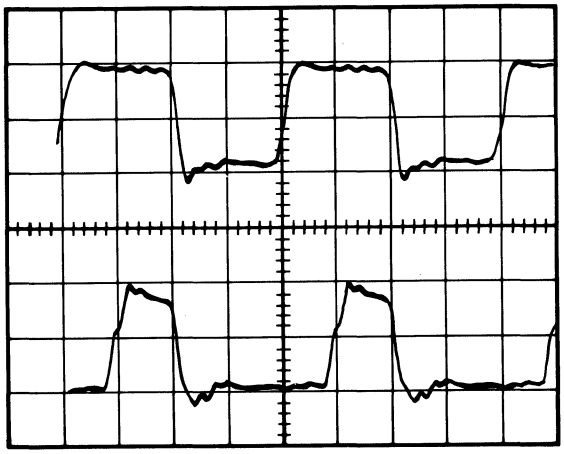


2133-148

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (CLK):
Input A1-E1
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{CLK3}$):
Input A1-E6
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.5 us

Signals CLK and $\overline{CLK3}$ Waveforms Showing Central Processor Freeze (using AND and JMP instructions)

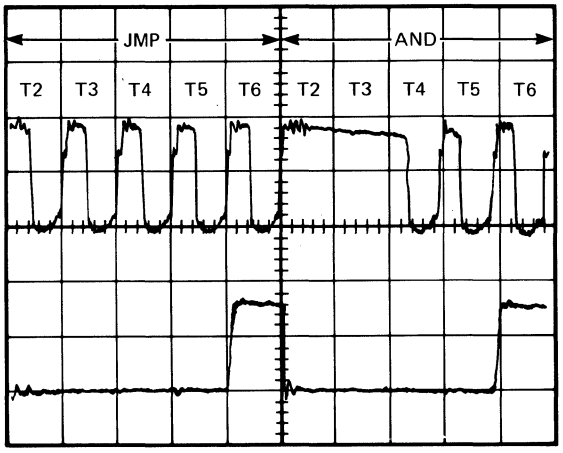


2133-149

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{CLK1}$):
Input A1-72
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (STCLK):
Input A1-36
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.05 us

Signals $\overline{CLK1}$ and STCLK Waveforms



2133-147

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (CLK):
Input A1-E1
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.5 us

Signals CLK and T6 Waveforms Showing Central Processor Freeze (using AND and JMP instructions)

Figure 4-3. Central Processor Clock Signals Timing (Sheet 2 of 2)

Table 4-6. Consolidated Coding of ROM Microcodes

CODE					R-BUS FIELD (3 BITS) 23 thru 21	S-BUS FIELD (4 BITS) 20 thru 17	FUNCTION FIELD (5 BITS) 16 thru 12	STORE FIELD (4 BITS) 11 thru 8	SPECIAL FIELD (4 BITS) 7 thru 4	SKIP FIELD (4 BITS) 3 thru 0
5-BIT FIELD										
	4-BIT FIELD									
		3-BIT FIELD								
1	1	1	1	1	NOP	NOP	IOR	NOP	NOP	NOP
1	1	1	1	0	*CQ	P	SOV	A	RW	UNC
1	1	1	0	1	AAB	CL	CLO	B	IOG1	EOP
1	1	1	0	0	CAB	CR	SFLG	AAB	CW	NAAB
1	1	0	1	1	F	S1	CFLG	CAB	ASG2	AAB
1	1	0	1	0	Q	S2	LWF	Q	ASG1	NMPV
1	1	0	0	1	B	S3	–	F	ECYN	CTR
1	1	0	0	0	A	S4	ARS	P	ECYZ	CTRI
1	0	1	1	1	–	COND	CRS	S1	LEP	TBZ
1	0	1	1	0	–	ADR	LGS	S2	AAB	FLG
1	0	1	0	1	–	CNTR	RSB	S3	SRG2	OVF
1	0	1	0	0	–	RRS	CJMP	S4	SRG1	COUT
1	0	0	1	1	–	M	JMP	IR	CNTR	NEG
1	0	0	1	0	–	T	JMP	T	R1	ODD
1	0	0	0	1	–	IOI	JSB	M	L1	RPT
1	0	0	0	0	–	CIR	JSB	IOO	RSS	ICTR
0	1	1	1	1	–	–	–	–	–	–
0	1	1	1	0	–	–	XOR	–	–	–
0	1	1	0	1	–	–	NOR	–	–	–
0	1	1	0	0	–	–	AND	–	–	–
0	1	0	1	1	–	–	ADD	–	–	–
0	1	0	1	0	–	–	ADDO	–	–	–
0	1	0	0	1	–	–	INC	–	–	–
0	1	0	0	0	–	–	INCO	–	–	–
0	0	1	1	1	–	–	–	–	–	–
0	0	1	1	0	–	–	DEC	–	–	–
0	0	1	0	1	–	–	SUB	–	–	–
0	0	1	0	0	–	–	DIV	–	–	–
0	0	0	1	1	–	–	MPY	–	–	–
0	0	0	1	0	–	–	*P1A	–	–	–
0	0	0	0	1	–	–	RFE	–	–	–
0	0	0	0	0	–	–	*RFI	–	–	–

*Reserved code for special maintenance by HP Service personnel.

Table 4-7. ROM Microcode Descriptions

FIELD CODES	DESCRIPTION
	R-BUS FIELD
A	Reads the A-register onto the R-bus.
AAB	Reads the A-register or B-register onto the R-bus, depending on whether the A Addressable FF or B Addressable FF is set. (Both FFs cannot be set at the same time.) If neither FF is set, the A-register will be read onto the R-bus unless COND is present in the S-Bus field (RBE signal will be true).
B	Reads the B-register onto the R-bus.
CAB	Reads the A-register or B-register onto the R-bus, depending on whether the I-register bit 11 is a "0" or a "1". (If "0", then the A-register will be read; if "1", then the B-register will be read.)
CQ	If the I-register bit 9 is a "1" and the Index Mode FF is set, reads the Q-register onto the R-bus.
F	Reads the Fence (F-) register onto the R-bus.
NOP	No operation; results in all "0's" on the R-bus.
Q	Reads the Q-register onto the R-bus.
	S-BUS FIELD
ADR	Reads the current operand address onto the S-bus. The operand address consists of I-register bits 0 thru 8, I-register bit 9 (if the Index Mode FF is cleared), or P-register bit 9 (if the Index Mode FF is set and I-register bit 10 is a "1"), and P-register bits 10 thru 15 (if I-register bit 10 is a "1") or "0's" (if I-register bit 10 is a "0").
CIR	Reads the Central Interrupt Register onto the S-bus during I/O time T6.
CL	Reads a constant onto the left-half (bits 8 thru 15) of the S-bus. The constant is obtained from bits 0 thru 7 of the ROM Instruction Register. Execution of the SKIP and SPECIAL fields is inhibited. Reads "0's" onto the right-half (bits 0 thru 7) of the S-bus.
CNTR	Reads the Repeat Counter bits 0 thru 4 onto S-bus bits 0 thru 4.
COND	If A Addressable FF is set, reads A-register onto the S-bus. If B Addressable FF is set, reads B-register onto the S-bus. If neither FF is set, reads the T-register onto the S-bus.
CR	Reads a constant onto the right-half (bits 0 thru 7) of the S-bus. The constant is obtained from bits 0 thru 7 of the ROM Instruction Register. Execution of the SKIP and SPECIAL fields is inhibited. Reads "0's" onto the left-half (bits 8 thru 15) of the S-bus.
IOI	Reads the I/O-bus onto the S-bus.
M	Reads the M-register onto the S-bus.
NOP	No operation; results in all "0's" on the S-bus.
P	Reads the P-register onto the S-bus.
RRS	Reads R-bus onto the S-bus.
S1	Reads scratch-pad 1 onto the S-bus.
S2	Reads scratch-pad 2 onto the S-bus.
S3	Reads scratch-pad 3 onto the S-bus.
S4	Reads scratch-pad 4 onto the S-bus.
T	Reads the T-register (memory data) onto the S-bus.

Table 4-7. ROM Microcode Descriptions (Continued)

FIELD CODES	DESCRIPTION
	FUNCTION FIELD
ADD	Adds the R-bus and S-bus.
ADDO	Adds the R-bus and S-bus. Enables the "not" Overflow FF logic. If a memory reference group instruction is detected, or ASG2 is present in the SPECIAL field, enables the Extend FF logic.
AND	Logical AND of the R-bus and S-bus.
ARS	32-bit arithmetic shift. The direction of shift is specified in the SPECIAL field (L1 or R1). If a right-shift, the sign is copied into "hi-bit" register bit 14, and "lo-bit" register bit 0 is lost. If a left-shift, the sign is copied into "hi-bit" register bit 15 and bit 14 is lost. A "0" is shifted into "lo-bit" register bit 0. Also if a left-shift, the "not" Overflow FF is cleared if ALU bit 14 or ALU bit 15 is a "1" (but not both). Enables the ALU Inclusive OR function. Note On right-shifts, the A-register and B-register must be used. The A-register contains the "lo-bits" (least significant bits), and the B-register contains the "hi-bits" (most significant bits). On left-shifts, the Q-register and F-register must be used. The Q-register contains the "lo-bits", and the F-register contains the "hi-bits".
CFLG	Clears the CPU Flag FF; enables the ALU Inclusive OR function.
CJMP	Conditional jump. Executes a jump if, in the run mode, an interrupt or an operator panel halt command is detected. Otherwise, the instruction is treated as an IOR. The jump address must be within the lowest 512 words of ROM. In the single-cycle mode, the detection of CJMP will cause the computer to halt unconditionally. The execution of the SPECIAL and SKIP fields is inhibited, and the execution of P in the S-BUS field is inhibited.
CLO	Sets the "not" Overflow FF; enables the ALU Inclusive OR function.
CRS	32-bit circular shift (rotate). (See the note above.) The direction of shift is specified in the SPECIAL field (L1 or R1). If a right-shift, "lo-bit" register bit 0 is transferred to "hi-bit" register bit 15. If a left-shift, "hi-bit" register bit 15 is transferred to "lo-bit" register bit 0. Enables the ALU Inclusive OR function.
DEC	One's complement subtract of the S-bus from the R-bus. (If the S-bus contains all "0's", the R-bus is decremented.
DIV	Divide step (normally in a repeat loop). Normally entered with the dividend most significant bit in the F-register, the least significant bit in the Q-register, and the divisor in a scratch-pad. Exits with the quotient in the Q-register and the remainder in the F-register. Subtracts the S-bus from the R-bus (2's complement and check COUT signal.) If COUT is a "1", shifts the ALU output left one and stores the result in the F-register. The Q-register shifts left one. Q-register bit 15 is read into F-register bit 0; COUT is read into Q-register bit 0, and F-register bit 15 is lost. If COUT is a "0", the shift-left mode of the F- and Q-registers is enabled (the T-bus is not stored). Q-register bit 15 is read into F-register bit 0; a "0" is read into Q-register bit 0, and F-register bit 15 is lost.

Table 4-7. ROM Microcode Descriptions (Continued)

FIELD CODES	DESCRIPTION
	FUNCTION FIELD (Continued)
INC	Increments the sum of the R-bus and S-bus.
INCO	Increments the sum of the R-bus and S-bus. Enables the "not" Overflow FF logic and the Extend FF logic.
IOR	Logical Inclusive OR of the R-bus and S-bus.
JMP	Jump. Results in an unconditional branch to the address contained in bits 0 thru 7 of the ROM Instruction Register (RIR). (RIR bits 0 thru 7 are transferred to ROM Address Register bits 0 thru 7). If 512 words of ROM are used, RIR bit 7 is the most significant bit of the address (execution of P in the S-BUS field is inhibited). (RIR bit 17 is transferred to ROM Address Register bit 8.) If 1K words of ROM are used, then RIR bit 12 (from the FUNCTION field) is the most significant bit of the address. (RIR bit 12 is transferred to ROM Address Register bit 9). The least significant bit of the JMP code specifies whether the jump is to the lower (a "0") or the upper (a "1") 512 words of ROM. The execution of the SPECIAL and SKIP fields is inhibited, and the execution of P in the S-BUS field is inhibited. Enables the ALU exclusive OR function. The enable ROM (ENRM) signal is inhibited which results in storing all "1's" in the RIR. This, in turn, causes an NOP on the following cycle.
JSB	Jump to ROM subroutine. The address of the jump is specified by ROM Instruction Register (RIR) bits 0 thru 7. (RIR bits 0 thru 7 are transferred to RAR bits 0 thru 7.) If 512 words of ROM are used, RIR bit 17 is the most significant bit of the address (execution of P in the S-BUS field is inhibited). (RIR bit 17 is transferred to ROM Address Register bit 8.) If 1K words of ROM are used, then RIR bit 12 (from the FUNCTION field) is the most significant bit of the address. (RIR bit 12 is transferred to ROM Address Register bit 9.) The least significant bit of the JSB code specifies whether the jump is to the lower (a "0") or the upper (a "1") 512 words of ROM. The "not" JSB FF is cleared, storing the current contents of the ROM Address Register (the return address) in the Save register. The execution of the SPECIAL and SKIP fields is inhibited, and the execution of P in the S-BUS field is inhibited. The enable ROM (ENRM) signal is inhibited which results in storing all 1's in the ROM Instruction Register. This, in turn, causes an NOP on the following cycle. The ALU Inclusive OR function is enabled.
LGS	32-bit logical shift. (See the preceding note.) The direction of shift is specified in the SPECIAL field (L1 or R1). If a right-shift, "hi-bit" register bit 15 is a "0", and "lo-bit" register bit 0 is lost. If a left-shift, "lo-bit" register bit 0 is a "0", and "hi-bit" register bit 15 is lost. Enables the Inclusive OR function.

Table 4-7. ROM Microcode Descriptions (Continued)

FIELD CODES	DESCRIPTION
	FUNCTION FIELD (Continued)
LWF	Link with flag. If L1 is coded in the SPECIAL field, the content of the CPU Flag FF is transferred to the left-shift input (LSI) of the T-bus shifter, thereby transferring its content to T-bus bit 0, and ALU bit 15 is transferred to the CPU Flag FF. If R1 is coded in the SPECIAL field, the content of the CPU Flag FF is transferred to the right-shift input (ALX16) of the T-bus shifter, thereby transferring its content to T-bus bit 15, and ALU bit 0 is transferred to the CPU Flag FF. Enables the ALU inclusive OR function.
MPY	Multiply step (normally in a repeat loop). Normally entered with the multiplier in the A-register, the multiplicand in a scratch-pad, and the B-register cleared. If A-register bit 0 is a "1", adds the R-bus and S-bus, shifts the result right one and places it on the T-bus. The COUT signal is read into T-bus bit 15, and ALU bit 0 is read into A-register bit 15. The T-bus bits 0 thru 15 are stored in the B-register. The A-register is shifted right one, and A-register bit 0 is lost. If A-register bit 0 is a "0", shifts the R-bus contents right one and places it on the T-bus. The COUT signal is read into T-bus bit 15, and ALU bit 0 is read into A-register bit 15. The T-bus bits 0 thru 15 are stored in the B-register. The A-register is shifted right one, and A-register bit 0 is lost.
NOP	Logical NOR of the R-bus and S-bus. (Note that by causing an NOP of one bus, the complement of the other is obtained.)
P1A	Sets Phase 1A and clears the current phase.
RFE	Rotates the CPU Flag and Extend FFs. The state of the CPU Flag FF is read into the Extend FF, and the state of the Extend FF is read into the CPU Flag FF.
RFI	Rotates the CPU Flag and Index Mode FFs. The state of the CPU Flag FF is read into the Extend FF, and the state of the Extend FF is read into the CPU Flag FF.
RSB	Return from ROM subroutine. Results in an unconditional branch to the address contained in Save Register bits 0 thru 9. (Save register bits 0 thru 9 are transferred to ROM Address Register bits 0 thru 9). Inhibits ROM enable. (Results in storing all "1's" in the ROM Instruction Register which causes an NOP on the following cycle.) Enables the Inclusive OR function. Sets the "not" JSB FF.
SFLG	Sets the CPU Flag FF; enables the ALU Inclusive OR function.
SOV	Clears the "not" Overflow FF; enables the ALU Inclusive OR function.
SUB	Two's complement subtract of the S-bus from the T-bus.
XOR	Logical Exclusive OR of the R-bus and S-bus.
	STORE FIELD
A	Stores the T-bus into the A-register.
AAB	Stores the T-bus into the A- or B-register, depending on whether the A Addressable FF or B Addressable FF is set. If neither FF is set, no store will occur.
B	Stores the T-bus into the B-register.
CAB	Stores the T-bus into the A- or B-register depending on whether the I-register bit 11 is a "0" or "1", respectively.
F	Stores the T-bus into the F-register.
IOO	Reads the S-bus onto the I/O bus.

Table 4-7. ROM Microcode Descriptions (Continued)

FIELD CODES	DESCRIPTION
	STORE FIELD (Continued)
IR	Stores the S-bus into the I-register.
M	Stores the S-bus into the M-register, and in the Violation Register if computer is in Phase 1A, memory protect mode is set, a no parity error exists.
NOP	No store.
P	Stores the T-bus into the P-register.
Q	Stores the T-bus into the Q-register.
S1	Stores the T-bus into scratch-pad 1.
S2	Stores the T-bus into scratch-pad 2.
S3	Stores the T-bus into scratch-pad 3.
S4	Stores the T-bus into scratch-pad 4.
T	Stores the S-bus into the T-register.
	SPECIAL FIELD
AAB	If the AAB signal is true, enables setting of the A Addressable FF or B Addressable FF, depending on whether ALU bit 0 is a "0" or "1", respectively.
ASG1	Enables skip and extend logic defined by I-register bits 0, and 3 thru 7.
ASG2	Enables skip and increment logic defined by I-register bits 0 thru 2.
CNTR	Stores S-bus bits 0 thru 3 into the Repeat Counter.
CW	Clear-Write memory cycle. CPU freezes until I/O time T6, then commands memory to begin a "write" cycle. Data present in the T-register is stored into memory at the end of the memory cycle. The Memory Busy FF is then cleared. CW is normally enabled by NMPV in the SKIP field.
ECYN	Enables the Carry FF logic. If the T-bus contains any "1's", sets the Carry FF.
ECYZ	Enables the Carry FF logic. If the T-bus contains all "0's", sets the Carry FF.
IOG1	Synchronizes CPU with I/O timing. Decodes I/O Group instructions from I-register during appropriate time intervals.
LEP	Legal entry point. Prevents illegal entry into ROM through an incorrect macroinstruction. Causes the CPU to NOP until LEP is detected, or until EOP is detected in the SKIP field.
L1	Enables the shift-left-one input to the T-bus shifter.
NOP	No operation.
RSS	Reverses the skip sense of the SKIP field functions.
RW	Read-Write memory cycle. CPU freezes until I/O time T6, then commands memory to begin a "read" cycle and sets the Memory Busy FF. Memory output data is stored into the T-register. The Data Ready FF is set to indicate to the CPU that data is available. A true AAB signal indicates that the data is contained in the A- or B-register.
R1	Enables the shift-right-one input to the T-bus shifter.
SRG1	Enables shift-rotate group functions defined by I-register bits 6 thru 9. Sets the SRG FF; enables CLE and SL* instruction logic during the next cycle.
SRG2	Enables shift/rotate group functions defined by I-register bits 0 thru 2, and 4.

Table 4-7. ROM Microcode Descriptions (Continued)

FIELD CODES	DESCRIPTION
	SKIP FIELD
AAB	Skips the next ROM microinstruction if either the A Addressable FF or the B Addressable FF is set.
COUT	Skips the next ROM microinstruction if "not" Carry Out signal is false.
CTR	Skips the next ROM microinstruction if the Repeat Counter contains all "1's" (ignores bit 4).
CTRI	Skips the next ROM microinstruction if the Repeat Counter contains all "1's" (ignores bit 4), then increments the counter.
EOP	End of Phase. Executes a hardware jump through the ROM mapper to the ROM address at the beginning of the next phase. Sets the proper phase FF and clears the "not" JSB FF.
FLG	Skips the next ROM microinstruction if the CPU Flag FF is set.
ICTR	Increments the Repeat Counter.
NAAB	Skips the next ROM microinstruction if the T-bus bits 1 thru 14 are not equal to zero. (Normally used to check the status of the A Addressable and B Addressable FFs.)
NEG	Skips the next ROM microinstruction if the ALU output is negative (ALU bit 15 is a "1").
NMPV	If Memory Protect is disabled, or if there is no memory protect violation (ALU bit 15 is a "1"), and if the A- or B-registers are not addressed, then skip the next ROM microinstruction.
NOP	No operation.
ODD	Skips the next ROM microinstruction if the ALU output is odd (ALU bit 0 is a "1").
OVF	Skips the next ROM microinstruction if the "not" Overflow FF is cleared.
RPT	Clears the Repeat FF and causes the next ROM microinstruction to be repeated until a skip condition is met.
TBZ	Skips the next ROM microinstruction if the T-bus contains all "0's".
UNC	Skip the next ROM microinstruction, unconditionally.

Table 4-8. Cross Reference of Basic Instruction to ROM Address

TYPE	BASIC COMPUTER INSTRUCTION	ROM STARTING ADDRESS	ROM MICROINSTRUCTION MNEMONIC
Memory Reference	AND	110	AND
	XOR	120	XOR
	IOR	130	IOR
	JSB	150	JSB
	JMP	124	JMP
	ISZ	170	ISZ
	ADA/B	144	ADD
	CPA/B	114	CP*
	LDA/B	164	LD*
	STA/B	134	ST*
Register Reference	Shift-Rotate Group		
	NOP	100	SRGA
	CLE	100	SRGA
	SLA/B	100/104	SRGA/SRGB
	A/BLS	100/104	SRGA/SRGB
	A/BRS	100/104	SRGA/SRGB
	RA/BL	100/104	SRGA/SRGB
	RA/BR	100/104	SRGA/SRGB
	A/BLR	100/104	SRGA/SRGB
	ERA/B	100/104	SRGA/SRGB
	ELA/B	100/104	SRGA/SRGB
	A/BLF	100/104	SRGA/SRGB
	Alter-Skip Group		
	CLA/B	25	ASGA
	CMA/B	31	ASGB
	CCA/B	35	ASGC
	CLE	21	ASGD
	CME	21	ASGD
	CCE	21	ASGD
	SEZ	21	ASGD
	SSA/B	21	ASGD
	SLA/B	21	ASGD
	INA/B	21	ASGD
	SZA/B	21	ASGD
	RSS	21	ASGD
Input/ Output	HLT	40	FLAG
	STF	40	FLAG
	CLF	40	FLAG
	SFC	40	FLAG
	SFS	40	FLAG
	MIA/B	60	MI*
	LIA/B	64	LI*
	OTA/B	70	OT*
	STC	74	CTRL
	CLC	74	CTRL
	STO	40	FLAG
	CLO	40	FLAG
	SOC	40	FLAG
	SOS	40	FLAG
Arithmetic Function	ASL	201	ASL
	ASR	241	ASR
	DIV	220	DIVID
	DLD	310	DLD
	DST	320	DST
	LSL	202	LSL
	LSR	242	LSR
	MPY	210	MULT
	RRL	204	RRL
	RRR	244	RRR

Table 4-9. ROM Program Listing

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0000	77330757	PH1A	–	P	CFLG	M	RW	–	Send current instruction address to memory, start read cycle.
0001	53771775		AAB	COND	IOR	IR	–	EOP	Put instruction from memory or A/B into I-register,set next phase.
0002	73373557		–	ADR	IOR	S1	AAB	–	If instruction is MRG, put operand address in S1, else NOP.
0004	70330757	PH1B	–	CIR	CFLG	M	RW	–	Send interrupt address to memory and start read cycle.
0005	77054377		–	P	SUB	P	–	–	Decrement the
0006	77154377		–	P	NOR	P	–	–	P-register.
0007	53771775		AAB	COND	IOR	IR	–	EOP	Put trap cell instruction into I-register and set next phase.
0010	73373557		–	ADR	IOR	S1	AAB	–	If MRG, put operand address in S1, else NOP.
0011	77054375	PDEC	–	P	SUB	P	–	EOP	Decrement the P-register and
0012	77154377		–	P	NOR	P	–	–	set next phase.
0014	75770757	PH2	–	S1	IOR	M	RW	–	Send indirect address to memory, start read cycle.
0015	53773775		AAB	COND	IOR	S1	–	EOP	Put operand address in S1 (also may be indirect), set next phase.
0016	75777557		–	S1	IOR	–	AAB	–	Test operand address for A- or B-register.
0017	45167635	XX	CAB	S2	XOR	–	ECYN	EOP	Exclusive-OR the contents of A/B-register with S2 and set
0020	77777777		–	–	IOR	–	–	–	Carry if result is non-zero. Set next phase.
0021	47777657	ASGD	CAB	–	IOR	–	ASG1	–	Executes the ASG instructions where I-register bits 8:9 = 0.
0022	47525675		CAB	–	ADDO	CAB	ASG2	EOP	
0023	77777777		–	–	IOR	–	–	–	
0025	77775657	ASGA	–	–	IOR	CAB	ASG1	–	Executes the ASG instructions where I-register bits 8:9
0026	47525675		CAB	–	ADDO	CAB	ASG2	EOP	indicate CLA/B.
0027	77777777		–	–	IOR	–	–	–	
0031	47555657	ASGB	CAB	–	NOR	CAB	ASG1	–	Executes the ASG instructions where I-register bits 8:9
0032	47525675		CAB	–	ADDO	CAB	ASG2	EOP	indicate CMA/B.
0033	77777777		–	–	IOR	–	–	–	
0035	77555657	ASGC	–	–	NOR	CAB	ASG1	–	Executes the ASG instructions where I-register bits 8:9
0036	47525675		CAB	–	ADDO	CAB	ASG2	EOP	indicate CCA/B.
0037	77777777		–	–	IOR	–	–	–	
0040	77777737	FLAG	–	–	IOR	–	IOG1	–	Synchronize CPU to I/O time T2. Executes the IOG instructions
0041	77777777		–	–	IOR	–	–	–	HLT, STF, CLF, SFS, SFC, SOS, SOC.
0042	77777775		–	–	IOR	–	–	EOP	
0043	77777777		–	–	IOR	–	–	–	
0060	77777737	MI*	–	–	IOR	–	IOG1	–	Synchronize CPU to I/O time T2. Executes the IOG instructions
0061	77777777		–	–	IOR	–	–	–	MIA and MIB.
0062	70777775		–	IOI	IOR	–	–	EOP	
0063	40775777		CAB	IOI	IOR	CAB	–	–	
0064	77777737	LI*	–	–	IOR	–	IOG1	–	Synchronize CPU to I/O time T2. Executes the IOG instructions
0065	77777777		–	–	IOR	–	–	–	LIA and LIB.
0066	70777775		–	IOI	IOR	–	–	EOP	
0067	70775777		–	IOI	IOR	CAB	–	–	
0070	77777737	OT*	–	–	IOR	–	IOG1	–	Synchronize CPU to I/O time T2. Executes the IOG instructions
0071	42377777		CAB	RRS	IOR	–	–	–	OTA and OTB.
0072	42370375		CAB	RRS	IOR	IOO	–	EOP	
0073	42370377		CAB	RRS	IOR	IOO	–	–	
0074	77777737	CTRL	–	–	IOR	–	IOG1	–	Synchronize CPU to I/O time T2. Executes the IOG instructions
0075	77777777		–	–	IOR	–	–	–	STC, CLC, SOV, CLO.
0076	77777775		–	–	IOR	–	–	EOP	
0077	77777777		–	–	IOR	–	–	–	
0100	07777117	SRGA	A	–	IOR	A	SRG1	–	Executes the SRG instructions involving the A-register.
0101	07777777		A	–	IOR	–	–	–	
0102	07777135		A	–	IOR	A	SRG2	EOP	
0103	77777777		–	–	IOR	–	–	–	

Table 4-9. ROM Program Listing (Continued)

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0104	17776517	SRGB	B	–	IOR	B	SRG1	–	Executes the SRG instructions involving the B-register.
0105	17777777		B	–	IOR	–	–	–	
0106	17776535		B	–	IOR	B	SRG2	EOP	
0107	77777777		–	–	IOR	–	–	–	
0110	75770757	AND	–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0111	53773375		AAB	COND	IOR	S2	–	EOP	Put data from operand address into S2. Set next phase.
0112	05147377		A	S2	AND	A	–	–	AND operand data with A-register, put result back in A-register.
0114	75770754	CP*	–	S1	IOR	M	RW	NAAB	Send operand address to memory, start read cycle. Skip next line if operand address in S1 is not A/B-register.
0115	57223017		AAB	–	JMP	S2	XX	–	Put A/B-register contents into S2 and jump to 0017.
0116	41167635		CAB	T	XOR	–	ECYN	EOP	Exclusive-OR operand with A/B-register (depending on IR11),
0117	77777777		–	–	IOR	–	–	–	set Carry if result is non-zero. Set next phase.
0120	75770757	XOR	–	S1	IOR	M	RW	–	Send operand address to memory, start read cycle.
0121	53773375		AAB	COND	IOR	S2	–	EOP	Put operand data into S2. Set next phase.
0122	05167377		A	S2	XOR	A	–	–	Exclusive-OR S2 with A-register, put result in A-register.
0124	77557557	JMP	–	–	NOR	–	AAB	–	Clear AAF and BAF.
0125	35467412		F	S1	DEC	–	RSS	NMPV	Test jump address in S1, skip next line if violation is detected and if memory protect is enabled.
0126	75774375		–	S1	IOR	P	–	EOP	Put jump address in P-register and set next phase.
0127	77777777		–	–	IOR	–	–	–	
0130	75770757	IOR	–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0131	53773375		AAB	COND	IOR	S2	–	EOP	Put operand data into S2. Set next phase.
0132	05377377		A	S2	IOR	A	–	–	OR operand in S2 with A-register, put result in A-register.
0134	35460712	ST*	F	S1	DEC	M	CW	NMPV	Test operand address. If no violation is detected, start memory clear/write cycle and skip next line.
0135	42376376		CAB	RRS	IOR	AAB	–	UNC	Put A/B-register data (per IR11) into A/B-register (per AAF/BAF) and skip next line.
0136	42371375		CAB	RRS	IOR	T	–	EOP	Put A/B-register data (per IR11) into T-register for storage into
0137	77777777		–	–	IOR	–	–	–	operand location. Set next phase.
									Continued from 0247:
0140	75377461	RRRA	–	S2	IOR	–	CNTR	RPT	Put shift count into counter and set repeat mode.
0141	17676450		B	–	CRS	B	R1	CTR1	Rotate B- and A-registers right until counter = 17B. Increment counter each shift. Exits with counter = 20B.
0142	77777775		–	–	IOR	–	–	EOP	Set next phase.
0143	77777777		–	–	IOR	–	–	–	NOP.
0144	75770757	ADD	–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0145	53773375		AAB	COND	IOR	S2	–	EOP	Put operand data into S2. Set next phase.
0146	45125777		CAB	S2	ADDO	CAB	–	–	Add A/B-register data (per IR11) to operand in S2, store result in A/B-register (per IR11). Enable Overflow.
0150	35460712	JSB	F	S1	DEC	M	CW	NMPV	Test jump address. If no violation is detected, start memory clear/write cycle and skip next line.
0151	77346373		–	P	SFLG	AAB	–	AAB	If AAF/BAF is set, store P-register into A/B-register and skip next line. Set CPU Flag FF.
0152	77371366		–	P	IOR	T	–	FLG	Store P-register into T-register. Skip next line if CPUFlag set.
0153	75514375		–	S1	INC	P	–	EOP	Increment jump address and store in P-register. Set next phase.
0154	77777777		–	–	IOR	–	–	–	
									Continued from 0213:
0155	77756461	MPY	–	–	CLO	B	CNTR	RPT	Clear counter, B-register, and Overflow. Set repeat mode.
0156	15036450		B	S2	MPY	B	R1	CTRI	Execute MPY on B and S2 16 times. Result in B, A-registers.
0157	14377403		–	S4	IOR	–	RSS	NEG	Skip next line if multiplicand (was A-register) is positive.
0160	15056777		B	S2	SUB	B	–	–	Subtract multiplier from high order word of result.
0161	75377403		–	S2	IOR	–	RSS	NEG	Skip next line if multiplier (from memory) is positive.
0162	14056775		B	S4	SUB	B	–	EOP	Subtract multiplicand from high word. Set next phase.
0163	77114377		–	P	INC	P	–	–	Increment P-register past the DEF software instruction.

Table 4-9. ROM Program Listing (Continued)

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0164	75770757	LD*	–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0165	53773375		AAB	COND	IOR	S2	–	EOP	Put operand data into S2. Set next phase.
0166	75375777		–	S2	IOR	CAB	–	–	Put S2 contents into A/B-register, depending on IR11.
0170	75770757	ISZ	–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0171	57513373		AAB	–	INC	S2	–	AAB	Increment A- or B-register (per AAF/BAF) and save in S2. Skip next line if AAF/BAF is set.
0172	71113376		–	T	INC	S2	–	UNC	Increment T-register contents, save in S2. Skip next line.
0173	75377616		–	S2	IOR	–	ECYZ	UNC	Set Carry if S2 content is 0. Skip next line.
0174	35460712		F	S1	DEC	M	CW	NMPV	Test operand address. If no violation is detected, start memory clear/write cycle and skip next line.
0175	75376376		–	S2	IOR	AAB	–	UNC	Put S2 contents into A/B (per AAF/BAF). Skip next line.
0176	75371215		–	S2	IOR	T	ECYZ	EOP	Put S2 contents into T-register. Set carry if S2 content is 0.
0177	77777777		–	–	IOR	–	–	–	Set next phase.
0200	77777775		–	–	IOR	–	–	EOP	Unused.
0201	77777577	ASL	–	–	IOR	–	LEP	–	Legal entry point for ASL. Execute next line.
0202	37222622	LSL	F	–	JMP	S3	ASLA	–	Save Fence register in S3, jump to 0222.
0203	77777577		–	–	IOR	–	LEP	–	Legal entry point for LSL. Execute next line.
0204	37222742	RRL	F	–	JMP	S3	LSLA	–	Save Fence register in S3, jump to 0342.
0205	77777577		–	–	IOR	–	LEP	–	Legal entry point for RRL. Execute next line.
0206	37222752		F	–	JMP	S3	RRLA	–	Save Fence register in S3, jump to 0352.
0207	77777777		–	–	IOR	–	–	–	NOP.
0210	77777577	MULT	–	–	IOR	–	LEP	–	Legal entry point for MPY. Execute next line.
0211	77207762		–	–	JSB	–	GETAD	–	Execute GETAD subroutine. Puts multiplier address in S1.
0212	77207632		–	–	JSB	–	OPGET	–	Execute OPGET subroutine. Puts multiplier in S2.
0213	07222155		A	–	JMP	S4	MPY	–	Save multiplicand in S4. Jump to 0155.
0214	77777777		–	–	IOR	–	–	–	Unused.
0215	77777777		–	–	IOR	–	–	–	Unused.
0216	77777775		–	–	IOR	–	–	EOP	Unused.
0217	77777777		–	–	IOR	–	–	–	Unused.
0220	77777577	DIVID	–	–	IOR	–	LEP	–	Legal entry point for DIV. Execute next line.
0221	77227651		–	–	JMP	–	DIV	–	Jump to 0251.
									Continued from 0202:
0222	73053377	ASLA	–	ADR	SUB	S2	–	–	Put 2's complement of shift count (IR0:3) into S2.
0223	17754777		B	–	CLO	F	–	–	Put B-register contents into F-register (high word). Clear OVF.
0224	07775377		A	–	IOR	Q	–	–	Put A-register contents into Q-register (low order word).
0225	75377461		–	S2	IOR	–	CNTR	RPT	Put shift count into counter and set repeat mode.
0226	37704430		F	–	ARS	F	L1	CTRI	Arithmetic left shift F, Q-registers until counter = 17B. Increment counter each shift. Set OVF if F15, F14 = 10 or 01 at any time. Exits with counter = 20B.
0227	27777377		Q	–	IOR	A	–	–	Replace low order word in A-register.
0230	37776775		F	–	IOR	B	–	EOP	Replace high order word in B-register. Set next phase.
0231	74774777		–	S3	IOR	F	–	–	Restore fence value to F-register.
0232	75770757	OPGET	–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0233	53773377		AAB	COND	IOR	S2	–	–	Put operand data into S2.
0234	77247411		–	–	CJMP	–	PDEC	–	Jump to 0011 if interrupt or panel halt. Else continue.
0235	77657777		–	–	RSB	–	–	–	Return to calling routine.
0236	77777777		–	–	IOR	–	–	–	Unused.
0237	77777775		–	–	IOR	–	–	EOP	Unused.
0240	77777777		–	–	IOR	–	–	–	Unused.
0241	77777577	ASR	–	–	IOR	–	LEP	–	Legal entry point for ASR. Execute next line.
0242	77227732	LSR	–	–	JMP	–	ASRA	–	Jump to 0332.
0243	77777577		–	–	IOR	–	LEP	–	Legal entry point for LSR. Execute next line.

Table 4-9. ROM Program Listing (Continued)

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0244	77227736	RRR	–	–	JMP	–	LSRA	–	Jump to 0336.
0245	77777577		–	–	IOR	–	LEP	–	Legal entry point for RRR. Execute next line.
0246	73053377		–	ADR	SUB	S2	–	–	Put 2's complement of shift count (IR0:3) into S2.
0247	77227540		–	–	JMP	–	RRRA	–	Jump to 0140.
0250	77777777		–	–	IOR	–	–	–	Unused.
									Continued from 0221:
0251	77207762	DIV	–	–	JSB	–	GETAD	–	Execute GETAD subroutine. Puts divisor address in S1.
0252	37202232		F	–	JSB	S4	OPGET	–	Execute OPGET subroutine. Puts divisor in S2.
0253	17764763		B	–	SOV	F	–	NEG	Put high order word of dividend in F-register. Set Overflow and skip next line if dividend is negative.
0254	07225262		A	–	JMP	Q	DVS	–	Put low order word of dividend in Q-register, jump to 0262.
0255	07773777		A	–	IOR	S1	–	–	Dividend is negative. Two's
0256	17772777		B	–	IOR	S3	–	–	complement it to make
0257	75455364		–	S1	SUB	Q	–	COUT	it positive, and put it
0260	74554776		–	S3	NOR	F	–	UNC	into the F- and Q-
0261	74454777		–	S3	SUB	F	–	–	registers.
0262	75373403	DVS	–	S2	IOR	S1	RSS	NEG	Save original divisor in S1. Skip next line if positive.
0263	75453377		–	S1	SUB	S2	–	–	Convert negative divisor to positive.
0264	35057763		F	S2	SUB	–	–	NEG	First overflow check. If dividend high word ⩾ divisor, set Overflow and exit with dividend unaltered.
0265	37226702		F	–	JMP	B	DONE	–	Exit: put dividend high word back in B-register, jump to 0302.
0266	37664437		F	–	LGS	F	L1	–	Logical left shift the dividend (F, Q-registers) one place.
0267	77752461		–	–	CLO	S3	CNTR	RPT	Clear OVF, S3 register, and counter. Set repeat mode.
0270	35044430		F	S2	DIV	F	L1	CTRI	Execute DIV on F-register and S2 16 times. Positive quotient is left in Q-register, and 2X remainder in F-register.
0271	27773367		Q	–	IOR	S2	–	TBZ	Save quotient in S2 for negation test. Skip next line if contents of Q-register = 0.
0272	15562403		B	S1	XOR	S3	RSS	NEG	Compare signs of dividend and divisor, save result in S3. Skip next line if signs are alike.
0273	75055377		–	S2	SUB	Q	–	–	2's complement quotient and put back in Q-register.
0274	24567403		Q	S3	XOR	–	RSS	NEG	Compare quotient sign with expected sign. Skip next line if the same. This tests for most negative integer = 100. . .00.
0275	77767777		–	–	SOV	–	–	–	Set OVF.
0276	37773057		F	–	IOR	S2	R1	–	Divide remainder by 2 (shift right) and save in S2.
0277	17777403		B	–	IOR	–	RSS	NEG	Skip next line if dividend is positive.
0300	75056776		–	S2	SUB	B	–	UNC	2's complement remainder and put in B-register. Skip next line.
0301	75376777		–	S2	IOR	B	–	–	Put remainder in B-register.
0302	27777377	DONE	Q	–	IOR	A	–	–	Put quotient into A-register (or dividend low order word if entered from 0265).
0303	74374775		–	S4	IOR	F	–	EOP	Restore fence value to F-register. Set next phase.
0304	77114377		–	P	INC	P	–	–	Increment P-register past the software DEF instruction.
0310	77777577	DLD	–	–	IOR	–	LEP	–	Legal entry point for DLD.
0311	77207762		–	–	JSB	–	GETAD	–	Use GETAD subroutine (0362) to fetch address of first word.
0312	75513377		–	S1	INC	S2	–	–	Increment first word address, and put in S2.
0313	75770757		–	S1	IOR	M	RW	–	Send first word address to memory and start read cycle.
0314	53777377		AAB	COND	IOR	A	–	–	Put first operand in A-register.
0315	75370757		–	S2	IOR	M	RW	–	Send 2nd word address to memory and start read cycle.
0316	53776775		AAB	COND	IOR	B	–	EOP	Put second operand in B-register. Set next phase.
0317	77114377		–	P	INC	P	–	–	Increment P-register past the software DEF instruction.
0320	77777577	DST	–	–	IOR	–	LEP	–	Legal entry point for DST.
0321	77207762		–	–	JSB	–	GETAD	–	Use GETAD subroutine (0362) to fetch address of first word.
0322	35460712		F	S1	DEC	M	CW	NMPV	Test 1st address for memory protect violation. If none, send it to memory (S1 stored in M regardless), start a clear/write cycle, and skip next line.
0323	02376376		A	RRS	IOR	AAB	–	UNC	Put 1st word in A/B-register if AAF/BAF set. Skip next line.
0324	02371377		A	RRS	IOR	T	–	–	Send 1st word to memory (T-register) for storing.
0325	75512557		–	S1	INC	S3	AAB	–	Increment 1st word address, put in S3. Set AAF/BAF if 0 or 1.
0326	34460712		F	S3	DEC	M	CW	NMPV	Test 2nd address for memory protect violation. If none, send it to memory (S3 stored in M regardless), start clear/write cycle, and skip next line.

Table 4-9. ROM Program Listing (Continued)

ROM Adrs	ROM Word (octal)	Entry Point Label	Field Contents						Comments
			R	S	FN	ST	SP	SK	
0327	12376376		B	RRS	IOR	AAB	–	UNC	Put 2nd word in A/B-register if AAF/BAF set. Skip next line.
0330	12371375		B	RRS	IOR	T	–	EOP	Send 2nd word to memory for storing. Set next phase.
0331	77114377		–	P	INC	P	–	–	Increment P-register past the software DEF instruction.
									Continued from 0242:
0332	73053377	ASRA	–	ADR	SUB	S2	–	–	Put 2's complement of shift count (IR0:3) into S2.
0333	75357461		–	S2	CLO	–	CNTR	RPT	Put shift count into counter, set repeat mode, clear OVF.
0334	17706450		B	–	ARS	B	R1	CTRI	Arithmetic right shift B, A-registers until counter = 17B. Increment counter each shift. Exits with counter = 20B.
0335	77777775		–	–	IOR	–	–	EOP	Set next phase.
									Continued from 0244:
0336	73053377	LSRA	–	ADR	SUB	S2	–	–	Put 2's complement of shift count (IR0:3) into S2.
0337	75377461		–	S2	IOR	–	CNTR	RPT	Put shift count into counter and set repeat mode.
0340	17666450		B	–	LGS	B	R1	CTRI	Logical right shift B, A-registers until counter = 17B. Increment counter each shift. Exits with counter = 20B.
0341	77777775		–	–	IOR	–	–	EOP	Set next phase.
									Continued from 0204:
0342	73053377	LSLA	–	ADR	SUB	S2	–	–	Put 2's complement of shift count (IR0:3) into S2.
0343	17774777		B	–	IOR	F	–	–	Put high order word into F-register.
0344	07775377		A	–	IOR	Q	–	–	Put low order word into Q-register.
0345	75377461		–	S2	IOR	–	CNTR	RPT	Put shift count into counter and set repeat mode.
0346	37664430		F	–	LGS	F	L1	CTRI	Logical left shift F, Q-registers until counter = 17B. Increment counter each shift. Exits with counter = 20B.
0347	37776777		F	–	IOR	B	–	–	Put high order word into B-register.
0350	27777375		Q	–	IOR	A	–	EOP	Put low order word into A-register. Set next phase.
0351	74774777		–	S3	IOR	F	–	–	Restore fence value to F-register.
									Continued from 0206:
0352	73053377	RRLA	–	ADR	SUB	S2	–	–	Put 2's complement of shift count (IR0:3) into S2.
0353	17774777		B	–	IOR	F	–	–	Put high order word into F-register.
0354	07775377		A	–	IOR	Q	–	–	Put low order word into Q-register.
0355	75377461		–	S2	IOR	–	CNTR	RPT	Put shift count into counter and set repeat mode.
0356	37674430		F	–	CRS	F	L1	CTRI	Rotate F, Q-registers left until counter = 17B. Increment counter each shift. Exits with counter = 20B.
0357	37776777		F	–	IOR	B	–	–	Put high order word into B-register.
0360	27777375		Q	–	IOR	A	–	EOP	Put low order word into A-register. Set next phase.
0361	74774777		–	S3	IOR	F	–	–	Restore fence value to F-register.
0362	77370757	GETAD	–	P	IOR	M	RW	–	Send P-register address to memory, start read cycle. Normally fetches contents of a software DEF instruction.
0363	53773403	ONEMO	AAB	COND	IOR	S1	RSS	NEG	Put fetched word into S1. Skip next line if not indirect (i.e., if bit 15 = 0).
0364	77227766		–	–	JMP	–	IND	–	Jump to 0366.
0365	75657557		–	S1	RSB	–	AAB	–	Set AAF/BAF if S1 contents = 0 or 1. Return to calling subroutine.
0366	77247411	IND	–	–	CJMP	–	PDEC	–	Jump to 0011 if interrupt or panel halt. Else continue.
0367	75770757		–	S1	IOR	M	RW	–	Send operand address to memory and start read cycle.
0370	77227763		–	–	JMP	–	ONEMO	–	Jump to 0363.
0371	77777777		–	–	IOR	–	–	–	Unused.
0372	77777777		–	–	IOR	–	–	–	Unused.
0373	77777775		–	–	IOR	–	–	EOP	Unused.
0374	77777777		–	–	IOR	–	–	–	Unused.
0375	77777777		–	–	IOR	–	–	–	Unused.
0376	77777775		–	–	IOR	–	–	EOP	Unused.
0377	77777777		–	–	IOR	–	–	–	Unused.

4-36. ROM MICROPROGRAM SERVICING DATA.

4-37. The following pages provide detailed central processor servicing information for all ROM microprogram-controlled phases of computer operation. The ROM microprogram servicing data is organized as shown by the following index.

Note: The asterisk (*) is used in the user instruction codes to indicate the choice of selecting either the A-register or B-register.

4-38. All ROM microinstructions are represented in this portion of the manual as shown in figure 4-4.

4-39. In this example, the ROM microinstruction is the first to be executed during the execute phase of the CP* (CPA or CPB) user instruction. The ROM address of this microinstruction is 114 octal. The 24-bit microinstruction word is represented in octal and binary form with the binary notation grouped according to the fields of the microinstruction. The condition statement implies that unless the stated condition (T6 in this case) is true, the microinstruction will not be executed and the central processor will "freeze". The freeze operation lasts until the condition is true then the microinstruction is executed. If the condition statement is "none", the microinstruction will be executed unconditionally immediately following the previous microinstruction.

4-40. The remainder of the example lists each microinstruction field code, the relevant signals resulting from that code, the logic levels of these signals, backplane source and destination information, and brief comments describing the effect of the signals. For some microinstructions, the comments make reference to another page. This is where further information supporting that operation can be found. This occurs under the following conditions.

a. EOP in the skip field. Refers to page 4-30 which describes the set phase logic enabled by the EOP.

b. JMP or JSB in the function field. The special field of a microinstruction having a JMP or JSB code in the function field provides the label of the jump-to location or the subroutine location in the microprogram. The comments portion of the special field provides the page number in this section where that portion of the microprogram is documented.

c. Special field enables a decoder (hardware). Certain I/O group, shift-rotate, and alter-skip group instructions are decoded by decoders. When the special field of a microinstruction enables one of these decoders, the page number is given in the comments where that decoder is documented.

CP*,EXECUTE PHASE

ROM ADDRESS: 114
ROM MICROINSTRUCTION: 75770754 111 1011 11111 0001 1110 1100
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NAAB	IF AAB	0	A5-26	A6-78	T-BUS(1-15) NOT 0
	---		A6(INTERNAL)		ENABLE SKIP FF
	IF AAB	1	A5-26	A6-78	T-BUS(1-15) IS 0
	---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

Figure 4-4. Example of ROM Microinstruction Servicing Data

4-41. SET PHASE LOGIC. During execution of the second-to-last microinstruction of every phase of operation (except DMA) an EOP (End of Phase) code is decoded in the skip field of that microinstruction. This EOP is decoded even when the previous microinstruction enables a ROM skip. The EOP code enables the set phase logic to determine the next phase of operation.

4-42. Figure 4-5 consists of four flowcharts which describe the operation of the set phase logic when an EOP is decoded. Use the flowchart corresponding to the present phase of operation to determine the phase that will be entered next.

4-43. PHASE 1A. Phase 1A (PH1A) is the normal computer fetch phase for any user instruction. Phase 1A directs the central processor to ROM address 000 and executes the microinstructions at ROM addresses 000, 001, and 002. Execution of these microinstructions results in the following:

a. ROM address 000. Transfers the P-register content to the M-register, starts a memory read-write cycle, and checks for A-register or B-register addressing.

b. ROM address 001. Transfers the A- or B- or T-register content to the I-register and sets the phase logic to the next phase. If the instruction word is not a memory reference group instruction, the next microinstruction (ROM address 002) is skipped.

c. ROM address 002. Transfers the full operand address (part of the I-register and part of the P-register) to the SP1-register and checks for A- or B-register addressing.

4-44. The following pages provide ROM decoding and signal information for the PH1A operation.

PH1A, ANY INSTRUCTION

ROM ADDRESS: 000 R S FUN STR SP SKIP
ROM MICROINSTRUCTION: 77330757 111 1110 11011 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
CFLG	---		A4 (INTERNAL)		CLEAR FLAG LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

PHIA•CONTINUED

ROM ADDRESS: 001
ROM MICROINSTRUCTION: 53771775 101 0111 11111 0011 1111 1101
CONDITION: DTRY(+4 time)

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
IR	STI	1	A3-44	A6-30	I = S-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

PH1A,CONTINUED

ROM ADDRESS: 002
ROM MICROINSTRUCTION: 73373557 111 0110 11111 0111 0110 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S1	WSP1	1	A3-55	A5-65	SP1 - T-BUS
SPECIAL					
AAB	IF AAB	1	A5-26	A6-78	T-BUS)1-14)=0
	AND ALU0	0	A5-58	A6-79	ALU(0)=0
	---		A6(INTERNAL)		SET AAFF LOGIC
	IF AAB	1	A5-26	A6-78	T-BUS(1-15)=0
	AND ALU0	1	A5-58	A6-79	ALU(0)=1
	---		A6(INTERNAL)		SET BAFF LOGIC
	IF AAB	0	A5-26	A6-78	T-BUS(1-14) NOT=0
	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

NOTE: IF THE FETCHED INSTRUCTION WORD IS NOT A MEMORY REFERENCE GROUP INSTRUCTION, THIS MICROINSTRUCTION IS SKIPPED.

4-45. PHASE 1B. Phase 1B (PH1B) is the fetch phase resulting from an I/O interrupt. Phase 1B directs the central processor to ROM address 004 and executes the microinstructions at ROM addresses 004, 005, 006, 007, and 010. Execution of these microinstructions results in the following:

a. ROM address 004. Transfers the central interrupt (CIR) register content to the M-register, starts a memory read-write cycle, and checks for A- or B-register addressing.

b. ROM address 005. Complements and increments the P-register content.

c. ROM address 006. Complements the P-register.

Note: The result of steps "b" and "c" is to decrement the P-register.

d. ROM address 007. Transfers the A- or B- or T-register content to the I-register and sets the phase logic to the next phase. If the fetched instruction word is not a memory reference group instruction, the next ROM microinstruction is skipped.

e. ROM address 010. Transfers the full operand address (part of the I-register and part of the P-register) to the SP1-register and checks for A- or B-register addressing.

4-46. The following pages provide ROM decoding and signal information for the PH1B operation.

PH1B•ANY INSTRUCTION

ROM ADDRESS: 004
ROM MICROINSTRUCTION: 70330757 111 0000 11011 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
CIR	RCIR	1	A3-23	A7-54	S-BUS = CIR
FUNCTION					
CFLG	---		A4 (INTERNAL)		CLEAR FLAG LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

PHIB•CONTINUED

ROM ADDRESS: 005
ROM MICROINSTRUCTION: 77054377 111 1110 00101 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPL0	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	$\overline{\text{FN3}}$	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

PH1B,CONTINUED

ROM ADDRESS: 006
ROM MICROINSTRUCTION: 77154377 111 1110 01101 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
NOR	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NEGATIVE OR
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

PH1B•CONTINUED

ROM ADDRESS: 007
ROM MICROINSTRUCTION: 53771775 101 0111 11111 0011 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
IR	STI	1	A3-44	A6-30	I = S-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

PH1B,CONTINUED

ROM ADDRESS: 010
ROM MICROINSTRUCTION: 73373557 111 0110 11111 0111 0110 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S1	WSP1	1	A3-55	A5-65	SP1 - T-BUS
SPECIAL					
AAB	IF AAB	1	A5-26	A6-78	T-BUS)1-14)=0
	AND ALU0	0	A5-58	A6-79	ALU(0)=0
	---		A6(INTERNAL)		SET AAFF LOGIC
	IF AAB	1	A5-26	A6-78	T-BUS(1-15)=0
	AND ALU0	1	A5-58	A6-79	ALU(0)=1
	---		A6(INTERNAL)		SET BAFF LOGIC
	IF AAB	0	A5-26	A6-78	T-BUS(1-14) NOT=0
	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

NOTE: IF THE FETCHED INSTRUCTION WORD IS NOT A MEMORY REFERENCE GROUP INSTRUCTION, THIS MICROINSTRUCTION IS SKIPPED.

4-47. PHASE 2. Phase 2 (PH2) is the computer indirect phase. Phase 2 directs the central processor to ROM address 014 and executes the microinstructions at ROM addresses 014, 015, and 016. Execution of these microinstructions results in the following:

a. ROM address 014. Transfers the SP1-register content (operand address) to the M-register, starts a memory read-write cycle, and checks for A- or B-register addressing.

b. ROM address 015. Transfers the A- or B- or T-register content to the SP1-register and sets the phase logic to the next phase.

c. ROM address 016. Checks the SP1-register content for A- or B-register addressing.

4-48. The following pages provide ROM decoding and signal information for the PH2 operation.

PH2, INDIRECT PHASE

ROM ADDRESS: 014
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

PH2•CONTINUED

ROM ADDRESS: 015
ROM MICROINSTRUCTION: 53773775 101 0111 11111 0111 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S1	WSP1	1	A3-55	A5-65	SP1 - T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

PH2•CONTINUED

ROM ADDRESS: 016
ROM MICROINSTRUCTION: 75777557 111 1011 11111 1111 0110 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
AAB	IF AAB	1	A5-26	A6-78	T-BUS)1-14)=0
	AND ALU0	0	A5-58	A6-79	ALU(0)=0
	---		A6(INTERNAL)		SET AAFF LOGIC
	IF AAB	1	A5-26	A6-78	T-BUS(1-15)=0
	AND ALU0	1	A5-58	A6-79	ALU(0)=1
	---		A6(INTERNAL)		SET BAFF LOGIC
	IF AAR	0	A5-26	A6-78	T-BUS(1-14) NOT=0
	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

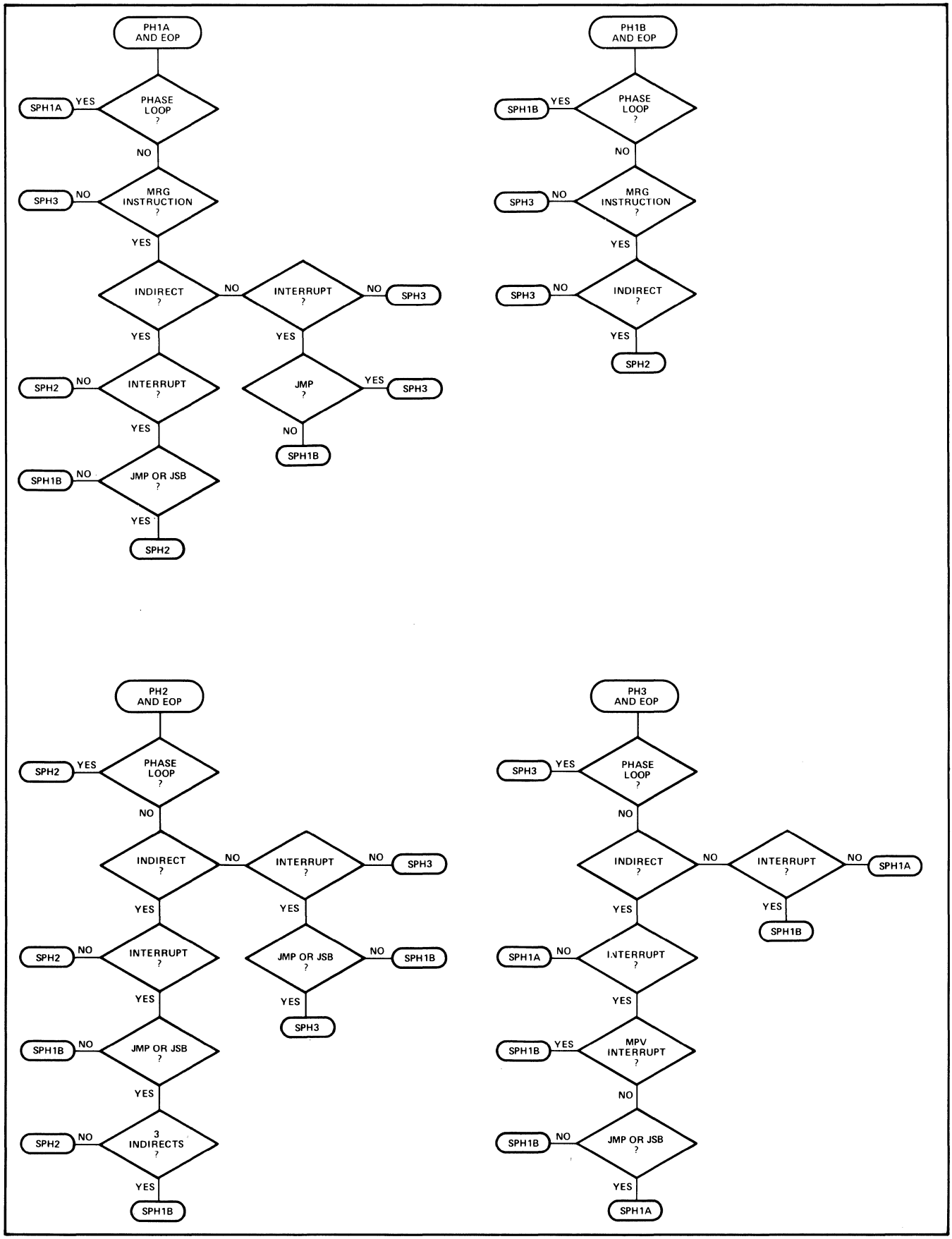


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Figure 4-5. Set Phase Logic, Flowcharts

4-49. PHASE 3. Phase 3 (PH3) is the execute phase for a user instruction. Each user instruction directs the central processor to a unique set of ROM microinstructions for the execute phase of that instruction. The following pages provide ROM service information for the execute phase of each 2100A Computer user instruction.

Note: The P-register is automatically incremented upon entering Phase 3.

4-50. MEMORY REFERENCE GROUP. Each memory reference instruction directs the central processor to a set of ROM microinstructions that is unique to that instruction. It must be understood that to perform the execute phase of an instruction, it must have been previously fetched by a PH1A or PH1B operation. The fetch operation leaves the central processor with the fetched instruction word in the I-register, the full operand address of the instruction in the SP1-register, and the A- or B-addressable logic set if the operand address is 000000 (A-register) or 000001 (B-register). The following pages detail the central processor operation for the execute phase of all user memory reference instructions.

4-51. AND Instruction. The AND instruction execute phase directs the central processor to ROM address 110 and executes the microinstructions at ROM addresses 110, 111, and 112. Execution of these microinstructions results in the following:

a. ROM address 110. Stores the SP1-register content (operand address) in the M-register, starts a memory read-write cycle, and checks for A- or B-register addressing.

b. ROM address 111. Stores the A- or B- or T-register content in the SP2-register and sets phase logic for the next phase.

c. ROM address 112. Logically ANDs the A-register content with the SP2-register content and stores the result in the A-register.

4-52. The following pages provide ROM decoding and signal information for the execute phase of the AND instruction.

AND•EXECUTE PHASE

ROM ADDRESS: 110
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

AND, CONTINUED

ROM ADDRESS: 111
ROM MICROINSTRUCTION: 51773375 101 0011 11111 0110 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

AND•CONTINUED

ROM ADDRESS: 112
ROM MICROINSTRUCTION: 05147377 000 1010 01100 1110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
AND	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	1	A4-3	A5-46	LOGICAL AND
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-53. XOR Instruction. The XOR instruction execute phase directs the central processor to ROM address 120 and executes the microinstructions at ROM addresses 120, 121, and 122. Execution of these microinstructions results in the following:

a. ROM address 120. Stores the SP1-register content in the M-register, starts a memory read-write cycle, and checks for A- or B-register addressing.

b. ROM address 121. Stores the A- or B- or T-register content in the SP2-register and sets phase logic for the next phase.

c. ROM address 122. Logically exclusive ORs the A-register content with the SP2-register content and stores the result in the A-register.

XOR•EXECUTE PHASE

ROM ADDRESS: 120
ROM MICROINSTRUCTION: 75770757 000 1010 01110 1110 1111 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

XOR•CONTINUED

ROM ADDRESS: 121
ROM MICROINSTRUCTION: 53773375 101 0111 11111 0110 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE
					(PAGE 4-30)

XOR, CONTINUED

ROM ADDRESS: 122
ROM MICROINSTRUCTION: 05167377 000 1010 01110 1110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
XOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	EXCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-54. IOR Instruction. The IOR instruction execute phase directs the central processor to ROM address 130 and executes the microinstructions at ROM addresses 130, 131, and 132. Execution of these microinstructions results in the following:

a. ROM address 130. Stores the SP1-register content in the M-register, starts a read-write cycle, and checks for A- or B-register addressing.

b. ROM address 131. Stores the A- or B- or T-register content in the SP2-register and sets phase logic for the next phase.

c. ROM address 132. Logically inclusive ORs the A-register content with the SP2-register content and stores the result in the A-register.

IOR, EXECUTE PHASE

ROM ADDRESS: 130
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

IOR•CONTINUED

ROM ADDRESS: 131
ROM MICROINSTRUCTION: 53773375 101 0111 11111 0110 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

IOR, CONTINUED

ROM ADDRESS: 132
ROM MICROINSTRUCTION: 05377377 000 1010 11111 1110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-55. JSB Instruction. The JSB instruction execute phase directs the central processor to ROM address 150 and executes the microinstructions at ROM addresses 150, 151, 152, 153, and 154. Execution of these microinstructions results in the following:

a. ROM address 150. Stores the SP1-register content (operand address) in the M-register, starts a memory clear-write cycle, and checks for a possible memory protect violation by doing a "1's" complement subtract of the SP1-register content (operand address) from the F-register content (fence) and checking for a positive (violation exists) or negative (no violation) result. If there is no violation and the operand address is not the A- or B-register, the next microinstruction (ROM address 151) is skipped.

b. ROM address 151. Sets the central processor FLAG FF. If the operand address is the A- or B-register, the P-register content is stored in that (A- or B-) register and the next microinstruction (ROM address 152) is skipped. If not, no store or skip takes place.

c. ROM address 152. Stores the P-register content in the T-register. Timing is such that this is written into memory as a result of the clear-write operation started during execution of ROM address 150. If the central processor FLAG FF is set, the next microinstruction (ROM address 153) is skipped.

d. ROM address 153. Increments the content of the SP1-register and stores the result in the P-register. Sets the phase logic to the next phase.

e. ROM address 154. No significant operation.

JSB, EXECUTE PHASE

ROM ADDRESS: 150
ROM MICROINSTRUCTION: 35460712 011 1011 00110 0001 1100 1010
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
DEC	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	1'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
CW	CW	1	A6-73	A107-76	CLEAR-WRITE MEMORY
SKIP					
NMPV	IF MPC	0	A8-80	A6-13	MEMORY PROTECT DISABLED
	OR $\overline{\text{ALU 15}}$	1	A5-21	A6-77	NO MP VIOLATION
	AND $\overline{\text{AAFF}}$	1	A6-5	A6-5	A ADDRESSABLE FF CLEAR
	AND BAFF	0	A6-7	A6-7	B ADDRESSABLE FF CLEAR
	---	A6(INTERNAL)			ENABLE SKIP FF
	ELSE ---				NO OPERATION

REVERSE IF RSS IN SPECIAL FIELD

JSB,CONTINUED

ROM ADDRESS: 151
ROM MICROINSTRUCTION: 77346373 111 1110 11100 1100 1111 1011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
SFLG	---		A4(INTERNAL)		SET FLAG LOGIC
	MC	1	A4-20	A5-12	
	FN3	1	A4-5	A5-55	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
AAB	IF $\overline{\text{AAFF}}$	0	A6-5	A3-52	A IS ADDRESSED
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF BAFF	1	A6-7	A3-43	B IS ADDRESSED
	STB	1	A3-63	A5-79	B = T-BUS
	IF $\overline{\text{AAFF}}$	1	A6-5	A3-52	A NOT ADDRESSED
	AND BAFF	0	A6-7	A3-43	B NOT ADDRESSED
	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
AAB	IF $\overline{\text{AAF}}$	0	A6-5	A6-5	A ADDRESS LOGIC SET
	OR BAF	1	A6-7	A6-7	B ADDRESS LOGIC SET
	---		A6(INTERNAL)		ENABLE SKIP FF
	IF $\overline{\text{AAFF}}$	1	A6-5	A6-5	A ADDRESS LOGIC CLEAR
	AND $\overline{\text{BAFF}}$	0	A6-7	A6-7	B ADDRESS LOGIC CLEAR
	---				NO OPERATION

REVERSE IF RSS IN SPECIAL FIELD

JSB,CONTINUED

ROM ADDRESS: 152
ROM MICROINSTRUCTION: 77371366 111 1110 11111 0010 1111 0110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPL0	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
T	SELT	1	A3-30	A107-74	T = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
NOP	---				NO OPERATION
SKIP					
FLG	IF FLG	1	A4-23	A6-80	FLAG FF SET
	---	A6(INTERNAL)			ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

JSB•CONTINUED

ROM ADDRESS: 153
ROM MICROINSTRUCTION: 75514375 111 1011 01001 1000 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
INC	MC	Ø	A4-20	A5-12	
	FNØ	1	A4-66	A5-50	
	FN1	Ø	A4-3	A5-46	ARITHMETIC ADD
	FN2	Ø	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	Ø	A4-14	A5-41	CARRY IN TO ALU
STORE					
P	$\overline{\text{STP}}$	Ø	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

JSB,CONTINUED

ROM ADDRESS: 154
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-56. JMP Instruction. The JMP instruction execute phase directs the central processor to ROM address 124 and executes the microinstructions at ROM addresses 124, 125, 126, and 127. Execution of these microinstructions results in the following:

a. ROM address 124. Clears the A- and B-register addressable logic by logically negative ORing the R- and S-buses (all "0's" due to NOPs in both fields) and testing for A- or B-register addressing.

b. ROM address 125. Checks for a possible memory protect violation by doing a "1's" complement subtract of the SP1-register (operand address) from the F-register (fence) and checking for a positive (violation exists) or negative (no violation) result. If there is a violation, the next microinstruction (ROM address 126) is skipped.

c. ROM address 126. Stores the SP1-register content (operand address) in the P-register and sets the phase logic to the next phase.

d. ROM address 127. No significant operation.

JMP, EXECUTE PHASE

ROM ADDRESS: 124
ROM MICROINSTRUCTION: 77557557 111 1111 01101 1111 0110 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
NOR	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NEGATIVE OR
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
AAB	IF AAB	1	A5-26	A6-78	T-BUS)1-14)=0
	AND ALU0	0	A5-58	A6-79	ALU(0)=0
	---		A6(INTERNAL)		SET AAFF LOGIC
	IF AAB	1	A5-26	A6-78	T-BUS(1-15)=0
	AND ALU0	1	A5-58	A6-79	ALU(0)=1
	---		A6(INTERNAL)		SET BAFF LOGIC
	IF AAB	0	A5-26	A6-78	T-BUS(1-14) NOT=0
	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

JMP,CONTINUED

ROM ADDRESS: 125
ROM MICROINSTRUCTION: 35467412 011 1011 00110 1111 0000 1010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
DEC	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	1'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NMPV	IF MPC	0	A8-80	A6-13	MEMORY PROTECT DISABLED
	OR $\overline{ALU\ 15}$	1	A5-21	A6-77	NO MP VIOLATION
	AND $\overline{AAFF}$	1	A6-5	A6-5	A ADDRESSABLE FF CLEAR
	AND BAFF	0	A6-7	A6-7	B ADDRESSABLE FF CLEAR
	---	A6(INTERNAL)			ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

JMP, CONTINUED

ROM ADDRESS: 126
ROM MICROINSTRUCTION: 75774375 111 1011 11111 1000 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

JMP,CONTINUED

ROM ADDRESS: 127
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-57. ISZ Instruction. The ISZ instruction execute phase directs the central processor to ROM address 170 and executes the microinstructions at ROM addresses 170 through 177. Execution of these microinstructions results in the following:

a. ROM address 170. Stores the SP1-register content (operand address) in the M-register and starts a memory read-write cycle.

b. ROM address 171. If the operand address is the A- or B-register, increments the contents of that register (A or B), stores the result in the SP2-register and skips the next microinstruction (ROM address 172). If the operand address is not the A- or B-register, no significant operation occurs.

c. ROM address 172. Increments the T-register content (memory data found at the operand address) and stores the result in the SP2-register. Unconditionally skips the next microinstruction (ROM address 173).

d. ROM address 173. Checks the SP2-register content (resulting from execution of ROM address 171) for all "0's" and if all "0's", sets the increment P-register logic. If not all "0's", no operation. Unconditionally skips the next microinstruction (ROM address 174).

e. ROM address 174. Stores the SP1-register content (operand address) in the M-register, starts a memory clear-write cycle, and checks for a possible memory protect violation by doing a "1's" complement subtract of the SP1-register content (operand address) from the F-register content (fence) and checking for a positive (violation exists) or negative (no violation) result. If there is no violation, the next microinstruction (ROM address 175) is skipped.

f. ROM address 175. If the operand address is the A- or B-register, stores the SP2-register content (resulting from execution of ROM address 171) in the addressed register (A or B). If the A- or B-register is not addressed, no operation. Unconditionally skips the next microinstruction (ROM address 176).

g. ROM address 176. Stores the SP2-register content (resulting from execution of ROM address 172) in the T-register. Timing is such that this is written into memory as a result of the clear-write operation started during execution of ROM address 174. If the SP2-register content is all "0's", sets the increment P-register logic. Sets the phase logic to the next phase.

h. ROM address 177. No significant operation.

ISZ, EXECUTE PHASE

ROM ADDRESS: 170
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

ISZ, CONTINUED

ROM ADDRESS: 171
ROM MICROINSTRUCTION: 77513373 111 1111 01001 0110 1111 1011
CONDITION: NONE

FIELD	SIGNALS		LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS						
AAB	IF	$\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND	COND	1	A3-20	A4-11	S-BUS DECODED COND
		$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF	$\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND	COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
		$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
		RBS1	0	A4-15	A5-64	R-BUS = A
	IF	$\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
		$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
		RBS1	0	A4-15	A5-64	R-BUS = A
	OR	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS						
NOP	---					NO OPERATION
FUNCTION						
INC	MC		0	A4-20	A5-12	
	FN0		1	A4-66	A5-50	
	FN1		0	A4-3	A5-46	ARITHMETIC ADD
	FN2		0	A4-4	A5-56	
	FN3		1	A4-5	A5-55	
	$\overline{CIN}$		0	A4-14	A5-41	CARRY IN TO ALU
STORE						
S2	WSP2		1	A3-56	A5-67	SP2 = T-BUS
SPECIAL						
NOP	---					NO OPERATION
SKIP						
AAB	IF	$\overline{AAF}$	0	A6-5	A6-5	A ADDRESS LOGIC SET
	OR	BAF	1	A6-7	A6-7	B ADDRESS LOGIC SET
		---	A6(INTERNAL)			ENABLE SKIP FF
	IF	$\overline{AAFF}$	1	A6-5	A6-5	A ADDRESS LOGIC CLEAR
	AND	$\overline{BAFF}$	0	A6-7	A6-7	B ADDRESS LOGIC CLEAR
		---				NO OPERATION

REVERSE IF RSS IN SPECIAL FIELD

ISZ,CONTINUED

ROM ADDRESS: 172
ROM MICROINSTRUCTION: 71113376 111 0010 01001 0110 1111 1110
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
T	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
FUNCTION					
INC	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	CARRY IN TO ALU
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---		A6(INTERNAL)		ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

ISZ•CONTINUED

ROM ADDRESS: 173
ROM MICROINSTRUCTION: 75377616 111 1010 11111 1111 1000 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
ECYZ	IF TBZ	1	A5-25	A6-19	T-BUS IS ALL 0'S
	SCRY	1	A6-28	A1-44	SET P CARRY LOGIC
	IF TBZ	0	A5-25	A6-19	T-BUS NOT ALL 0'S
	SCRY	0	A6-28	A1-44	NO OPERATION
SKIP					
UNC	---	A6(INTERNAL)			ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

ISZ, CONTINUED

ROM ADDRESS: 174
ROM MICROINSTRUCTION: 35460712 011 1011 00110 0001 1100 1010
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
DEC	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	1'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
CW	CW	1	A6-73	A107-76	CLEAR-WRITE MEMORY
SKIP					
NMPV	IF MPC	0	A8-80	A6-13	MEMORY PROTECT DISABLED
	OR $\overline{\text{ALU 15}}$	1	A5-21	A6-77	NO MP VIOLATION
	AND $\overline{\text{AAFF}}$	1	A6-5	A6-5	A ADDRESSABLE FF CLEAR
	AND BAFF	0	A6-7	A6-7	B ADDRESSABLE FF CLEAR
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

ISZ, CONTINUED

ROM ADDRESS: 175
ROM MICROINSTRUCTION: 75376376 111 1010 11111 1100 1111 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
AAB	IF $\overline{\text{AAFF}}$	0	A6-5	A3-52	A IS ADDRESSED
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF BAFF	1	A6-7	A3-43	B IS ADDRESSED
	STB	1	A3-63	A5-79	B = T-BUS
	IF $\overline{\text{AAFF}}$	1	A6-5	A3-52	A NOT ADDRESSED
	AND BAFF	0	A6-7	A3-43	B NOT ADDRESSED
	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---		A6(INTERNAL)		ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

ISZ, CONTINUED

ROM ADDRESS: 176
ROM MICROINSTRUCTION: 75371215 111 1010 11111 0010 1000 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
T	SELT	1	A3-30	A107-74	T = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
ECYZ	IF TBZ	1	A5-25	A6-19	T-BUS IS ALL 0'S
	SCRY	1	A6-28	A1-44	SET P CARRY LOGIC
	IF TBZ	0	A5-25	A6-19	T-BUS NOT ALL 0'S
	SCRY	0	A6-28	A1-44	NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ISZ, CONTINUED

ROM ADDRESS: 177
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-58. AD* Instruction. The AD* instruction execute phase directs the central processor to ROM address 144 and executes the microinstructions at ROM addresses 144, 145, and 146. Execution of these microinstructions results in the following:

a. ROM address 144. Stores the SP1-register content (operand address) in the M-register, starts a memory read-write cycle, and checks for A- or B-register addressing.

b. ROM address 145. Stores the A- or B- or T-register content in the SP2-register and sets the phase logic to the next phase.

c. ROM address 146. Arithmetically adds the selected register (A or B) content with the SP2-register content and stores the result in the selected register (A or B). (The selected register is determined by bit 11 of the AD* instruction word.)

AD*, EXECUTE PHASE

ROM ADDRESS: 144
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: ~~NONE~~ T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

AD*•CONTINUED

ROM ADDRESS: 145
ROM MICROINSTRUCTION: 53773375 101 0111 11111 0110 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RBE	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

AD*,CONTINUED

ROM ADDRESS: 146
ROM MICROINSTRUCTION: 45125777 100 1010 01010 1011 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
ADDO	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	ENOV	1	A4-51	A6-83	ENABLE OVERFLOW LOGIC
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-59. CP* Instruction. The CP* instruction execute phase directs the central processor to ROM address 114 and consists of the microinstructions at ROM addresses 114 through 117, 017, and 020. If the operand address of the CP* instruction word is the A- or B-register, the microinstructions at ROM addresses 114, 115, 017, and 020 are executed in that order. If the operand address is not the A- or B-register, the microinstructions at ROM addresses 114, 116, and 117 are executed in that order. Execution of these microinstructions results in the following:

a. ROM address 114. Stores the SP1-register content (operand address) in the M-register, starts a memory read-write cycle, checks for A- or B-register addressing, and if the operand address is not the A- or B-register, skips the next microinstruction (ROM address 115).

b. ROM address 115. Stores the A- or B-register content in the SP2-register and initiates a ROM jump to ROM address 017.

c. ROM address 116. Logically exclusive OR's the content of the selected register (A or B as determined by bit 11 of the CP* instruction word) with the T-register content (resulting from the read-write operation started by ROM address 114), sets the increment P-register logic if the result is not all "0's," and sets the phase logic to the next phase.

d. ROM address 117. No significant operation.

e. ROM address 017. Logically exclusive OR's the content of the selected register (A or B as determined by bit 11 of the CP* instruction word) with the SP2-register content (resulting from execution of ROM address 115), sets the increment P-register logic if the result is not all "0's," and sets the phase logic to the next phase.

f. ROM address 018. No significant operation.

4-60. The following pages provide ROM decoding and signal information for the execute phase of the CP* instruction.

CP*, EXECUTE PHASE

ROM ADDRESS: 114
ROM MICROINSTRUCTION: 75770754 111 1011 11111 0001 1110 1100
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NAAB	IF AAB	0	A5-26	A6-78	T-BUS(1-15) NOT 0
	---	A6(INTERNAL)			ENABLE SKIP FF
	IF AAB	1	A5-26	A6-78	T-BUS(1-15) IS 0
	---				NO OPERATION

REVERSE IF RSS IN SPECIAL FIELD

CP*,CONTINUED

ROM ADDRESS: 115
ROM MICROINSTRUCTION: 57223017 101 1110 10010 0110 0000 1111
CONDITION: NONE

FIELD	SIGNALS		LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS						
AAB	IF	$\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND	COND	1	A3-20	A4-11	S-BUS DECODED COND
		$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF	$\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND	COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
		$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
		$\overline{RBS1}$	0	A4-15	A5-64	R-BUS = A
	IF	$\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
		$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
		RBS1	0	A4-15	A5-64	R-BUS = A
	OR	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS						
NOP	---					NO OPERATION
FUNCTION						
JMP	MC		1	A4-20	A5-12	
	FN0		0	A4-66	A5-50	
	FN1		1	A4-3	A5-46	INCLUSIVE OR
	FN2		1	A4-4	A5-56	
	FN3		1	A4-5	A5-55	
	$\overline{JMPS}$		0	A4-46	A1-73	ROM JUMP
	$\overline{SRAR}$		0	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP		1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{JMPF}$		0	A4-49	A3-36	JMP FUNCTION
	ENSS		0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE						
S2	WSP2		1	A3-56	A5-67	SP2 = T-BUS
SPECIAL						
XX	---					SET ROM ADDRESS 017 (PAGE 4-77)
SKIP						
NOP	---					NO OPERATION

CP*,CONTINUED

ROM ADDRESS: 116
ROM MICROINSTRUCTION: 41167635 100 0010 01110 1111 1001 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
T	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
FUNCTION					
XOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	EXCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
ECYN	IF TBZ	0	A5-25	A6-19	T-BUS NOT ALL 0'S
	SCRY	1	A6-28	A1-44	SET P CARRY LOGIC
	IF TBZ	1	A5-25	A6-19	T-BUS IS ALL 0'S
	SCRY	0	A6-28	A1-44	NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

CP*•CONTINUED

ROM ADDRESS: 117
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

XX•CP* CONTINUED

ROM ADDRESS: 017
ROM MICROINSTRUCTION: 45167637 100 1010 01110 1111 1001 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
XOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	EXCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
ECYN	IF TBZ	0	A5-25	A6-19	T-BUS NOT ALL 0'S
	SCRY	1	A6-28	A1-44	SET P CARRY LOGIC
	IF TBZ	1	A5-25	A6-19	T-BUS IS ALL 0'S
	SCRY	0	A6-28	A1-44	NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE
					(PAGE 4-30)

XX.CONTINUED

ROM ADDRESS: 020
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-61. LD* Instruction. The LD* instruction execute phase directs the central processor to ROM address 164 and executes the microinstructions at ROM addresses 164, 165, and 166. Execution of these microinstructions results in the following:

a. ROM address 164. Stores the content of the SP1-register (operand address) in the M-register, starts a memory read-write cycle, and checks for A- or B-register addressing.

b. ROM address 165. Stores the content of the A- or B- or T-register in the SP2-register and sets the phase logic to the next phase.

c. ROM address 166. Stores the content of the SP2-register in the selected register (determined by bit 11 of the LD* instruction word).

4-62. The following pages provide ROM decoding information for the execute phase of the LD* instruction.

LD*, EXECUTE PHASE

ROM ADDRESS: 164
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

LD*•CONTINUED

ROM ADDRESS: 165
ROM MICROINSTRUCTION: 53773375 101 0111 11111 0110 1111 1101
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

LD*,CONTINUED

ROM ADDRESS: 166
ROM MICROINSTRUCTION: 75375777 111 1010 11111 1011 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-~~64~~ 67	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-63. ST* Instruction. The ST* instruction execute phase directs the central processor to ROM address 134 and executes the microinstructions at ROM addresses 134 through 137. Execution of these microinstructions results in the following:

a. ROM address 134. Stores the content of the SP1-register (operand address) in the M-register, starts a memory clear-write cycle, and checks for a possible memory protect violation by doing a "1's" complement subtract of the SP1-register content (operand address) from the F-register content (fence) and checking for a positive (violation exists) or negative (no violation) result. If there is no violation and the operand address is not the A- or B-register, the next microinstruction (ROM address 135) is skipped.

b. ROM address 135. Stores the content of the selected register (A or B as determined by bit 11 of the ST* instruction word) in the A- or B-register (determined by the operand address of the ST* instruction word). Unconditionally skips the next microinstruction (ROM address 136).

c. ROM address 136. Stores the content of the selected register (A or B as determined by bit 11 of the ST* instruction word) in the T-register. Timing is such that this is written in memory as a result of the clear-write cycle started by ROM address 134. Sets the phase logic to the next phase.

d. ROM address 137. No significant operation.

ST*, EXECUTE PHASE

ROM ADDRESS: 134
ROM MICROINSTRUCTION: 35460712 011 1011 00110 0001 1100 1010
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
DEC	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	1'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
CW	CW	1	A6-73	A107-76	CLEAR-WRITE MEMORY
SKIP					
NMPV	IF MPC	0	A8-80	A6-13	MEMORY PROTECT DISABLED
	OR ALU 15	1	A5-21	A6-77	NO MP VIOLATION
	AND $\overline{\text{AAFF}}$	1	A6-5	A6-5	A ADDRESSABLE FF CLEAR
	AND BAFF	0	A6-7	A6-7	B ADDRESSABLE FF CLEAR
	---	A6(INTERNAL)			ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

ST*,CONTINUED

ROM ADDRESS: 135
ROM MICROINSTRUCTION: 42376376 100 0100 11111 1100 1111 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
AAB	IF $\overline{\text{AAFF}}$	0	A6-5	A3-52	A IS ADDRESSED
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF BAFF	1	A6-7	A3-43	B IS ADDRESSED
	STB	1	A3-63	A5-79	B = T-BUS
	IF $\overline{\text{AAFF}}$	1	A6-5	A3-52	A NOT ADDRESSED
	AND BAFF	0	A6-7	A3-43	B NOT ADDRESSED
	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---		A6(INTERNAL)		ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

ST*,CONTINUED

ROM ADDRESS: 136
ROM MICROINSTRUCTION: 42371375 100 0100 11111 0010 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
T	SELT	1	A3-30	A107-74	T = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE
					(PAGE 4-30)

ST*,CONTINUED

ROM ADDRESS: 137
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-64. SHIFT-ROTATE GROUP. All shift-rotate group (SRG) instructions direct the central processor to one of two sets of ROM microinstructions. One set is executed for SRG instructions that operate on the A-register and the other for B-register SRG instructions. Decoding of the SRG instructions is accomplished by an SRG decoder. The decoder is enabled by an SRG1 in the ROM special field which gates bits 6 through 9 of the instruction field to the decoder and an SRG2 in the ROM special field which gates bits 0 through 2, and 4 to the decoder. Detailed signal information for the SRG decoder is given on page 4-94.

4-65. SRGA Instructions. Shift-rotate instructions that operate on the A-register and the NOP instruction direct the central processor to ROM address 100 and execute the microinstructions at ROM addresses 100 through 103. Execution of these microinstructions results in the following:

a. ROM address 100. Enables I-register bits 6 through 9 to the SRG decoder (page 4-94), transfers the A-register content via the R-bus to the function generator and shifter circuits where decoded SRG instructions are applied, and stores the result in the A-register.

b. ROM address 101. Transfers the A-register content via the R-bus to the function generator and shifter circuits where it is tested for possible program skip conditions.

c. ROM address 102. Enables I-register bits 0 through 2 and 4 of the SRG decoder (page 4-94), transfers the A-register content to the function generator and shifter circuits where decoded SRG instructions are applied, stores the result in the A-register, and sets the phase logic to the next phase.

d. ROM address 103. No significant operation.

4-66. The following pages provide ROM decoding and signal information for the SRGA microinstructions.

SRGA, ALL SRG ON A-REG

ROM ADDRESS: 100
ROM MICROINSTRUCTION: 07777117 000 1111 11111 1110 0100 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
SRG1	---		A6(INTERNAL)		ENABLE SRG DECODE OF I(6-9) (PAGE 4-94) SET SRG FF
SKIP					
NOP	---				NO OPERATION

SRGA, CONTINUED

ROM ADDRESS: 101
ROM MICROINSTRUCTION: 07777777 000 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

SRGA, CONTINUED

ROM ADDRESS: 102
ROM MICROINSTRUCTION: 07777135 000 1111 11111 1110 0101 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
SRG2	---		A6(INTERNAL)		ENABLE SRG DECODE OF I(0-2) AND I(4) (PAGE 4-94)
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

SRGA.CONTINUED

ROM ADDRESS: 103
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-67. SRGB Instructions. Shift-rotate group instructions that operate on the B-register direct the central processor to ROM address 104 and execute the microinstructions at ROM addresses 104 through 107. Execution of these microinstructions results in the following:

a. ROM address 104. Enables I-register bits 6 through 9 to the SRG decoder (page 4-94), transfers the B-register content via the R-bus to the function generator and shifter circuits where decoded SRG instructions are applied, and stores the result in the B-register.

b. ROM address 105. Transfers the B-register content via the R-bus to the function generator and shifter circuits where it is tested for possible program skip conditions if required by an SL* instruction (instruction word bit 3).

c. ROM address 106. Enables I-register bits 0 through 2 and 4 to the SRG decoder (page 4-94), transfers the B-register content to the function generator and shifter circuits where decoded SRG instructions are applied, stores the result in the B-register, and sets the phase logic to the next phase.

d. ROM address 107. No significant operation.

4-68. The following pages provide ROM decoding and signal information for the SRGB microinstructions.

SRGB, ALL SRG ON B-REG

ROM ADDRESS: 104
ROM MICROINSTRUCTION: 17776517 001 1111 11111 1101 0100 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
SRG1	---		A6(INTERNAL)		ENABLE SRG DECODE OF I(6-9) (PAGE 4-94) SET SRG FF
SKIP					
NOP	---				NO OPERATION

SRGB,CONTINUED

ROM ADDRESS: 105
ROM MICROINSTRUCTION: 17777777 001 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

SRGB.CONTINUED

ROM ADDRESS: 106
ROM MICROINSTRUCTION: 17776535 001 1111 11111 1101 0101 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
SRG2	---		A6(INTERNAL)		ENABLE SRG DECODE OF I(0-2) AND I(4) (PAGE 4-94)
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

SRGB,CONTINUED

ROM ADDRESS: 107
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

SRG Decoder

INSTRUCTION	SIGNAL(S)	LEVEL	SOURCE	COMMENTS
*LS	SL1	1	A6-71	Shift left 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then ALX14	1	A6-3	back in bit 15
*RS	SR1	1	A6-72	Shift right 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then ALX16	1	A6-17	back in bit 15
R*L	SL1	1	A6-71	Shift left 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then LSI	1	A6-20	in bit 0
R*R	SR1	1	A6-72	Shift right 1
	If ALU0	1	A5-58	Puts bit 0 content
	Then ALX16	1	A6-17	in bit 15
*LR	ARSS	0	A6-25	Right Shift A- or B-register
ER*	SR1	1	A6-72	Shift right 1
	If EXTEND FF	1	A6(internal)	Puts extend bit
	Then ALX16	1	A6-17	in bit 15
	If ALU0	1	A5-58	Puts bit 0 content
	Then EXTEND FF	1	A6(internal)	in EXTEND FF
EL*	SL1	1	A6-71	Shift left 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then EXTEND FF	1	A6(internal)	in EXTEND FF
	If EXTEND FF	1	A6(internal)	Puts extend bit
	Then LSI	1	A6-20	in bit 0
*LF	$\overline{SL4}$	0	A6-50	Shift left 4
SL* (note 1)	If ALU0	0	A5-58	Least sig. bit = 0
	Then SCRY	1	A6-28	Set P-register increment logic
CLE (note 1)	–	–	A6(internal)	Clears EXTEND FF

NOTES: 1. SL* and CLE is decoded after any SRG1 instruction and before any SRG2 instruction.

2. * equals users choice of A- or B-register.

4-69. ALTER-SKIP GROUP. All alter-skip group (ASG) instructions direct the central processor to one of four sets of ROM microinstructions. If the instruction contains a CL* code, the microinstructions designated ASGA are executed. If the instruction contains a CM* code, the microinstructions designated ASGB are executed. If the instruction contains a CC* code, the microinstructions designated ASGC are executed. If the instruction does not contain a CL*, CM*, or CC*, the microinstructions designated ASGD are executed. All ASG instructions except CL*, CM*, and CC* are decoded by two decoders designated ASG1 and ASG2 and enabled by ASG1 and ASG2 codes in the ROM special fields. Detailed signal information for the decoders is given on page 4-107.

4-70. ASGA Instructions. If a CL* instruction is included as part of an alter-skip group instruction, the central processor is directed to ROM address 025 and ROM microinstructions 025, 026, and 027 are executed. Execution of these microinstructions results in the following:

a. ROM address 025. Clears the selected register (A or B as determined by bit 11 of the instruction word), enables the ASG1 decoder, and provides an all "0's" word to be checked for program skips in the event that the instruction word contains an SS* or SL* code.

b. ROM address 026. Enables the ASG2 decoder, transfers the selected register content to the function generator and shifter circuits in the event that the instruction word contains an IN* or SZ* code, and sets the phase logic to the next phase.

c. ROM address 027. No significant operation.

4-71. The following pages provide ROM decoding and signal information for the execute phase of an ASGA instruction.

ASGA,CL* EXECUTE PHASE

ROM ADDRESS: 025
ROM MICROINSTRUCTION: 77775657 111 1111 11111 1011 1010 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG1	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(3-7) (PAGE 4-107)
SKIP					
NOP	---				NO OPERATION

ASGA,CONTINUED

ROM ADDRESS: 026
ROM MICROINSTRUCTION: 47525675 100 1111 01010 1011 1011 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
ADD0	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	ENOV	1	A4-51	A6-83	ENABLE OVERFLOW LOGIC
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG2	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(0-2) (PAGE 4-107)
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ASGA,CONTINUED

ROM ADDRESS: 027
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-72. ASGB Instructions. If a CM* instruction is included as part of an alter-skip group instruction, the central processor is directed to ROM address 031 and ROM microinstructions 031, 032, and 033 are executed. Execution of these microinstructions results in the following:

a. ROM address 031. Complements the selected register (A or B as determined by bit 11 of the instruction word), enables the ASG1 decoder, and provides the complemented word to be checked for program skips in the event that the instruction word contains an SS* or SL* code.

b. ROM address 032. Enables the ASG2 decoder, transfers the selected register content to the function generator and shifter circuits in the event that the instruction word contains an IN* or SZ* code, and sets the phase logic to the next phase.

c. ROM address 033. No significant operation.

4-73. The following pages provide ROM decoding and signal information for the execute phase of an ASGB instruction.

ASGB•CM* EXECUTE PHASE

ROM ADDRESS: 031
ROM MICROINSTRUCTION: 47555657 100 1111 01101 1011 1010 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
NOR	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NEGATIVE OR
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG1	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(3-7) (PAGE 4-107)
SKIP					
NOP	---				NO OPERATION

ASGB•CONTINUED

ROM ADDRESS: 032
ROM MICROINSTRUCTION: 47525675 100 1111 01010 1011 1011 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
ADDO	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	ENOV	1	A4-51	A6-83	ENABLE OVERFLOW LOGIC
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG2	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(0-2) (PAGE 4-107)
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ASGB, CONTINUED

ROM ADDRESS: 033
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-74. ASGC Instruction. If a CC* instruction is included as part of an alter-skip group instruction, the central processor is directed to ROM address 035 and ROM microinstructions 035, 036, and 037 are executed. Execution of these microinstructions results in the following:

a. ROM address 035. Clears and complements the selected register (A or B as determined by bit 11 of the instruction word), enables the ASG1 decoder, and provides an all "1's" word to be checked in the event that the instruction word contains an SS* or SL* code.

b. ROM address 036. Enables the SRG2 decoder, transfers the selected register content to the function generator and shifter circuits in the event that the instruction word contains an IN* or SZ* code, and sets the phase logic to the next phase.

c. ROM address 037. No significant operation.

4-75. The following pages provide ROM decoding and signal information for the execute phase of an ASGC instruction.

ASGC,CC* EXECUTE PHASE

ROM ADDRESS: 035
ROM MICROINSTRUCTION: 77555657 111 1111 01101 1011 1010 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
NOR	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NEGATIVE OR
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG1	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(3-7) (PAGE 4-107)
SKIP					
NOP	---				NO OPERATION

ASGC, CONTINUED

ROM ADDRESS: 036
ROM MICROINSTRUCTION: 47525675 100 1111 01010 1011 1011 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
ADDO	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	ENOV	1	A4-51	A6-83	ENABLE OVERFLOW LOGIC
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG2	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(0-2) (PAGE 4-107)
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ASGC, CONTINUED

ROM ADDRESS: 037
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-76. ASGD Instructions. If CL*, CM*, or CC* codes are not included as part of an alter-skip group instruction, the central processor is directed to ROM address 021 and ROM microinstructions 021, 022, and 023 are executed. Execution of these microinstructions results in the following:

a. ROM address 021. Enables the ASG1 decoder and provides the content of the selected register (A or B as determined by bit 11 of the instruction word) to be checked for program skips in the event that the instruction word contains an SS* or SL* code.

b. ROM address 022. Enables the ASG2 decoder, transfers the selected register content to the function generator and shifter circuits in the event that the instruction word contains an IN* or SZ* code, and sets the phase logic to the next phase.

c. ROM address 023. No significant operation.

4-77. The following pages provide ROM decoding and signal information for the execute phase of an ASGD instruction.

ASGD,ASG NOT CL*,CM*,OR CC*

ROM ADDRESS: 021
ROM MICROINSTRUCTION: 47777657 100 1111 11111 1111 1010 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
ASG1	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(3-7) (PAGE 4-107)
SKIP					
NOP	---				NO OPERATION

ASGD, CONTINUED

ROM ADDRESS: 022
ROM MICROINSTRUCTION: 47525675 100 1111 01010 1011 1011 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
ADD0	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	ENOV	1	A4-51	A6-83	ENABLE OVERFLOW LOGIC
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
ASG2	---		A6(INTERNAL)		ENABLE ASG DECODE OF I(0-2) (PAGE 4-107)
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ASGD•CONTINUED

ROM ADDRESS: 023
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

ASG1 Decoder

INSTRUCTION	SIGNAL(S)	LEVEL	SOURCE	COMMENTS
CLE	–	–	A6(internal)	Clears EXTEND FF
CME	–	–	A6(internal)	Complements EXTEND FF
CCE	–	–	A6(internal)	Sets EXTEND FF
†SEZ	If EXTEND FF	0	A6(internal)	
	Then SCRY	1	A6-28	Sets increment P-register logic
†SL*	If ALU0	0	A5-58	Select register, bit 0
	Then SCRY	1	A6-28	Sets increment P-register logic
†SS*	If ALU15	0	A5-21	Select register, bit 15
	Then SCRY	1	A6-28	Sets increment P-register logic

NOTES: † RSS (I-register, bit 0 = 1) reverses condition for skip.
* equals user choice of A- or B-register.

ASG2 Decoder

INSTRUCTION	SIGNAL(S)	LEVEL	SOURCE	COMMENTS
IN*	$\overline{\text{CIN}}$	0	A6-84	Carry in to ALU Function Generator
†SZ*	If TBZ	1	A5-25	T-bus = all 0's
	Then SCRY	1	A6-28	Sets increment P-register logic

NOTES: † RSS (I-register, bit 0 = 1) reverses condition for skip.
* equals user choice of A- or B-register.

4-78. INPUT/OUTPUT GROUP. Five sets of ROM microinstructions handle the execution of the input/output (I/O) group of user instructions. The LI*, MI*, and OT* instructions are each executed with unique sets of microinstructions. The remaining I/O instructions are divided into a flag group (STF, CLF, SFC, SFS, STO, CLO, SOC, SOS, and HLT) and a control group (STC and CLC) and are designated FLAG and CTRL respectively. The I/O group circuits are enabled by an IOG1 code in the special field of a ROM microinstruction. Flag and control group instructions are decoded by an I/O instruction decoder (hardware) which is also enabled by the IOG1 code. Signal information and timing details for the I/O instruction decoder is provided on page 4-128.

4-79. LI* Instruction. The LI* instruction execute phase directs the central processor to ROM address 064 and executes the microinstructions at ROM addresses 064 through 067. Execution of these microinstructions results in the following:

a. ROM address 064. Enables the I/O group instruction decoder which remains enabled for the remainder of the I/O cycle.

b. ROM address 065. Occupies the central processor to allow sufficient time for the I/O cycle.

c. ROM address 066. Transfers the I/O-bus data (input from the I/O device) to the S-bus allowing time for the input data lines to settle before the store operation in the next microinstruction (ROM address 067) is executed. Sets the phase logic to the next phase.

d. ROM address 067. Stores the I/O-bus content (input data) in the selected register (A or B as determined by bit 11 of the I/O instruction word).

4-80. The following pages provide ROM decoding and signal information for the execute phase of an LI* instruction.

LI*, EXECUTE PHASE

ROM ADDRESS: 064
ROM MICROINSTRUCTION: 77777737 111 1111 11111 1111 1101 1111
CONDITION: T2

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
IOG1	IOG1	1	A6-21	A7-38	ENABLE I/O INST DECODER (PAGE 4-128)
SKIP					
NOP	---				NO OPERATION

LI*,CONTINUED

ROM ADDRESS: 065
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

LI*,CONTINUED

ROM ADDRESS: 066
ROM MICROINSTRUCTION: 70777775 111 0001 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
IOI	RIOI	1	A3-34	A8-61	S-BUS = IO-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

LI*,CONTINUED

ROM ADDRESS: 067
ROM MICROINSTRUCTION: 70775777 111 0001 11111 1011 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
IOI	RIOI	1	A3-34	A8-61	S-BUS = IO-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
CAB	IF IR11	0	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-81. MI* Instruction. The MI* instruction execute phase directs the central processor to ROM address 060 and executes the microinstructions at ROM addresses 060 through 063. Execution of these microinstructions results in the following:

a. ROM address 060. Enables the I/O section and I/O instruction decoder which remains enabled for the remainder of the I/O cycle.

b. ROM address 061. Occupies the central processor to allow sufficient time for the I/O cycle.

c. ROM address 062. Transfers the I/O-bus data (input from the I/O device) to the S-bus allowing time for the input data lines to settle before the store operation in the next microinstruction (ROM address 063) is executed. Sets the phase logic to the next phase.

d. ROM address 063. Inclusive OR's (merges) the content of the selected register (determined by bit 11 of the I/O instruction word) with the I/O-bus data (input) and stores the results in the selected register.

4-82. The following pages provide ROM decoding and signal information for the execute phase of the MI* instruction.

MI*, EXECUTE PHASE

ROM ADDRESS: 060
ROM MICROINSTRUCTION: 77777737 111 1111 11111 1111 1101 1111
CONDITION: T2

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
IOG1	IOG1	1	A7-38	A6-21	ENABLE I/O INST DECODER (PAGE 4-128)
SKIP					
NOP	---				NO OPERATION

MI*,CONTINUED

ROM ADDRESS: 061
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

MI*,CONTINUED

ROM ADDRESS: 062
ROM MICROINSTRUCTION: 70777775 111 0001 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
IOI	RIOI	1	A3-34	A8-61	S-BUS = IO-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

MI*,CONTINUED

ROM ADDRESS: Ø63
ROM MICROINSTRUCTION: 40775777 100 0001 11111 1011 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	Ø	A4-22	A5-5	ENABLE R-BUS
	IF IR11	Ø	A6-58	A4-24	INST WORD SELECTS A
	RBS1	Ø	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
IOI	RIOI	1	A3-34	A8-61	S-BUS = IO-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FNØ	Ø	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
CAB	IF IR11	Ø	A6-58	A3-71	INST WORD SELECTS A
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF IR11	1	A6-58	A3-71	INST WORD SELECTS B
	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-83. OT* Instruction. The OT* instruction execute phase directs the central processor to ROM address 070 and executes the microinstructions at ROM addresses 070 through 073. Execution of these microinstructions results in the following:

a. ROM address 070. Enables the I/O section and I/O instruction decoder which remains enabled for the remainder of the I/O cycle.

b. ROM address 071. Puts the contents of the selected register (A or B determined by bit 11 of the I/O instruction word) on the S-bus.

c. ROM address 072. Transfers the content of the selected register via the R-, S-, and I/O-buses to the selected I/O channel, and sets the phase logic to the next phase.

d. Continues transfer of the selected register content to the selected I/O channel.

4-84. The following pages provide ROM decoding and signal information for the execute phase of the OT* instruction.

OT*, EXECUTE PHASE

ROM ADDRESS: 070
ROM MICROINSTRUCTION: 77777737 111 1111 11111 1111 1101 1111
CONDITION: T2

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
IOG1	IOG1	1	A7-38	A6-21	ENABLE I/O INST DECODER (PAGE 4-128)
SKIP					
NOP	---				NO OPERATION

OT*,CONTINUED

ROM ADDRESS: 071
ROM MICROINSTRUCTION: 42377777 100 0100 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

OT*•CONTINUED

ROM ADDRESS: 072
ROM MICROINSTRUCTION: 42370375 100 0100 11111 0000 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
IOO	SIOB	1	A3-46	A8-33	I/O-BUS = S-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

OT*,CONTINUED

ROM ADDRESS: 073
ROM MICROINSTRUCTION: 42370377 100 0100 11111 0000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
CAB	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	IF IR11	0	A6-58	A4-24	INST WORD SELECTS A
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF IR11	1	A6-58	A4-24	INST WORD SELECTS B
	RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
IOO	SIOB	1	A3-46	A8-33	I/O-BUS = S-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-85. Flag Group Instructions. All flag group I/O instructions direct the central processor to ROM address 040 and execute the microinstructions at ROM addresses 040 through 043. These four microinstructions occupy the central processor to provide sufficient time for execution of the I/O instruction. The significant operations directed by these microinstructions are:

a. ROM address 040. Enables the I/O section and I/O group instruction decoder.

b. ROM address 042. Sets the phase logic to the next phase.

4-86. The following pages provide ROM decoding and signal information for the execute phase of a flag group I/O instructions.

for STF, CLF, SFS, SFC, etc only

FLAG,I/O FLAG GROUP

ROM ADDRESS: 040
ROM MICROINSTRUCTION: 77777737 111 1111 11111 1111 1101 1111
CONDITION: T2

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
IOG1	IOG1	1	A7-38	A6-21	ENABLE I/O INST DECODER (PAGE 4-128)
SKIP					
NOP	---				NO OPERATION

FLAG•CONTINUED

ROM ADDRESS: 041
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

FLAG,CONTINUED

ROM ADDRESS: 042
ROM MICROINSTRUCTION: 77777775 111 1111 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

FLAG, CONTINUED

ROM ADDRESS: 043
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-87. Control Group Instructions. All control group I/O instructions direct the central processor to ROM address 074 and execute the microinstructions at ROM addresses 074 through 077. These four microinstructions occupy the central processor to provide sufficient time for execution of the I/O instruction. The significant operations directed by these microinstructions are:

a. ROM address 074. Enables the I/O section and I/O group instruction decoder.

b. ROM address 076. Sets the phase logic to the next phase.

4-88. The following pages provide ROM decoding and signal information for the execute phase of the control group I/O instructions.

for STC, CLC only

CTRL, I/O CONTROL GP, EXECUTE PHASE

ROM ADDRESS: 074
ROM MICROINSTRUCTION: 77777737 111 1111 11111 1111 1101 1111
CONDITION: T2

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
IOG1	IOG1	1	A7-38	A6-21	ENABLE I/O INST DECODER (PAGE 4-128)
SKIP					
NOP	---				NO OPERATION

CTRL, CONTINUED

ROM ADDRESS: 075
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

CTRL, CONTINUED

ROM ADDRESS: 076
ROM MICROINSTRUCTION: 77777775 111 1111 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

CTRL, CONTINUED

ROM ADDRESS: 077
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

I/O Group Decoder

INSTRUCTION	SIGNAL(S)	SOURCE	DESTINATION	TIME	COMMENTS
CLF(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	CLF	A8-51	*-7	T4	Clear Flag
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
STF(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	STF	A8-49	*-9	T3	Set Flag
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
SFC(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	SFC	A8-52	*-5	T3-T6	Skip if Flag Clear
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
SFS(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	SFS	A8-59	*-25	T3-T6	Skip if Flag Set
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
STO	STF	A8-49	A4-73	T3	Set Overflow
	SC01	A7-49	A4-71	T3-T6	
CLO	CLF	A8-51	A4-76	T4	Clear Overflow
	SC01	A7-49	A4-71	T3-T6	
SOC	SFC	A8-52	A4-70	T3-T6	Skip if Overflow Clear
	SC01	A7-49	A4-71	T3-T6	
SOS	SFS	A8-59	A4-72	T3-T6	Skip if Overflow Set
	SC01	A7-49	A4-71	T3-T6	
HLT	HIN	A8-50	A1-65 A24-74	T3	Program Halt
STC(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	STC	A8-55	*-22	T4	Set Control
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
CLC(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	CLC	A8-66	*-21	T4	Clear Control
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
OTA/B	IOG	A8-46	*-15	T3-T6	Input/Output Group
	IOO	A8-78	*-16,34	T3-T4	Enable I/O Bus Data to Interface Card
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	

*Signals routed to all interface card slots. See the backplane wire list (Diagrams Manual) for card and pin number references.

4-89. EXTENDED ARITHMETIC GROUP. The extended arithmetic group information is divided into left shifts and rotates; right shifts and rotates; MULT, DIVID, DLD, and DST instructions; followed by the OPGET, GETAD, and PDEC subroutines.

4-90. Left Shifts and Rotates. All EAG left shifts and rotates are accomplished using the F- and Q-registers. Before the actual shift or rotate operation, the following initiation always takes place:

a. The F-register content (memory protect "fence") is transferred to the SP3-register for interim storage.

b. The A-register content is transferred to the Q-register, and the B-register content is transferred to the F-register.

c. An S-bus field ADR microcode gets the low order bits (0 through 9) from the I-register and the high order bits (10 through 15) from the P-register. This 16-bit word is made negative by a SUB microcode in the Function field, and the result is stored in the SP2-register. Bits 0 through 3 of this word are the only significant bits and in their present form are the "2's" complement of the number of shifts or rotates specified in the original instruction word.

d. This 4-bit word is then transferred to the repeat counter (CNTR microcode in the Special field) and the REPEAT FF is cleared (RPT microcode in the Skip field).

e. In summary:

(1) SP3 :=F;
(2) Q :=A, F :=B;
(3) SP2 := - (I(0:9) + P(10:15));
(4) CNTR :=SP2(0:3), REPEAT FF :=CLEAR

4-91. The following shift operation is common to all EAG left shift and rotate operations:

a. The F-register content is read onto the R-bus and inclusive "or'ed" to the ALU shifter. A left shift is applied at the shifter, and the result is stored in the F-register.

b. Simultaneously with the above, the Q-register is shifted left. Bit 15 of the Q-register is applied to the ALU circuits to become bit 0 of the word stored in the F-register. The source of bit 0 input to the Q-register and the disposition of the high order bits (14 and 15) depends on the particular instruction word (ASL, LSL, or RRL).

4-92. Each time a shift operation is executed, the repeat counter is incremented. When the repeat count is 1111, the specified number of operations has been accomplished and the REPEAT FF is set. The remainder of the operation is then as follows:

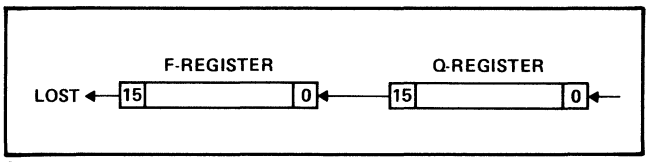
a. F-register content is transferred to the B-register.

b. Q-register content is transferred to the A-register.

c. SP3-register is transferred to the F-register restoring the memory protect "fence" address.

4-93. LSL (Logical Shift Left) Instruction. Bit 0 input to the Q-register is always zero. Bit 15 of the F-register is lost. No overflow or sign considerations are made. Figure 4-6 shows the LSL operation.

4-94. The following pages provide ROM decoding and signal information for the execute phase of the LSL instruction.



2133-105

Figure 4-6. LSL Operation

LSL•EXECUTE PHASE

ROM ADDRESS: 202
ROM MICROINSTRUCTION: 37222622 011 1110 10010 0101 1001 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
		NOTE			
	THIS MICROINSTRUCTION SERVES AS THE ENTRY POINT FOR THE LSL USER INSTRUCTION; HOWEVER, SINCE AN LEP (LEGAL ENTRY POINT) CODE DOES NOT APPEAR IN THE SPECIAL FIELD, THE MICROINSTRUCTION EXECUTES AS A NOP.				

ROM ADDRESS: 203
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

LSL, CONTINUED

ROM ADDRESS: 204
ROM MICROINSTRUCTION: 37222742 011 1110 10010 0101 1110 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{JMPS}$	0	A4-46	A1-73	ROM JUMP
	$\overline{SRAR}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{JMPF}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
LSLA	---				SET ROM ADDRESS 342 (PAGE 4-132)
SKIP					
NOP	---				NO OPERATION

LSL•CONTINUED

ROM ADDRESS: 342
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

LSL, CONTINUED

ROM ADDRESS: 343
ROM MICROINSTRUCTION: 17774777 001 1111 11111 1001 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

LSL•CONTINUED

ROM ADDRESS: 344
ROM MICROINSTRUCTION: 07775377 000 1111 11111 1010 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
Q	SQM	1	A3-70	A5-75	SET Q TO PARALLEL INPUT MODE
	STQ	1	A3-80	A5-73	Q = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

LSL•CONTINUED

ROM ADDRESS: 345
ROM MICROINSTRUCTION: 75377461 111 1010 11111 1111 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

LSL•CONTINUED

ROM ADDRESS: 346
ROM MICROINSTRUCTION: 37664430 011 1111 10110 1001 0001 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
LGS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF SR1	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
L1	SL1	1	A6-71	A4-6	ENABLE FUNCT LEFT SHIFT
	TBS2	1	A4-44	A5-54	SHIFT T-BUS LEFT 1
SKIP					
CTRI	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER
	REVERSE IF RSS IN SPECIAL FIELD				

LSL•CONTINUED

ROM ADDRESS: 347
ROM MICROINSTRUCTION: 37776777 011 1111 11111 1101 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

LSL, CONTINUED

ROM ADDRESS: 350
ROM MICROINSTRUCTION: 27777375 010 1111 11111 1110 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
Q	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = Q
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

LSL•CONTINUED

ROM ADDRESS: 351
ROM MICROINSTRUCTION: 74774777 111 100 11111 100 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-95. ASL (Arithmetic Shift Left) Instruction. Bit 0 input to the Q-register is always zero. The sign bit (bit 15) of the F-register is always copied back into bit 15 of the F-register. If bit 14 of the F-register is significant, i.e., if the sign is positive (bit 15 = 0) and bit 14 = 1, or if the sign is negative (bit 15 = 1) and bit 14 = 0, the OVF ("not" Overflow) FF is cleared. This amounts to an exclusive "or" of the F-register bits 14 and 15 applied to the OVF FF. If bit 14 is not significant, the OVF FF is set. Other than the consideration for the OVF FF, bit 14 of the F-register is lost. Figure 4-7 graphically describes the ASL operation.

4-96. The following pages provide ROM decoding and signal information for the execute phase of the ASL instruction.

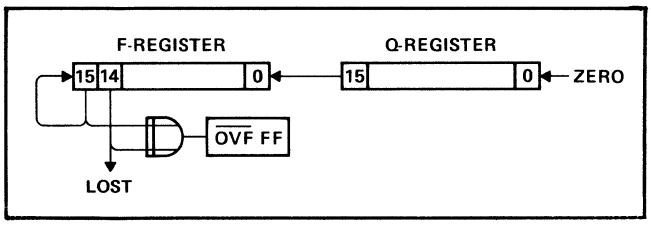


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Figure 4-7. ASL Operation

ASL•EXECUTE PHASE

ROM ADDRESS: 201
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

ASL•CONTINUED

ROM ADDRESS: 202
ROM MICROINSTRUCTION: 37222622 011 1110 10010 0101 1001 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{JMPS}$	0	A4-46	A1-73	ROM JUMP
	$\overline{SRAR}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{JMPF}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
ASLA	---				SET ROM ADDRESS 222 (PAGE 4-142)
SKIP					
NOP	---				NO OPERATION

ASL•CONTINUED

ROM ADDRESS: 222
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

ASL•CONTINUED

ROM ADDRESS: 223
ROM MICROINSTRUCTION: 17754777 001 1111 11101 1001 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CLO	---		A4(INTERNAL)		CLEAR OVERFLOW LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

ASL•CONTINUED

ROM ADDRESS: 224
ROM MICROINSTRUCTION: 07775377 000 1111 11111 1010 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
Q	SQM	1	A3-70	A5-75	SET Q TO PARALLEL INPUT MODE
	STQ	1	A3-80	A5-73	Q = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

ASL,CONTINUED

ROM ADDRESS: 225
ROM MICROINSTRUCTION: 75377461 111 1010 11111 1111 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

ASL,CONTINUED

ROM ADDRESS: 226
ROM MICROINSTRUCTION: 37704430 011 1111 11000 1001 0001 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
ARS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	$\overline{FN3}$	1	A4-5	A5-55	
	$\overline{ARS}$	0	A4-84	A6-18	32-BIT ARITHMETIC SHIFT
	$\overline{ARSS}$	0	A6-25	A4-33	ARITH SHIFT SIGN BIT
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF ALU15	1	A5-21	A4-35	ALU BIT 15 = 1
	ALX14	1	A4-41	A5-7	INPUT TO ALU SHIFTER
	ALX16	1	A4-9	A5-23	INPUT TO ALU SHIFTER
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
				A4-6	
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF ALU14	0	A5-22	A4-38	ALU BIT 14 = 0
	AND ALU15	1	A5-21	A4-35	ALU BIT 15 = 1
	OR ALU14	1	A5-22	A4-38	ALU BIT 14 = 1
	AND ALU15	0	A5-21	A4-35	ALU BIT 15 = 0
	---		A4(INTERNAL)		SET OVERFLOW LOGIC
	IF SRI	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
L1	SL1	1	A6-71	A4-6	ENABLE FUNCT LEFT SHIFT
	TBS2	1	A4-44	A5-54	SHIFT T-BUS LEFT 1
SKIP					
CTRI	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER
	REVERSE IF RSS IN SPECIAL FIELD				

ASL, CONTINUED

ROM ADDRESS: 227
ROM MICROINSTRUCTION: 27777377 010 1111 11111 1110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
Q	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = Q
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

ASL, CONTINUED

ROM ADDRESS: 230
ROM MICROINSTRUCTION: 37776775 011 1111 11111 1101 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ASL•CONTINUED

ROM ADDRESS: 231
ROM MICROINSTRUCTION: 74774777 111 1001 11111 1001 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-97. RRL (Rotate Left) Instruction. Bit 0 input to the Q-register is the output bit 15 of the F-register. No overflow or sign considerations are made. Figure 4-8 shows the RRL operation.

4-98. The following pages provide ROM decoding and signal information for the execute phase of the RRL instruction.

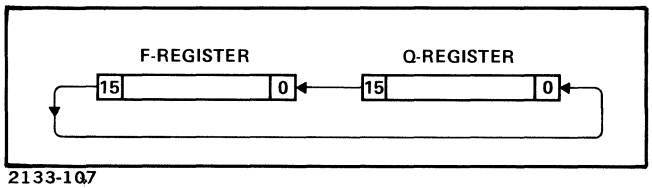


Figure 4-8. RRL Operation

RRL, EXECUTE PHASE

ROM ADDRESS: 204
ROM MICROINSTRUCTION: 37222742 011 1110 10010 0101 1110 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS

NOTE

THIS MICROINSTRUCTION SERVES AS THE ENTRY POINT FOR THE RRL USER INSTRUCTION; HOWEVER, SINCE AN LEP (LEGAL ENTRY POINT) CODE DOES NOT APPEAR IN THE SPECIAL FIELD, THE MICROINSTRUCTION EXECUTES AS A NOP.

RRL•CONTINUED

ROM ADDRESS: 205
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

RRL, CONTINUED

ROM ADDRESS: 206
ROM MICROINSTRUCTION: 37222752 011 1110 10010 0101 1110 1010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
RRLA	---				SET ROM ADDRESS 352 (PAGE 4-153)
SKIP					
NOP	---				NO OPERATION

RRL,CONTINUED

ROM ADDRESS: 352
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

RRL•CONTINUED

ROM ADDRESS: 353
ROM MICROINSTRUCTION: 17774777 001 1111 11111 1001 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

RRL•CONTINUED

ROM ADDRESS: 354
ROM MICROINSTRUCTION: 07775377 000 1111 11111 1010 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
Q	SQM	1	A3-70	A5-75	SET Q TO PARALLEL INPUT MODE
	STQ	1	A3-80	A5-73	Q = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

RRL•CONTINUED

ROM ADDRESS: 355
ROM MICROINSTRUCTION: 75377461 111 1010 11111 1111 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

RRL•CONTINUED

ROM ADDRESS: 356
ROM MICROINSTRUCTION: 37674430 011 1111 10111 1001 0001 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CRS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF ALU15	1	A5-21	A4-35	ALU BIT 15 = 1
	QSI	1	A4-42	A5-83	Q SHIFT INPUT = 1
	IF AR0	1	A5-45	A4-36	A BIT 0 = 1
	ALX16	1	A4-41	A5-23	ALU SHIFT INPUT = 1
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF SR1	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
L1	SL1	1	A6-71	A4-6	ENABLE FUNCT LEFT SHIFT
	TBS2	1	A4-44	A5-54	SHIFT T-BUS LEFT 1
SKIP					
CTRI	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER
	REVERSE IF RSS IN SPECIAL FIELD				

RRL•CONTINUED

ROM ADDRESS: 357
ROM MICROINSTRUCTION: 37776777 011 1111 11111 1101 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

RRL, CONTINUED

ROM ADDRESS: 360
ROM MICROINSTRUCTION: 27777375 010 1111 11111 1110 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
Q	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = Q
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

RRL•CONTINUED

ROM ADDRESS: 361
ROM MICROINSTRUCTION: 74774777 111 1001 11111 1001 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-99. Right Shifts and Rotates. Right shifts and rotates are accomplished using the A- and B-registers. Before the actual shift or rotate operation takes place, a counter is initialized as follows:

a. An S-bus field ADR microcode gets the low order bits (0 through 9) from the I-register and the high order bits (10 through 15) from the P-register. This 16-bit word is made negative by a SUB microcode in the Function field, and the result is stored in the SP2-register. Bits 0 through 3 of this word are the only significant bits and in their present form, are the "2's" complement of the number of shifts or rotates specified in the original instruction word.

b. The three significant bits of the above operation are then stored in the repeat counter (by a CNTR microcode in the Special field) and the REPEAT FF is cleared (by an RPT microcode in the Skip field).

4-100. The following shift operation is common to all right shift and rotate operations:

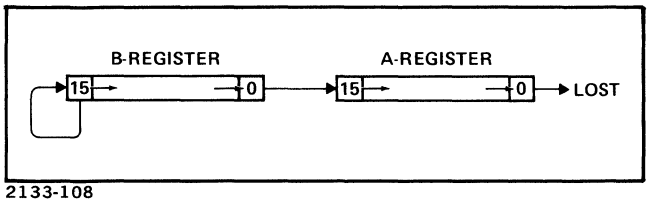
a. The B-register content is read to the R-bus and inclusive "or'ed" to the ALU shifter. A right shift is applied at the shifter, and the result replaces the original B-register content.

b. Simultaneously with the above, the A-register is shifted right. Bit 0 (ALU0) from the ALU shifter is applied as a right shift carry-in to the A-register. The source of bit 15 input to the B-register and the disposition of bit 0 of the A-register depends upon the particular instruction word (ASR, LSR, or RRR).

4-101. The last microinstruction of the ASR (ROM address 0336) and the LSR (ROM address 0342) operations shows an ADR (S-bus field), a SUB (Function field), and an S2 (Store field) microcode. Although these operations are performed, their effect has no significance. These microinstructions actually are part of the execute phase of two other user instructions, and their effect, in this case, is only to allow time for the phase logic to select the next phase of operation.

4-102. ASR (Arithmetic Shift Right) Instruction. The sign bit (bit 15 of the B-register) is always copied back into bit 15 of the B-register. Bit 0 of the A-register is lost. Figure 4-9 shows the ASR operation.

4-103. The following pages provide ROM decoding and signal information for the execute phase of the ASR instruction.



2133-108

Figure 4-9. ASR Operation

ASR•EXECUTE PHASE

ROM ADDRESS: 241
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

ASR,CONTINUED

ROM ADDRESS: 242
ROM MICROINSTRUCTION: 37227732 011 1110 10010 1111 1101 1010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	$\overline{\text{FN3}}$	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
ASRA	---				SET ROM ADDRESS 332 (PAGE 4-163)
SKIP					
NOP	---				NO OPERATION

ASR, CONTINUED

ROM ADDRESS: 332
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	$\overline{\text{FN3}}$	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

ASR,CONTINUED

ROM ADDRESS: 333
ROM MICROINSTRUCTION: 75357461 111 1010 11101 1111 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
CLO	---		A4(INTERNAL)		CLEAR OVERFLOW LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

ASR,CONTINUED

ROM ADDRESS: 334
ROM MICROINSTRUCTION: 17706450 001 1111 11000 1101 0010 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
ARS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{ARS}}$	0	A4-84	A6-18	32-BIT ARITHMETIC SHIFT
	$\overline{\text{ARSS}}$	0	A6-25	A4-33	ARITH SHIFT SIGN BIT
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF ALU15	1	A5-21	A4-35	ALU BIT 15 = 1
	ALX14	1	A4-41	A5-7	INPUT TO ALU SHIFTER
	ALX16	1	A4-9	A5-23	INPUT TO ALU SHIFTER
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
				A4-6	
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF ALU14	0	A5-22	A4-38	ALU BIT 14 = 0
	AND ALU15	1	A5-21	A4-35	ALU BIT 15 = 1
	OR ALU14	1	A5-22	A4-38	ALU BIT 14 = 1
	AND ALU15	0	A5-21	A4-35	ALU BIT 15 = 0
	---		A4(INTERNAL)		SET OVERFLOW LOGIC
	IF SRI	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
R1	SR1	1	A6-72	A4-6	ENABLE FUNCT RIGHT SHIFT
	TBS1	1	A4-45	A5-53	SHIFT T-BUS RIGHT 1
SKIP					
CTRI	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER

REVERSE IF RSS IN SPECIAL FIELD

ASR•CONTINUED

ROM ADDRESS: 335
ROM MICROINSTRUCTION: 77777775 111 1111 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

ASR, CONTINUED

ROM ADDRESS: 336
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-104. LSR (Logical Shift Right) Instruction. The input to bit 15 of the B-register is always zero. Output from bit 0 of the A-register is lost. Figure 4-10 shows the LSR operation.

4-105. The following pages provide ROM decoding and signal information for the execute phase of the LSR instruction.

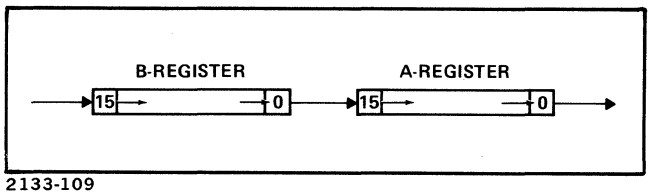


Figure 4-10. LSR Operation

LSR, EXECUTE PHASE

ROM ADDRESS: 242
ROM MICROINSTRUCTION: 37227732 011 1110 10010 1111 1101 1010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS

NOTE

THIS MICROINSTRUCTION SERVES AS THE ENTRY POINT FOR THE LSR USER INSTRUCTION; HOWEVER, SINCE AN LEP (LEGAL ENTRY POINT) CODE DOES NOT APPEAR IN THE SPECIAL FIELD, THE MICROINSTRUCTION EXECUTES AS A NOP.

LSR, CONTINUED

ROM ADDRESS: 243
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

LSR, CONTINUED

ROM ADDRESS: 244
ROM MICROINSTRUCTION: 77227736 111 1110 10010 1111 1101 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
LSRA	---				SET ROM ADDRESS 336 (PAGE 4-171)
SKIP					
NOP	---				NO OPERATION

LSR,CONTINUED

ROM ADDRESS: 336
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	$\overline{FN3}$	0	A4-5	A5-55	
	$\overline{CIN}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

LSR, CONTINUED

ROM ADDRESS: 337
ROM MICROINSTRUCTION: 75377461 111 1010 11111 1111 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

LSR,CONTINUED

ROM ADDRESS: 340
ROM MICROINSTRUCTION: 17666450 001 1111 10110 1101 0010 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
LGS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF SR1	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
R1	SR1	1	A6-72	A4-6	ENABLE FUNCT RIGHT SHIFT
	TBS1	1	A4-45	A5-53	SHIFT T-BUS RIGHT 1
SKIP					
CTR1	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER

REVERSE IF RSS IN SPECIAL FIELD

LSR•CONTINUED

ROM ADDRESS: 341
ROM MICROINSTRUCTION: 77777775 111 1111 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

LSR•CONTINUED

ROM ADDRESS: 342
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-106. RRR (Rotate Right) Instruction. The input to bit 15 of the B-register is the output from bit 0 of the A-register. Figure 4-11 shows the RRR operation.

4-107. The following pages provide ROM decoding and signal information for the execute phase of the RRR instruction.

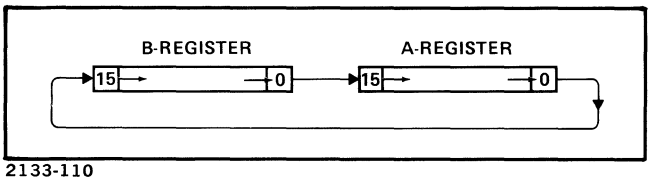


Figure 4-11. RRR Operation

RRR,EXECUTE PHASE

ROM ADDRESS: 244
ROM MICROINSTRUCTION: 77227736 111 1110 10010 1111 1101 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS

NOTE

THIS MICROINSTRUCTION SERVES AS THE ENTRY POINT FOR THE RRR USER INSTRUCTION; HOWEVER, SINCE AN LEP (LEGAL ENTRY POINT) CODE DOES NOT APPEAR IN THE SPECIAL FIELD, THE MICROINSTRUCTION EXECUTES AS A NOP.

RRR,CONTINUED

ROM ADDRESS: 245
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

RRR, CONTINUED

ROM ADDRESS: 246
ROM MICROINSTRUCTION: 73053377 111 0110 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
ADR	IF INM	0	A4-7	A2-67	INDEX MODE FF CLEAR
	ADR	1	A3-16	A2-68	S-BUS(0-9)=I(0-9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	IF INM	1	A4-7	A2-67	INDEX MODE FF SET
	ADR	1	A3-16	A2-68	S-BUS(0-8)=I(0-8)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

RRR•CONTINUED

ROM ADDRESS: 247
ROM MICROINSTRUCTION: 77227540 111 1110 10010 1111 0110 0000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
RRRA	---				SET ROM ADDRESS 140 (PAGE 4-180)
SKIP					
NOP	---				NO OPERATION

RRR•CONTINUED

ROM ADDRESS: 140
ROM MICROINSTRUCTION: 75377461 111 1010 11111 1111 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

RRR,CONTINUED

ROM ADDRESS: 141
ROM MICROINSTRUCTION: 17676450 001 1111 10111 1101 0010 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CRS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF ALU15	1	A5-21	A4-35	ALU BIT 15 = 1
	QSI	1	A4-42	A5-83	Q SHIFT INPUT = 1
	IF AR0	1	A5-45	A4-36	A BIT 0 = 1
	ALX16	1	A4-41	A5-23	ALU SHIFT INPUT = 1
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF SR1	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
R1	SR1	1	A6-72	A4-6	ENABLE FUNCT RIGHT SHIFT
	TBS1	1	A4-45	A5-53	SHIFT T-BUS RIGHT 1
SKIP					
CTR1	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER

REVERSE IF RSS IN SPECIAL FIELD

RRR•CONTINUED

ROM ADDRESS: 142
ROM MICROINSTRUCTION: 77777775 111 1111 11111 1111 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

RRR,CONTINUED

ROM ADDRESS: 143
ROM MICROINSTRUCTION: 77777777 111 1111 11111 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-108. MULT Instruction. The operation of the MULT instruction in flowchart form, is shown in figure 4-12 on page 4-257. The microroutine for the MULT instruction is entered with the multiplicand in the A-register and the address of the memory location containing the multiplier address in the P-register.

4-109. The following pages provide ROM decoding and signal information for the execute phase of the MULT instruction.

MULT, EXECUTE PHASE

ROM ADDRESS: 210
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

MULT,CONTINUED

ROM ADDRESS: 211
ROM MICROINSTRUCTION: 77207762 111 1110 10000 1111 1111 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	---		A4(INTERNAL)		CLEAR $\overline{\text{JSB}}$ FF
	JSB	1	A4-18	A2-69	LOAD ROM SAVE REGISTER
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	SRAR	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD SUBROUTINE ADR IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
GETAD	---				SET ROM ADDRESS 362 (PAGE 4-247)
SKIP					
NOP	---				NO OPERATION

MULT,CONTINUED

ROM ADDRESS: 212
ROM MICROINSTRUCTION: 77207632 111 1110 10000 1111 1001 1010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	---		A4(INTERNAL)		CLEAR $\overline{\text{JSB}}$ FF
	$\overline{\text{JSB}}$	1	A4-18	A2-69	LOAD ROM SAVE REGISTER
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	SRAR	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD SUBROUTINE ADR IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
OPGET	---				SET ROM ADDRESS 232 (PAGE 4-243)
SKIP					
NOP	---				NO OPERATION

MULT,CONTINUED

ROM ADDRESS: 213
ROM MICROINSTRUCTION: 07222155 000 1110 10010 0100 0110 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{JMPS}$	0	A4-46	A1-73	ROM JUMP
	$\overline{SRAR}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{JMPF}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
S4	WSP4	1	A3-49	A5-71	SP4 = T-BUS
SPECIAL					
MPY	---				SET ROM ADDRESS 155 (PAGE 4-188)
SKIP					
NOP	---				NO OPERATION

MULT,CONTINUED

ROM ADDRESS: 155
ROM MICROINSTRUCTION: 77756461 111 1111 11101 1101 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CLO	---		A4(INTERNAL)		CLEAR OVERFLOW LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

MULT•CONTINUED

ROM ADDRESS: 156
ROM MICROINSTRUCTION: 15036450 001 1010 00011 1101 0010 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
MPY	$\overline{\text{MPY}}$	0	A4-60	A3-39	MULTIPLY FUNCT DECODED
	IF AR0	1	A5-45	A4-36	A-REG BIT 0 = 1
	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	IF $\overline{\text{COUT}}$	0	A5-19	A4-56	ABOVE ADD GIVES A CARRY
	ALX16	1	A4-9	A5-23	ALU SHIFT INPUT = 1
	IF $\overline{\text{COUT}}$	1	A5-19	A4-56	ABOVE ADD GIVES NO CARRY
	ALX16	0	A4-9	A5-23	ALU SHIFT INPUT = 0
	IF AR0	0	A5-45	A4-36	A-REG BIT 0 = 0
	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NO FUNCT (ALU = R-BUS)
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
R1	SR1	1	A6-72	A4-6	ENABLE FUNCT RIGHT SHIFT
	TBS1	1	A4-45	A5-53	SHIFT T-BUS RIGHT 1
SKIP					
CTR1	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER
	REVERSE IF RSS IN SPECIAL FIELD				

MULT,CONTINUED

ROM ADDRESS: 157
ROM MICROINSTRUCTION: 74377403 111 1000 11111 1111 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S4	RSP4	1	A3-8	A5-11	S-BUS = SP4
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

MULT,CONTINUED

ROM ADDRESS: 160
ROM MICROINSTRUCTION: 15056777 001 1010 00101 1101 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRAC1
	FN2	1	A4-4	A5-56	
	$\overline{FN3}$	0	A4-5	A5-55	
	$\overline{CIN}$	0	A4-14	A5-41	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

MULT,CONTINUED

ROM ADDRESS: 161
ROM MICROINSTRUCTION: 75377403 111 1010 11111 1111 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---	A6(INTERNAL)			ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

MULT,CONTINUED

ROM ADDRESS: 162
ROM MICROINSTRUCTION: 14056775 001 1000 00101 1101 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
S4	RSP4	1	A3-8	A5-11	S-BUS = SP4
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	$\overline{FN3}$	0	A4-5	A5-55	
	$\overline{CIN}$	0	A4-14	A5-41	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

MULT•CONTINUED

ROM ADDRESS: 163
ROM MICROINSTRUCTION: 77114377 111 1110 01001 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
INC	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	CARRY IN TO ALU
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-110. DIVID Instruction. The operation of the DIVID instruction, in flowchart form, is shown in figure 4-13 on page 4-259. The microroutine for the DIVID instruction is entered with the low order word of the dividend in the A-register, the high order word of the dividend in the B-register, and the address of the memory location containing the divisor address in the P-register.

4-111. The following pages provide ROM decoding and signal information for the execute phase of the DIVID instruction.

DIVID, EXECUTE PHASE

ROM ADDRESS: 220
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 221
ROM MICROINSTRUCTION: 77227651 111 1110 10010 1111 1010 1001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
DIV	---				SET ROM ADDRESS 251 (PAGE 4-197)
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 251
ROM MICROINSTRUCTION: 77207762 111 1110 10000 1111 1111 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	---		A4(INTERNAL)		CLEAR JSB FF
	JSB	1	A4-18	A2-69	LOAD ROM SAVE REGISTER
	JMPS	0	A4-46	A1-73	ROM JUMP
	SRAR	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD SUBROUTINE ADR IN RAR (SEE SPECIAL FIELD)
	JMPF	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
GETAD	---				SET ROM ADDRESS 362 (PAGE 4-247)
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 252
ROM MICROINSTRUCTION: 37202232 011 1110 10000 0100 1001 1010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	---		A4(INTERNAL)		CLEAR JSB FF
	$\overline{\text{JSB}}$	1	A4-18	A2-69	LOAD ROM SAVE REGISTER
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	SRAR	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD SUBROUTINE ADR IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
S4	WSP4	1	A3-49	A5-71	SP4 = T-BUS
SPECIAL					
OPGET	---				SET ROM ADDRESS 232 (PAGE 4-243)
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 253
ROM MICROINSTRUCTION: 17764763 001 1111 11110 1001 1111 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
SOV	---		A4(INTERNAL)		SET OVERFLOW LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID, CONTINUED

ROM ADDRESS: 254
ROM MICROINSTRUCTION: 07225262 000 1110 10010 1010 1011 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
Q	SQM	1	A3-70	A5-75	SET Q TO PARALLEL INPUT MODE
	STQ	1	A3-80	A5-73	Q = T-BUS
SPECIAL					
DVS	---				SET ROM ADDRESS 262 (PAGE 4-206)
SKIP					
NOP	---				NO OPERATION

DIVID•CONTINUED

ROM ADDRESS: 255
ROM MICROINSTRUCTION: 07773777 000 1111 11111 0111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S1	WSP1	1	A3-55	A5-65	SP1 - T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 256
ROM MICROINSTRUCTION: 17772777 001 1111 11111 0101 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 257
ROM MICROINSTRUCTION: 75455364 111 1011 00101 1010 1111 0100
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	$\overline{FN3}$	0	A4-5	A5-55	
	$\overline{CIN}$	0	A4-14	A5-41	
STORE					
Q	SQM	1	A3-70	A5-75	SET Q TO PARALLEL INPUT MODE
	STQ	1	A3-80	A5-73	Q = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
COUT	IF $\overline{COUT}$	0	A5-19	A6-11	ALU CARRY OUT=1
	---	A6(INTERNAL)			ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID•CONTINUED

ROM ADDRESS: 260
ROM MICROINSTRUCTION: 74554776 111 1001 01101 1001 1111 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
NOR	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NEGATIVE OR
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---		A6(INTERNAL)		ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

DIVID,CONTINUED

ROM ADDRESS: 261
ROM MICROINSTRUCTION: 74454777 111 1001 00101 1001 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID•CONTINUED

ROM ADDRESS: 262
ROM MICROINSTRUCTION: 75373403 111 1010 11111 0111 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S1	WSP1	1	A3-55	A5-65	SP1 - T-BUS
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID,CONTINUED

ROM ADDRESS: 263
ROM MICROINSTRUCTION: 75453377 111 1011 00101 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 264
ROM MICROINSTRUCTION: 35057763 011 1010 00101 1111 1111 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{CIN}$	0	A4-14	A5-41	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID•CONTINUED

ROM ADDRESS: 265
ROM MICROINSTRUCTION: 37226702 100 1110 10010 1101 1100 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	$\overline{\text{FN3}}$	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
DONE	---				SET ROM ADDRESS 302 (PAGE 4-222)
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 266
ROM MICROINSTRUCTION: 37664437 011 1111 10110 1001 0001 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
LGS	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	SHIFT	1	A4-83	A3-78	ENABLE A+Q MODE SELECT
	IF SL1	1	A6-71	A3-65	SPECIAL FIELD DECODED
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF SR1	1	A6-72	A3-62	SPECIAL FIELD DECODED
	SAM	0	A3-67	A5-77	A TO SERIAL INPUT MODE
	STA	1	A3-69	A5-81	RIGHT SHIFT A
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
L1	SL1	1	A6-71	A4-6	ENABLE FUNCT LEFT SHIFT
	TBS2	1	A4-44	A5-54	SHIFT T-BUS LEFT 1
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 267
ROM MICROINSTRUCTION: 77752461 111 1111 11101 0101 0011 0001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CLO	---		A4(INTERNAL)		CLEAR OVERFLOW LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
CNTR	---		A6(INTERNAL)		COUNTER=S-BUS(0-3)
SKIP					
RPT	---		A6(INTERNAL)		SET REPEAT LOGIC

DIVID,CONTINUED

ROM ADDRESS: 270
ROM MICROINSTRUCTION: 35044430 011 1010 00100 1001 0001 1000
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
DIV	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-66	
	$\overline{CIN}$	0	A4-14	A5-41	
	$\overline{DIV}$	0	A4-58	A3-82	DIVIDE FUNCT DECODED
	SQM	0	A3-70	A5-75	Q TO SERIAL INPUT MODE
	$\overline{FRZ}$	0	A3-35	A1-80	CPU FREEZE (SEE NOTE)
	STQ	1	A3-80	A5-73	LEFT SHIFT Q
	IF $\overline{COUT}$	0	A5-19	A3-50	ABOVE SUBTRACT OPERATION
		0		A4-56	GENERATES A CARRY
	QSI	1	A4-42	A5-83	Q SHIFT INPUT = 2
	SFM	1	A3-74	A5-82	F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
	IF $\overline{COUT}$	1	A5-19	A3-50	ABOVE SUBTRACT DOES
				A4-56	NOT GENERATE A CARRY
	QSI	0	A4-42	A5-83	Q SHIFT INPUT = 0
	SFM	0	A3-74	A5-82	F TO SERIAL INPUT MODE
	STOF	1	A3-82	A5-84	LEFT SHIFT F
	NOTE: ALL DIV FUNCTIONS REQUIRE TWO CYCLES. CPU FREEZE DISABLES STF AND $\overline{STQ}$ DURING FIRST CYCLE ALLOWING TIME TO CHECK $\overline{COUT}$				
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
L1	SL1	1	A6-71	A4-6	ENABLE FUNCT LEFT SHIFT
	TBS2	1	A4-44	A5-54	SHIFT T-BUS LEFT 1
SKIP					
CTRI	IF ---		A6(INTERNAL)		RPT COUNTER=ALL 1'S
	---		A6(INTERNAL)		ENABLE SKIP FF
	---		A6(INTERNAL)		INCREMENT RPT COUNTER
	ELSE ---		A6(INTERNAL)		INCREMENT RPT COUNTER
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID,CONTINUED

ROM ADDRESS: 271
ROM MICROINSTRUCTION: 27773367 010 1111 11111 0110 1111 0111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
Q	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = Q
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
TBZ	IF TBZ	1	A5-25	A6-19	T-BUS(0-15)=0
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID•CONTINUED

ROM ADDRESS: 272
ROM MICROINSTRUCTION: 15562403 001 1011 01110 0101 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
XOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	EXCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID•CONTINUED

ROM ADDRESS: 273
ROM MICROINSTRUCTION: 75055377 111 1010 00101 1010 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
SUB	MC	Ø	A4-20	A5-12	
	FNØ	Ø	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	Ø	A4-5	A5-55	
	$\overline{\text{CIN}}$	Ø	A4-14	A5-41	
STORE					
Q	SQM	1	A3-70	A5-75	SET Q TO PARALLEL INPUT MODE
	STQ	1	A3-80	A5-73	Q = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 274
ROM MICROINSTRUCTION: 24567403 010 1001 01110 1111 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
Q	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = Q
	RBS2	1	A4-25	A5-62	
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
XOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	EXCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID,CONTINUED

ROM ADDRESS: 275
ROM MICROINSTRUCTION: 77767777 111 1111 11110 1111 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
SOV	---		A4(INTERNAL)		SET OVERFLOW LOGIC
	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID•CONTINUED

ROM ADDRESS: 276
ROM MICROINSTRUCTION: 37773057 011 1111 11111 0110 0010 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	Ø	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FNØ	Ø	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
R1	SR1	1	A6-72	A4-6	ENABLE FUNCT RIGHT SHIFT
	TBS1	1	A4-45	A5-53	SHIFT T-BUS RIGHT 1
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 277
ROM MICROINSTRUCTION: 17777403 001 1111 11111 1111 0000 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID,CONTINUED

ROM ADDRESS: 300
ROM MICROINSTRUCTION: 75056776 111 1010 00101 1101 1111 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---		A6(INTERNAL)		ENABLE SKIP FF
	REVERSE IF RSS IN SPECIAL FIELD				

DIVID,CONTINUED

ROM ADDRESS: 301
ROM MICROINSTRUCTION: 75376777 111 1010 11111 1101 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID,CONTINUED

ROM ADDRESS: 302
ROM MICROINSTRUCTION: 27777377 010 1111 11111 1110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
Q	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = Q
	RBS2	1	A4-25	A5-62	
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DIVID, CONTINUED

ROM ADDRESS: 303
ROM MICROINSTRUCTION: 74374775 111 1000 11111 1001 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S4	RSP4	1	A3-8	A5-11	S-BUS = SP4
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
F	SFM	1	A3-74	A5-82	SET F TO PARALLEL INPUT MODE
	STOF	1	A3-82	A5-84	F = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

DIVID•CONTINUED

ROM ADDRESS: 304
ROM MICROINSTRUCTION: 77114377 111 1110 01001 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN•	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
INC	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	CARRY IN TO ALU
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-112. DLD Instruction. The DLD (Double Load) instruction loads the contents of two consecutive memory locations (m and m+1) in the A- and B-registers, respectively. The following discussion gives the DLD operation.

a. ROM address 0310. This provides the legal entry point for the DLD instruction.

b. ROM address 0311. The address of the first word (memory location "m") is fetched and stored in the SP1-register by the GETAD subroutine in ROM locations 0362 through 0370.

c. ROM address 0312. The content of the SP1-register (memory location "m") is incremented ("m"+1) and placed in the SP2-register. This provides the memory address of the second word.

d. ROM address 0313. The address of the first word is placed in the M-register and a read/write cycle is started. Also, a check is made for A- and B-register addressing.

e. ROM address 0314. The content (the first operand) of the A- and B-register (if addressed), or the T-register is placed in the A-register.

f. ROM address 0315. The address of the second word is placed in the M-registe; and a read/write cycle is started. Also, a check is made for A- or B-register addressing.

g. ROM address 0316. The content (the second operand) of the A- or B-register (if addressed), or the T-register is placed in the B-register. The phase logic is set to the next phase.

h. ROM address 0317. The content of the P-register is placed on the S-bus, incremented by the function generator, and placed back in the P-register. This increments the P-register past the memory location containing the address of the first word.

4-113. The following pages provide ROM decoding and signal information for the execute phase of the DLD instruction.

DLD•EXECUTE PHASE

ROM ADDRESS: 310Ø
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 Ø111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-2Ø	A5-12	
	FNØ	Ø	A4-66	A5-5Ø	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

DLD•CONTINUED

ROM ADDRESS: 311
ROM MICROINSTRUCTION: 77207762 111 1110 10000 1111 1111 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	---		A4(INTERNAL)		CLEAR JSB FF
	JSB	1	A4-18	A2-69	LOAD ROM SAVE REGISTER
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	SRAR	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD SUBROUTINE ADR IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
GETAD	---				SET ROM ADDRESS 362 (PAGE 4-247)
SKIP					
NOP	---				NO OPERATION

DLD,CONTINUED

ROM ADDRESS: 312
ROM MICROINSTRUCTION: 75513377 111 1011 01001 0110 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
INC	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	CARRY IN TO ALU
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DLD,CONTINUED

ROM ADDRESS: 313
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

DLD,CONTINUED

ROM ADDRESS: 314
ROM MICROINSTRUCTION: 53777377 101 0111 11111 1110 1111 1111
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	$\overline{READ}$	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
A	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DLD,CONTINUED

ROM ADDRESS: 315
ROM MICROINSTRUCTION: 75370757 111 1010 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S2	RSP2	1	A3-7	A5-15	S-BUS = SP2
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

DLD,CONTINUED

ROM ADDRESS: 316
ROM MICROINSTRUCTION: 73776775 111 0111 11111 1101 1111 1101
CONDITION: DRTY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
B	STB	1	A3-63	A5-79	B = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE

(PAGE 4-30)

DLD•CONTINUED

ROM ADDRESS: 317
ROM MICROINSTRUCTION: 77314377 111 1110 11001 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(Ø-8)=P(Ø-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
INC	MC	Ø	A4-20	A5-12	
	FNØ	1	A4-66	A5-50	
	FN1	Ø	A4-3	A5-46	ARITHMETIC ADD
	FN2	Ø	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	Ø	A4-14	A5-41	CARRY IN TO ALU
STORE					
P	$\overline{\text{STP}}$	Ø	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-114. DST Instruction. The DST (Double Store) instruction stores the contents of the A- and B-registers in two consecutive memory locations, (m and m+1) respectively. The following discussion gives the DST operation.

a. ROM address 0320. This provides the legal entry point for the DST instruction.

b. ROM address 0321. The address for the first word (memory location "m") is fetched and stored in the SP1-register by the GETAD subroutine in ROM locations 0362 through 0370.

c. ROM address 0322. This microinstruction tests the first address (m) for a memory protect violation.

(1) The contents of the memory protect Fence (F-) register and the SP1-register (memory location "m") are placed on the R- and S-buses, respectively. The DEC microcode in the Function field causes the function generator to subtract the S-bus from the R-bus.

(2) If the result is negative (ALU15=1), memory location "m" is above the protected area of memory. The content of the SP1-register is placed in the M-register and a clear/write cycle is initiated. Since there is no memory protect violation, the next microinstruction (address 0323) is skipped.

(3) If the result is positive (ALU15=0), then location "m" is in the protected area of memory. The content of the SP1-register is placed in the M-register, but the initiation of a clear/write cycle is inhibited. The memory protect violation also causes the next microinstruction (address 0323) to be executed.

d. ROM address 0323. Read the A-register content (the first word) onto the R-bus, and read the R-bus onto the S-bus. Inclusive-OR the R- and S-buses, and store the result in the A- or B-register (if addressed); otherwise, no store will occur. Then perform an unconditional skip to address 0325.

e. ROM address 0324. Read the A-register content (the first word) onto the R-bus, and read the R-bus onto the S-bus. Store the S-bus contents in the T-register.

f. ROM address 0325. Read the content of the SP1-register (m) onto the S-bus, increment it (m+1), and store it in the SP3-register. Set the A- or B-Addressable FF if ALU bit 0 is a "0" or "1", respectively.

g. ROM address 0326. This microinstruction tests the second address (m+1) for a memory protect violation.

(1) The contents of the memory protect Fence (F-) register and the SP3-register (memory location "m"+1) are placed on the R- and S-buses, respectively. The DEC microcode in the Function field causes the function generator to subtract the S-bus from the R-bus.

(2) If the result is negative (ALU15=1), memory location "m"+1 is above the protected area of memory. The content of the SP3-register is placed in the M-register and a clear/write cycle is initiated. Since there is no memory protect violation, the next microinstruction (address 0327) is skipped.

(3) If the result is positive (ALU15=0), then location "m"+1 is in the protected area of memory. The content of the SP3-register is placed in the M-register, but the initiation of a clear/write cycle is inhibited. The memory protect violation also causes the next microinstruction (address 0327) is executed.

h. ROM address 0327. Read the B-register content (the second word) onto the R-bus, and read the R-bus onto the S-bus. Inclusive "or" the R- and S-buses, and store the result in the A- or B-register (if addressed); otherwise, no store will occur. Then perform an unconditional skip to address 0331.

i. ROM address 0330. Read the B-register content (the second word) onto the R-bus, and read the R-bus onto the S-bus. Store the S-bus contents in the T-register, and set the next phase.

j. ROM address 0331. The content of the P-register is placed on the S-bus, incremented by the function generator, and placed back in the P-register. This increments the P-register past the memory location containing the address of the first word.

4-115. The following pages provide ROM decoding and signal information for the execute phase of the DST instruction.

DST•EXECUTE PHASE

ROM ADDRESS: 320
ROM MICROINSTRUCTION: 77777577 111 1111 11111 1111 0111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
NOP	---				NO OPERATION
SPECIAL					
LEP	---		A2(INTERNAL)		SET LEP FF
SKIP					
NOP	---				NO OPERATION

DST, CONTINUED

ROM ADDRESS: 321
ROM MICROINSTRUCTION: 77207762 111 1110 10000 1111 1111 0010
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	---		A4(INTERNAL)		CLEAR JSB FF
	JSB	1	A4-18	A2-69	LOAD ROM SAVE REGISTER
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	SRAR	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD SUBROUTINE ADR IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
GETAD	---				SET ROM ADDRESS 362 (PAGE 4-247)
SKIP					
NOP	---				NO OPERATION

DST•CONTINUED

ROM ADDRESS: 322
ROM MICROINSTRUCTION: 35460712 011 1011 00110 0001 1100 1010
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
DEC	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	1'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
CW	CW	1	A6-73	A107-76	CLEAR-WRITE MEMORY
SKIP					
NMPV	IF MPC	0	A8-80	A6-13	MEMORY PROTECT DISABLED
	OR $\overline{\text{ALU 15}}$	1	A5-21	A6-77	NO MP VIOLATION
	AND $\overline{\text{AAFF}}$	1	A6-5	A6-5	A ADDRESSABLE FF CLEAR
	AND BAFF	0	A6-7	A6-7	B ADDRESSABLE FF CLEAR
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DST•CONTINUED

ROM ADDRESS: 323
ROM MICROINSTRUCTION: 02376376 000 0100 11111 1100 1111 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
AAB	IF $\overline{\text{AAFF}}$	0	A6-5	A3-52	A IS ADDRESSED
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF BAFF	1	A6-7	A3-43	B IS ADDRESSED
	STB	1	A3-63	A5-79	B = T-BUS
	IF $\overline{\text{AAFF}}$	1	A6-5	A3-52	A NOT ADDRESSED
	AND BAFF	0	A6-7	A3-43	B NOT ADDRESSED
	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---	A6(INTERNAL)			ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

DST,CONTINUED

ROM ADDRESS: 324
ROM MICROINSTRUCTION: 02371377 000 0100 11111 0010 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
A	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	RBS2	0	A4-25	A5-62	
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
T	SELT	1	A3-30	A107-74	T = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DST•CONTINUED

ROM ADDRESS: 325
ROM MICROINSTRUCTION: 75512557 111 1011 01001 0101 0110 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
INC	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	$\overline{FN3}$	1	A4-5	A5-55	
	$\overline{CIN}$	0	A4-14	A5-41	CARRY IN TO ALU
STORE					
S3	WSP3	1	A3-45	A5-69	SP3 = T-BUS
SPECIAL					
AAB	IF AAB	1	A5-26	A6-78	T-BUS)1-14)=0
	AND ALU0	0	A5-58	A6-79	ALU(0)=0
	---		A6(INTERNAL)		SET AAFF LOGIC
	IF AAB	1	A5-26	A6-78	T-BUS(1-15)=0
	AND ALU0	1	A5-58	A6-79	ALU(0)=1
	---		A6(INTERNAL)		SET BAFF LOGIC
	IF AAB	0	A5-26	A6-78	T-BUS(1-14) NOT=0
	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

DST•CONTINUED

ROM ADDRESS: 326
ROM MICROINSTRUCTION: 34460712 111 1001 00110 0001 1100 1010
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
F	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = F
	RBS2	1	A4-25	A5-62	
S-BUS					
S3	RSP3	1	A3-5	A5-13	S-BUS = SP3
FUNCTION					
DEC	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	1'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
CW	CW	1	A6-73	A107-76	CLEAR-WRITE MEMORY
SKIP					
NMPV	IF MPC	0	A8-80	A6-13	MEMORY PROTECT DISABLED
	OR $\overline{\text{ALU 15}}$	1	A5-21	A6-77	NO MP VIOLATION
	AND $\overline{\text{AAFF}}$	1	A6-5	A6-5	A ADDRESSABLE FF CLEAR
	AND BAFF	0	A6-7	A6-7	B ADDRESSABLE FF CLEAR
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION
	REVERSE IF RSS IN SPECIAL FIELD				

DST•CONTINUED

ROM ADDRESS: 327
ROM MICROINSTRUCTION: 12376376 001 0100 11111 1100 1111 1110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
AAB	IF $\overline{\text{AAFF}}$	0	A6-5	A3-52	A IS ADDRESSED
	SAM	1	A3-67	A5-77	SET A TO PARALLEL INPUT MODE
	STA	1	A3-64	A5-81	A = T-BUS
	IF BAFF	1	A6-7	A3-43	B IS ADDRESSED
	STB	1	A3-63	A5-79	B = T-BUS
	IF $\overline{\text{AAFF}}$	1	A6-5	A3-52	A NOT ADDRESSED
	AND BAFF	0	A6-7	A3-43	B NOT ADDRESSED
	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
UNC	---		A6(INTERNAL)		ENABLE SKIP FF

REVERSE IF RSS IN SPECIAL FIELD

DST•CONTINUED

ROM ADDRESS: 330
ROM MICROINSTRUCTION: 12371375 001 0100 11111 0010 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
B	$\overline{\text{RBE}}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	1	A4-15	A5-64	R-BUS = B
	RBS2	0	A4-25	A5-62	
S-BUS					
RRS	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
T	SELT	1	A3-30	A107-74	T = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

DST, CONTINUED

ROM ADDRESS: 331
ROM MICROINSTRUCTION: 77114377 111 1110 01001 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPL0	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
INC	MC	0	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	ARITHMETIC ADD
	FN2	0	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	CARRY IN TO ALU
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-116. OPGET Subroutine. The OPGET (Get Operand) subroutine is used during execution of the MPY and DIVID instructions to obtain the multiplier, or divisor, at the memory address fetched by the GETAD subroutine and place it in the SP2-register. The operation of the OPGET subroutine is as follows:

a. ROM address 0232. The content of the SP1-register (the memory address fetched by the GETAD subroutine) is transferred to the M-register, a read/write cycle is started, and A- or B-register addressing is checked.

b. ROM address 0233. The A-, B-, or T-register content (multiplier or divisor) is placed in the SP2-register.

c. ROM address 0234. A jump to the PDEC subroutine is executed if any interrupts are pending or a panel halt is detected.

d. ROM address 0235. A jump to the calling routine is executed (target address is either 0213 or 0253).

4-117. The following pages provide ROM decoding and signal information for the execution of the OPGET subroutine.

OPGET•EAG SUBROUTINE

ROM ADDRESS: 232
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

OPGET•CONTINUED

ROM ADDRESS: 233
ROM MICROINSTRUCTION: 73773377 111 0111 11111 0110 1111 1111
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S2	WSP2	1	A3-56	A5-67	SP2 = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

OPGET, CONTINUED

ROM ADDRESS: 234
ROM MICROINSTRUCTION: 77247411 111 1110 10100 1111 0000 1001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CJMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CJMP}}$	0	A4-62	A1-60	CONDITIONAL ROM JUMP
	IF INT	1	A7-45	A1-22	I/O INTERRUPT
	OR HALT		A1 (INTERNAL)		DISPLAY PANEL HALT
	$\overline{\text{SRAR}}$	0	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
	IF NOT HALT, INTERRUPT, OR SINGLE CYCLE, NO OPERATION				
STORE					
NOP	---				NO OPERATION
SPECIAL					
PDEC	---				SET ROM ADDRESS 011 (PAGE 4-254)
SKIP					
NOP	---				NO OPERATION

OPGET•CONTINUED

ROM ADDRESS: 235
ROM MICROINSTRUCTION: 77657777 111 1111 1010 1111 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
RSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	RSAV	1	A4-17	A1-71 A2-41	READ SAVE REG TO RAR
STORE					
NOP	---				NO OPERATION
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

4-118. GETAD Subroutine. The GETAD (Get Address) subroutine is used during execution of the MPY, DIVID, DLD, and DST instructions to obtain the multiplier address, divisor address, or first word address and place it in the SP1-register. The P-register supplies the first memory address, and the contents of that location are examined for indirect addressing. If the address obtained is indirect, the subroutine continues to fetch each indirect address location until a direct address is obtained. Once obtained, the address is stored in the SP1-register. The operation of the GETAD subroutine is as follows:

a. The P-register content is transferred to the M-register, a read/write cycle is started, and A- or B-register addressing is checked.

b. The next microinstruction to be executed is the ONEMO entry point. The ONEMO portion of the microroutine examines the contents of the memory location for indirect addressing. If the address is indirect, the IND portion of the microroutine is entered. The contents of the A-, B-, and T-register is

placed in the SP1-register. The next microinstruction is skipped if the address is not indirect (ALU bit 15 = 0).

c. If the fetched address is a direct address, the content of the SP1-register is examined for A- or B-register addressing and the corresponding addressable FF is set (if addressed). Also, a return-from-ROM-subroutine is executed.

d. If the fetched address is an indirect address, the next microinstruction to be executed is the IND entry point. The IND portion of the microroutine allows any pending interrupt or panel halt condition to be processed, and fetches the contents of the location specified by the indirect address in the ONEMO portion of the subroutine. A jump is executed to the ONEMO portion of the subroutine so that the fetched address can be examined for indirect addressing.

e. The first microinstruction of the IND portion contains a CJMP microcode in the Function field which allows a jump to PDEC entry point if an interrupt or panel halt condition is present. PDEC decrements the P-register so that the data in the registers lost as a result of the interrupt can be resotred by executing the user EAG instruction again.

f. The second microinstruction transfers the content of the SP1-register to the M-register, starts a read/write cycle, and checks for A- or B-register addressing.

g. The last microinstruction causes a jump to the ONEMO entry point. Steps "b" through "g" are repeated until a direct address is obtained.

4-119. The following pages provide ROM decoding and signal information for the execution of the GETAD subroutine.

GETAD,EAG SUBROUTINE

ROM ADDRESS: 362
ROM MICROINSTRUCTION: 77370757 111 1110 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

GETAD•CONTINUED

ROM ADDRESS: 363
ROM MICROINSTRUCTION: 53773403 101 0111 11111 0111 0000 0010
CONDITION: DTRY

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
AAB	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	1	A3-20	A4-11	S-BUS DECODED COND
	$\overline{RBE}$	1	A4-22	A5-5	DISABLE R-BUS
	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	AND COND	0	A3-20	A4-11	NOT S-BUS DECODED COND
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	$\overline{RBE}$	0	A4-22	A5-5	ENABLE R-BUS
	RBS1	0	A4-15	A5-64	R-BUS = A
	OR RBS1	1	A4-15	A5-64	R-BUS = B
S-BUS					
COND	IF $\overline{ABF}$	1	A3-66	A4-21	A OR B NOT ADDRESSED
	SELT	1	A3-30	A107-74	S-BUS = T
	READ	1	A3-28	A107-72	
	IF $\overline{ABF}$	0	A3-66	A4-21	A OR B IS ADDRESSED
	RRSB	1	A3-24	A5-36	S-BUS = R-BUS
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
S1	WSP1	1	A3-55	A5-65	SP1 - T-BUS
SPECIAL					
RSS	---		46(INTERNAL)		REVERSE SKIP FIELD SENSE
SKIP					
NEG	IF ALU15	1	A5-21	A6-11	ALU OUTPUT IS NEGATIVE
	---		A6(INTERNAL)		ENABLE SKIP FF
	ELSE ---				NO OPERATION

REVERSE IF RSS IN SPECIAL FIELD

GETAD, CONTINUED

ROM ADDRESS: 364
ROM MICROINSTRUCTION: 77227766 111 1110 10010 1111 1111 0110
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
IND	---				SET ROM ADDRESS 366 (PAGE 4-251)
SKIP					
NOP	---				NO OPERATION

GETAD•CONTINUED

ROM ADDRESS: 365
ROM MICROINSTRUCTION: 75657557 111 1011 10101 1111 0110 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
RSB	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	RSAV	1	A4-17	A1-71 A2-41	READ SAVE REG TO RAR
STORE					
NOP	---				NO OPERATION
SPECIAL					
AAB	IF AAB	1	A5-26	A6-78	T-BUS)1-14)=0
	AND ALU0	0	A5-58	A6-79	ALU(0)=0
	---		A6(INTERNAL)		SET AAFF LOGIC
	IF AAB	1	A5-26	A6-78	T-BUS(1-15)=0
	AND ALU0	1	A5-58	A6-79	ALU(0)=1
	---		A6(INTERNAL)		SET BAFF LOGIC
	IF AAB	0	A5-26	A6-78	T-BUS(1-14) NOT=0
	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION

GETAD•CONTINUED

ROM ADDRESS: 366
ROM MICROINSTRUCTION: 77247411 111 1110 10100 1111 0000 1001
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
CJMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{CJMP}}$	0	A4-62	A1-60	CONDITIONAL ROM JUMP
	IF INT	1	A7-45	A1-22	I/O INTERRUPT
	OR HALT		A1(INTERNAL)		DISPLAY PANEL HALT
	$\overline{\text{SRAR}}$	0	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
	IF NOT HALT, INTERRUPT, OR SINGLE CYCLE, NO OPERATION				
STORE					
NOP	---				NO OPERATION
SPECIAL					
PDEC	---				SET ROM ADDRESS 011 (PAGE 4-254)
SKIP					
NOP	---				NO OPERATION

GETAD•CONTINUED

ROM ADDRESS: 367
ROM MICROINSTRUCTION: 75770757 111 1011 11111 0001 1110 1111
CONDITION: T6

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
S1	RSP1	1	A3-10	A5-17	S-BUS = SP1
FUNCTION					
IOR	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
STORE					
M	SELM	1	A3-22	A107-66	M = S-BUS
	STORE	1	A3-53	A107-73	
SPECIAL					
RW	RW	1	A6-74	A107-75	READ-WRITE MEMORY ENABLE ABFF LOGIC
SKIP					
NOP	---				NO OPERATION

GETAD•CONTINUED

ROM ADDRESS: 370
ROM MICROINSTRUCTION: 77227763 111 1110 10010 1111 1111 0011
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
NOP	---				NO OPERATION
FUNCTION					
JMP	MC	1	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	INCLUSIVE OR
	FN2	1	A4-4	A5-56	
	FN3	1	A4-5	A5-55	
	$\overline{\text{JMPS}}$	0	A4-46	A1-73	ROM JUMP
	$\overline{\text{SRAR}}$	1	A1-61	A2-60	PARALLEL ENABLE RAR
	RJMP	1	A1-75	A2-56	LOAD JUMP-TO ADDRESS IN RAR (SEE SPECIAL FIELD)
	$\overline{\text{JMPF}}$	0	A4-49	A3-36	JMP FUNCTION
	ENSS	0	A3-61	A6-15	DISABLE SPECIAL AND SKIP
STORE					
NOP	---				NO OPERATION
SPECIAL					
ONEMO	---				SET ROM ADDRESS 363 (PAGE 4-248)
SKIP					
NOP	---				NO OPERATION

4-120. PDEC Subroutine. The PDEC subroutine is used to decrement the P-register and to set the next phase of operation. The PDEC subroutine is the jump target for the CJMP microcode in the Function field. The CJMP microcode appears in the OPGET and GETAD subroutines to allow pending interrupts or a panel halt to be processed. Since the data present in various registers will be lost when the interrupt is processed, the P-register is decremented to allow the interrupted instruction to be executed again, after the interrupt is processed. The operation of the PDEC subroutine is as follows:

a. ROM address 0011. The content of the P-register is placed on the S-bus. The SUB microcode in the Function field activates the arithmetic function of the function generator which performs an R-bus minus S-bus minus 1 operation. However, the SUB microcode also generates a false CIN ("not" Carry In) signal which results in an overall function of the R-bus (all "0's") minus the S-bus (P-register content). The result is stored back into the P-register, and the phase logic is set to the next phase.

b. ROM address 0012. The new P-register content is placed on the S-bus. The NOR microcode in the Function field activates the logic function of the function generator which performs a logical NOR of the R-bus (all "0's") and the S-bus (P-register content). The result is stored back into the P-register.

4-121. The following pages provide ROM decoding and signal information for the execution of the PDEC subroutine.

PDEC, INTERRUPT DURING EAG

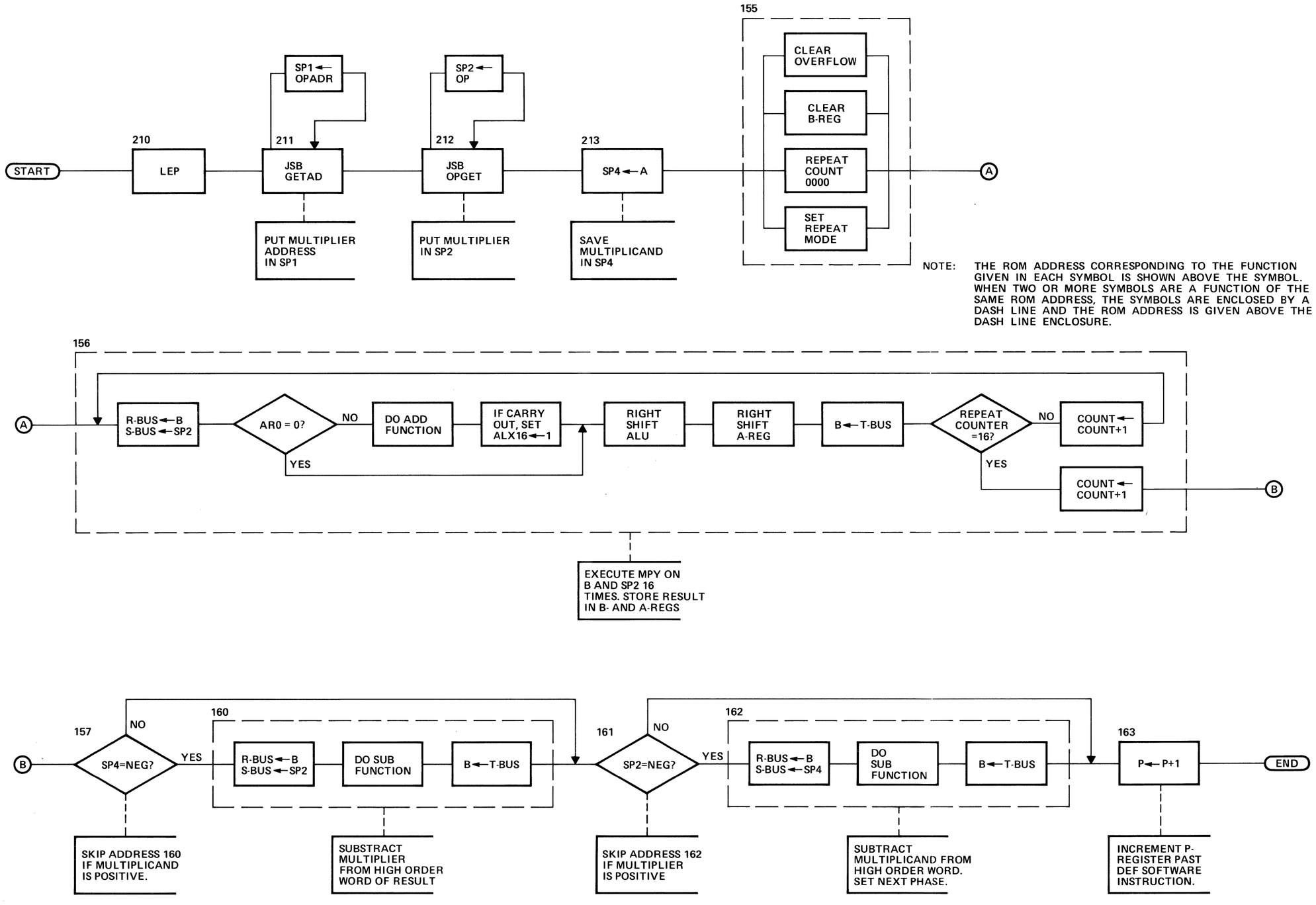
ROM ADDRESS: 011
ROM MICROINSTRUCTION: 77054375 111 1110 00101 1000 1111 1101
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
SUB	MC	0	A4-20	A5-12	
	FN0	0	A4-66	A5-50	
	FN1	1	A4-3	A5-46	2'S COMPLEMENT SUBTRACT
	FN2	1	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
	$\overline{\text{CIN}}$	0	A4-14	A5-41	
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
EOP	EOP	1	A2-65	A1-46	END OF PHASE (PAGE 4-30)

PDEC•CONTINUED

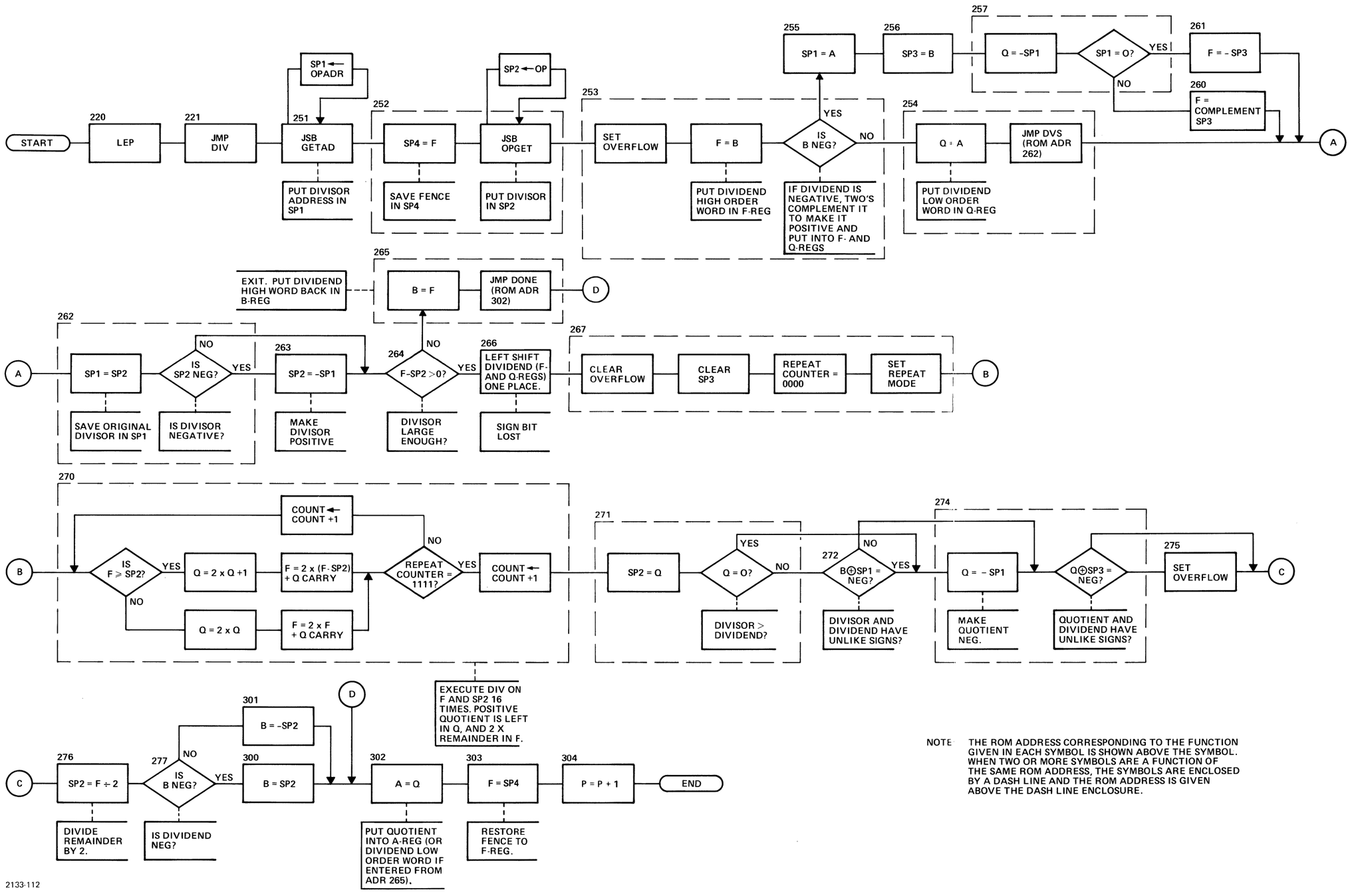
ROM ADDRESS: 012
ROM MICROINSTRUCTION: 77154377 111 1110 01101 1000 1111 1111
CONDITION: NONE

FIELD	SIGNALS	LEVEL	SOURCE	DESTIN.	COMMENTS
R-BUS					
NOP	---				NO OPERATION
S-BUS					
P	RPLO	1	A3-6	A5-57	S-BUS(0-8)=P(0-8)
	RP9	1	A3-21	A5-27	S-BUS(9)=P(9)
	RPHI	1	A3-23	A5-28	S-BUS(10-15)=P(10-15)
FUNCTION					
NOR	MC	1	A4-20	A5-12	
	FN0	1	A4-66	A5-50	
	FN1	0	A4-3	A5-46	NEGATIVE OR
	FN2	0	A4-4	A5-56	
	FN3	0	A4-5	A5-55	
STORE					
P	$\overline{\text{STP}}$	0	A3-64	A5-63	P = T-BUS
SPECIAL					
NOP	---				NO OPERATION
SKIP					
NOP	---				NO OPERATION



NOTE: THE ROM ADDRESS CORRESPONDING TO THE FUNCTION GIVEN IN EACH SYMBOL IS SHOWN ABOVE THE SYMBOL. WHEN TWO OR MORE SYMBOLS ARE A FUNCTION OF THE SAME ROM ADDRESS, THE SYMBOLS ARE ENCLOSED BY A DASH LINE AND THE ROM ADDRESS IS GIVEN ABOVE THE DASH LINE ENCLOSURE.

Figure 4-12. MULT Operation Flowchart



NOTE THE ROM ADDRESS CORRESPONDING TO THE FUNCTION GIVEN IN EACH SYMBOL IS SHOWN ABOVE THE SYMBOL. WHEN TWO OR MORE SYMBOLS ARE A FUNCTION OF THE SAME ROM ADDRESS, THE SYMBOLS ARE ENCLOSED BY A DASH LINE AND THE ROM ADDRESS IS GIVEN ABOVE THE DASH LINE ENCLOSURE.

Figure 4-13. DIV Operation Flowchart

4-122. MEMORY SECTION SERVICING.

4-123. GENERAL.

4-124. The core memory in the computer is of three-wire design, with an X-drive line, Y-drive line, and inhibit-sense line strung through each core. A current reversing capability for the X-drive line permits two 4K (4,096 word) modules to share common lines and operate in tandem as a single 8K (8,192 word) core stack. The computer mainframe can contain from one to four core stacks (a maximum of 32,768 words).

4-125. Figure 3-2 is an overall block diagram of the computer, including the memory section. When a word is to be read from memory, the address is placed in the M-register. The address is decoded by the address decoding gates on the memory address decoder and X-Y driver/switch cards, which select the appropriate driver and switch circuits. Current flows from the driver to the switch, or vice versa, and the cores of the selected word are set to the zero state. For each core that contained logic 1, a sense amplifier detects an output from the core. The sense amplifier sets the corresponding position of the T-register to logic 1 via the multiplexer.

4-126. The word read from memory is stored in the T-register. The word read out must then be restored in the memory location from which is was acquired. To do this, the memory section attempts to store logic 1 in every bit position of the word. However, the inhibit driver for each bit of the word senses the corresponding bit in the T-register, and if the bit is logic 0 the inhibit driver prevents the writing of logic 1 in the appropriate bit position of the selected word location in memory. By this means the word read from memory is restored in the original location.

4-127. The operation described above is also performed when placing a new word into a memory location, except that the word read out of memory is not stored in the T-register. Instead, the new word is placed in the T-register via the S-bus lines and the multiplexer. The new word is then stored in memory rather than the original word. (Refer to paragraph 3-487 for a more detailed account of memory operation). When troubleshooting the memory section, it is necessary to determine which of the following types of faults exist:

a. Addressing fault.
b. Read fault.
c. Write fault.

4-128. The type of fault can be determined from the symptoms observed, from running the diagnostic programs, and by using operator panel controls to store and read test words. A small test program can be used (refer to paragraph 4-134) as a further means of determining the type of fault.

4-129. TEST PROCEDURE.

4-130. The following paragraphs provide servicing information for the 2100A Computer memory and associated circuits. Table 4-10 is a troubleshooting table listing trouble symptoms and the circuit cards wherein the probable cause of the trouble lies. Figure 4-14 is a servicing diagram of a 32K memory section. For memory sizes less than 32K, the nonexistent core stack or stacks and associated circuitry can be ignored.

4-131. Figures 4-15 and 4-16 are memory addressing indexes which provide, for any memory address, the driver/switch card number and enabling signal, the memory address decoder enabling signals, and the combination of driver outputs and switch grounds required to read from and write into that address. Figure 4-15 applies to all 8K memory modules. If the memory module used in the computer has a 4K core stack (A103 when memory size is 4K and A102 when memory size is 12K), figure 4-16 provides the addressing information for that (4K) module. Figures 4-17 through 4-59 provide timing and waveshape details for a properly functioning memory section. Figures 4-18 through 4-59 are examples of actual oscilloscope observations of the memory timing signals.

4-132. The following diagnostic test programs are used to test the operation of the computer memory circuits:

a. Low Memory Address Test.
b. High Memory Address Test.
c. Low Memory Pattern Test.
d. High Memory Pattern Test.

4-133. Refer to paragraph 4-14 in this section and the corresponding diagnostic program procedure in the Manual of Diagnostics for diagnostic operating procedures.

4-134. In addition to the diagnostic test programs, maintenance switches on the computer operator panel allow the operator to load all memory locations with any desired 16-bit test word. The procedure for doing this is as follows:

Note: If the loader locations in memory are to be loaded with the test word, press the LOADER ENABLE switch; otherwise, ensure that the LOADER ENABLE switch indicator is not lit.

a. Ensure that the computer is in the halt mode.

b. Remove the computer front panel.

c. Press the operator panel MEMORY DATA switch and load the desired test word in the display register.

d. Set the memory test switch (see figure 1-11, item 10) in the inhibit position and the operation loop switch (see figure 1-11, item 11) in the loop position.

e. Press and hold the operator panel INCREMENT M switch for about one second.

4-135. If the memory section is functioning properly, all locations in memory now contain the 16-bit test word specified in step "c" of paragraph 4-134.

4-136. The test word will continue to be stored (written) throughout memory, or loaded into the A-register from memory, until the INCREMENT M switch is released. To change the test word, release the INCREMENT M switch and repeat steps "c" thru "e" of paragraph 4-134.

4-137. During these test operations, oscilloscope examination of waveforms will serve as an aid in determining the type of fault. It should be noted that when an addressing fault exists, it affects both read and write operations. Therefore, if a word is written in a given location and then read back, operation may appear normal because the word will have been written in and read from the wrong location.

4-138. ADDRESSING CIRCUITS.

4-139. DESCRIPTION. The selection of a particular word location in the core stack assembly is a function of the following cards:

a. Data Control Card A107.

b. X-Y Driver/Switch Cards A101, A104, A109, and A112.

c. Core Stack Sense Amplifier Cards A102, A103, A110, and A111.

4-140. Data Control Card. The data control card procedures timing and control signals (MRTY, MWTY, MIT, XT1, XT2, MSG, and MST) for the memory circuits. It also contains the M-register and T-register circuits and the memory module decoding circuit.

4-141. X-Y Driver/Switch Cards. The X-Y driver/switch cards decode the memory address bits MR0 through MR11. When decoded, these signals, along with the timing signals MWTY, MRTY, MIT, XT1, and XT2, and the module address signals MOD0/1 through MOD6/7 select the proper driver/switch circuits. The driver/switch circuits provide X and Y drive-line currents at the proper time to read data from and write data into the selected memory location.

4-142. Core Stack/Sense Amplifier Cards. The core stack/sense amplifier cards contain the memory core stack diode matrixes which direct the current along the proper X- and Y-lines through the core stack.

4-143. TEST PROCEDURE. The following general-purpose procedure may be used to troubleshoot a memory addressing problem where no parity error has been indicated.

a. Using the method described in paragraph 4-134 load all locations in memory (except the protected area) with logic 0's.

b. Press and release the HALT switch.

c. Address location 000003 and load it with 172001 (STA, I 01).

d. Address location 000004 and load it with 002004 (INA).

e. Address location 000005 and load it with 006004 (INB).

f. Address location 000006 and load it with 026003 (JMP, 03).

g. Address the A-register and load it with 000007.

h. Address the B-register and load it with 000007.

i. Set the M- and P-registers to location 000003.

j. Press the EXTERNAL PRESET, INTERNAL PRESET, and RUN switches. Let the machine run for approximately 30 seconds.

k. Press the HALT switch.

4-144. This program places the number of the location in the location (i.e., location 000012 will contain 000012, location 000013 will contain 000013, etc.) until the program itself is encountered. At this time the program halts and the M-register contains 177777, the P-register contains 000003, locations 000000 and 000001 contain 177777, variable data will be contained in location 000002, and the remainder of the program will be contained in locations 000003 through 000006.

4-145. After the above program has been entered and run, enter and run the following program which checks the first program for the faulty addressing:

a. Address location 000003 and load it with 006004 (INB).

b. Address location 000004 and load it with 162001 (LDA, I, 01).

c. Address location 00005 and load it with 052001 (CPA, 01).

d. Address location 000006 and load it with 102003 (HLT, 03).

e. Address the A-register and load it with 000010.

f. Address the B-register and load it with 000010.

g. Set the M- and P-registers to location 000004.

h. Press the EXTERNAL PRESET, INTERNAL PRESET, and RUN switches. The HALT indicator will light when the program has checked every location in memory (except the upper 77 octal LOADER locations) or an error condition is sensed.

4-146. This program compares the data loaded into the A-register from memory with the reference data in the B-register. When the data in these two registers does not compare, the program is halted with 102003 displayed in the DISPLAY REGISTER. At this time the location from which the bad data was obtained will be shown in the B-register. If the program ran properly and there was no addressing errors encountered, the B-register will contain 77 less than the number of the highest memory location available in the machine. (The 77 locations not tested are the protected LOADER locations.) The M-, P-, and A-registers will contain 000007, 000010, and 000000, respectively.

4-147. A further location-by-location check should now be made to ascertain whether the error location indicated in the B-register is the only location with an error or the complete module or stack is not being addressed properly. Also, all bits of the bad location should be checked by writing "1's" and "0's" into the cores to make sure the error is not a bit error. Tables 4-10 through 4-14 and figures 4-14, 4-15, and 4-16 will aid in locating the faulty circuit card.

4-148. READ AND WRITE CIRCUITS.

4-149. DESCRIPTION. The read and write circuits control data bits as they are stored in, and removed from, the addressed core memory location. These functions are performed by the following circuit cards:

a. Data Control Card A107.

b. Core Stack/Sense Amplifier Cards A102, A103, A110, and A111.

c. Inhibit Driver Cards A105 and A108.

d. Inhibit Load Card A106.

4-150. Data Control Card. The data control card produces timing, control, and data signals (MSG, MST, and TR0 through TR16) for the memory section. This card also contains the memory data transfer register (T-register).

4-151. Core Stack/Sense Amplifier Cards. The circuits on these cards transfer data from the addressed memory location to the T-register on the data control card. The sense amplifier cards each contain an 8K core stack assembly and 17 or 34 amplifier circuits (17 for each 4K module) which sense, rectify, and amplify the pulses from the 17 ferrite cores of the addressed memory location. A pulse is produced when a core storing a logic 1 is switched to the logic 0 state during memory read time (MRTY).

4-152. Inhibit Driver and Inhibit Driver Load Cards. The inhibit driver cards each contain 68 inhibit driver circuits (17 for each module of a 16K memory configuration) which sense the bit-positions of the T-register. For each bit position containing logic 0, an inhibit driver circuit is turned on by the MIT (memory inhibit time) pulse to prevent the writing of logic 1 in the corresponding bit position of the addressed memory location during memory write time (MWTY). The inhibit driver load card provides a constant current source for the inhibit drive circuits and consists of R-C networks and a temperature sensitive resistor for sensing the temperature of the memory section of the computer. This resistor controls the voltage output of the +20 volts memory supply and assures that for a given temperature within the memory area the optimum operating voltage will be applied to the memory circuits.

4-153. TEST PROCEDURE. Troubleshooting the memory read and write circuits can be accomplished by exchanging circuit cards. After determining which core stack is associated with the failure, the circuit cards associated with that core stack can be exchanged, one card at a time, with the circuit cards associated with another core stack (if the computer has a memory configuration greater than 16K, or spare circuit cards are available). Each time a circuit card is exchanged, a test of the failing core stack locations must be made to ascertain if the trouble indication still exists, or has moved to the core stack locations with which the card was exchanged. If the trouble indication moves or disappears, it can be presumed that the circuit card originally in the card position was faulty. Troubleshooting the memory read and write circuits can also be accomplished by observing signal waveforms produced by the memory circuits. The following procedure may be used:

a. Using the method described in paragraph 4-134, load all locations in memory (except the protected area) with logic "1's".

b. With an oscilloscope, examine the input and outputs of the circuits affecting the failing bit position or positions while holding down the INCREMENT M switches on the operator panel and compare these signals with the waveforms shown in figures 4-17 through 4-59. If these signals do not come within reasonable tolerances of comparison, the most probable cause of trouble is in the output circuit of the signal currently being examined.

4-154. An alternate method to the above is listed below.

a. For write signal examination:

(1) Address the A-register and load it with 177777 (or any other test pattern).

(2) Address a location in memory (not the suspected location) and load it with 072XXX (STA, X, where X is the suspected location).

(3) Address the next sequential location and load it with 026YYY (JMP, Y, where Y is the location of the STA instruction in substep (2).

(4) Set the M- and P-registers to the location of the STA instruction in substep (2).

(5) Press the RUN switch and examine the questionable signals.

b. For read signal examination:

(1) Address the suspected location and load it with 177777 (or any other test pattern).

(2) Address a location in memory (not the suspected location) and load it with 062XXX (LDA, X, where X is the suspected location).

(3) Address the next sequential location and load it with 026YYY (JMP, Y, where Y is the location of the LDA instruction in substep (2).

(4) Set the M- and P-registers to the location of the LDA instruction in substep (2).

(5) Press the RUN switch and examine the questionable signals.

4-155. The waveforms shown in figures 4-18 through 4-59 were observed while the computer was in the halt mode or the run mode using the above listed test procedures. The oscilloscope settings were as follows, unless otherwise specified:

a. Triggering mode: internal ACF
b. Triggering source: trace B
c. Time/cm: 0.05 us
d. Magnification: X1
e. Slope: +
f. Sync: trace B
g. Trace mode: normal
h. Coupling: DC
i. Volts/cm: 0.2
j. Voltage probe: 10:1 attenuation
k. Current probe: 1mv=1ma

Table 4-10. 2100A Memory Troubleshooting

TROUBLE SYMPTOM	PROBABLE CAUSE OR CAUSES			
	SENSE AMPLIFIER	INHIBIT DRIVER	DRIVER/SWITCH	DATA CONTROL
BIT ERROR:				
MOD 0/1 ONLY	A103	A105	– – –	– – –
MOD 2/3 ONLY	A102	A105	– – –	– – –
MOD 0/1/2/3	– – –	A105	– – –	– – –
MOD 4/5 ONLY	A110	A108	– – –	– – –
MOD 6/7 ONLY	A111	A108	– – –	– – –
MOD 4/5/6/7		A108	– – –	– – –
MOD 0 THRU 7		LOAD CARD A106	– – –	A107 T-REGISTER
LOCATION ERROR:				
MOD 0/1 ONLY	A103	– – –	A104	A107 MODULE DECODER
MOD 2/3 ONLY	A102	– – –	A101	A107 MODULE DECODER
MOD 4/5 ONLY	A110	– – –	A109	A107 MODULE DECODER
MOD 6/7 ONLY	A111	– – –	A112	A107 MODULE DECODER
ALL MODULES				A107 MODULE DECODER MODULE SELECTION GATES
MODULE ERROR:				
MOD 0/2/4/6 ONLY	– – –	– – –	– – –	A107 MODULE SELECTION GATES
MOD 1/3/5/7 ONLY	– – –	– – –	– – –	A107 MODULE SELECTION GATES
BIT ERROR IN ONLY ONE LOCATION	CORE STACK			

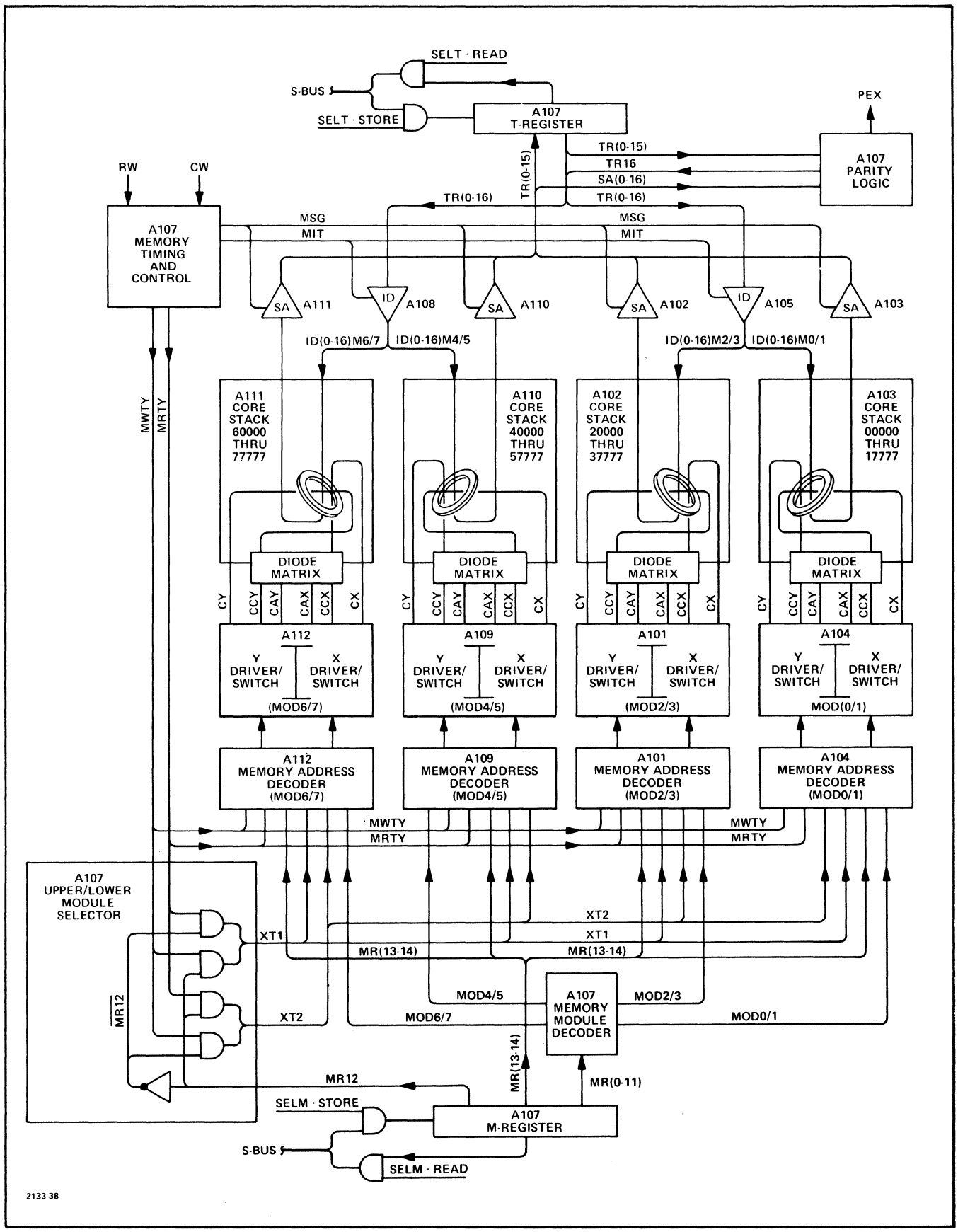
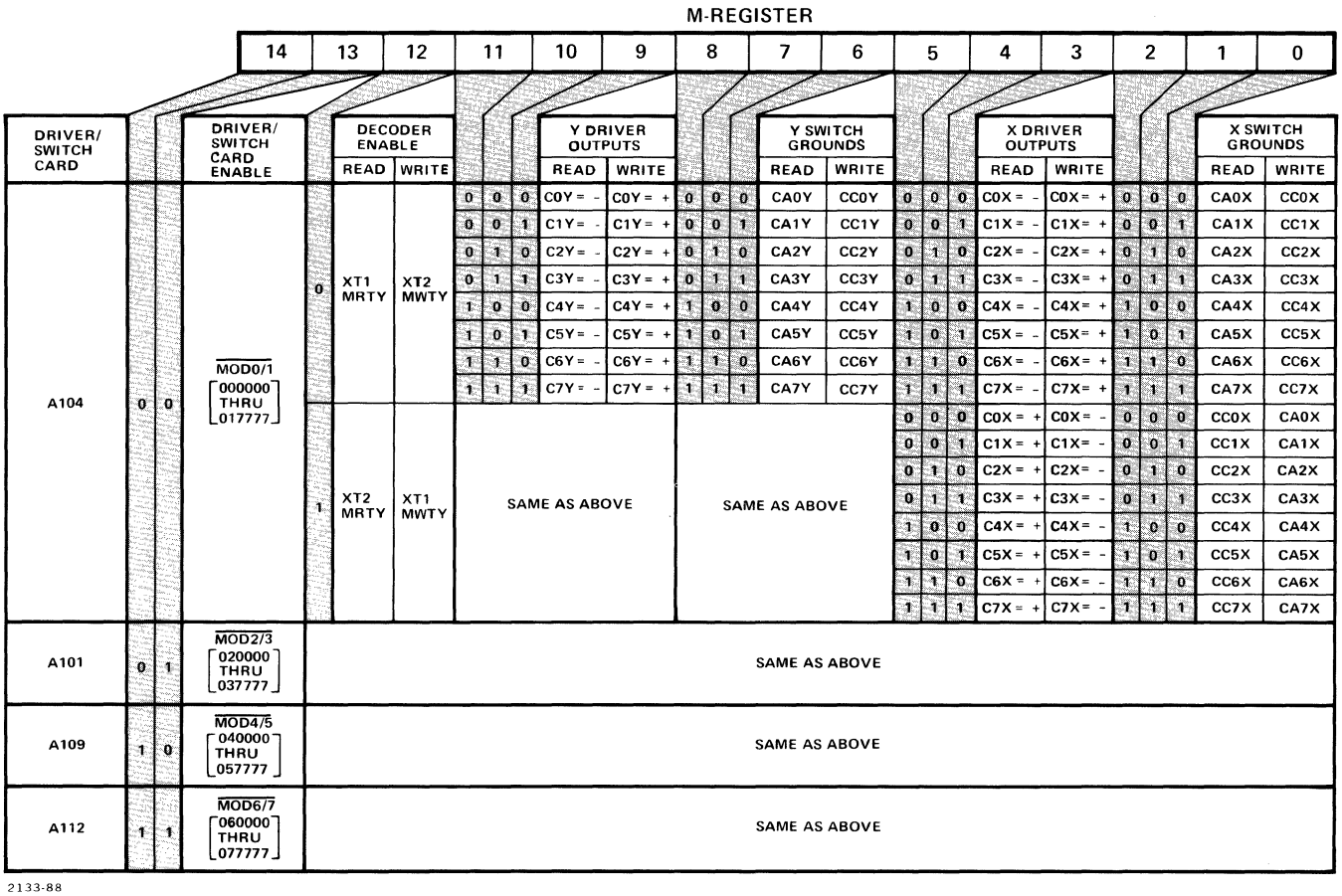
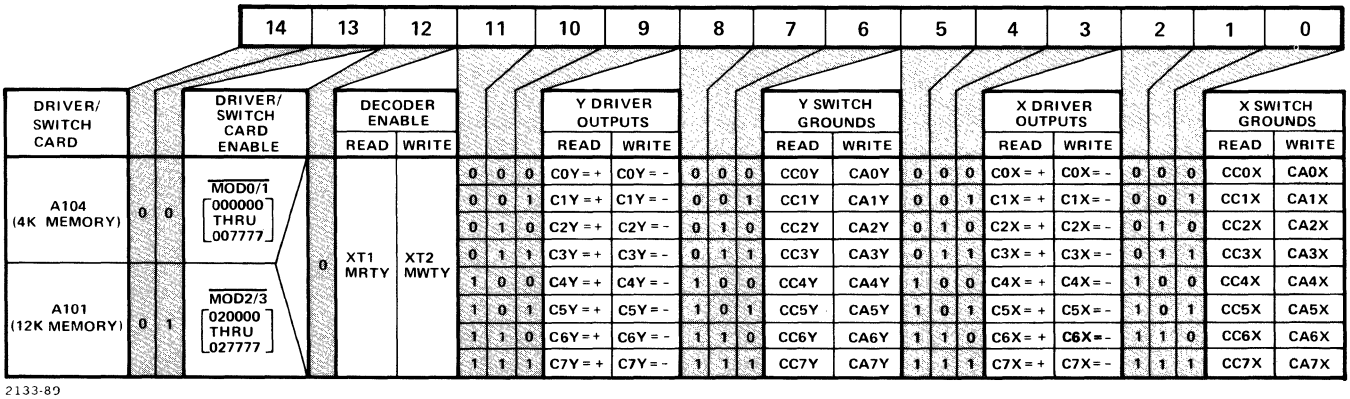


Figure 4-14. Memory Section Servicing Diagram



2133-88

Figure 4-15. Memory Addressing Index (8K Modules)



2133-89

Figure 4-16. Memory Addressing Index (4K Modules)

Table 4-11. X-Y Driver Switch Circuit Functions

					M-REGISTER BITS											
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					NOT USED	CORE STACK		UPPER OR LOWER MODULE	Y-DRIVE LINE SELECTION						X-DRIVE LINE SELECTION					
									MSD			LSD			MSD			LSD		
CARD	MODULE	ADDRESSES	MODES	TIMING SIGNALS	CONTROL SIGNAL				DECODER		DRIVERS	DECODER		DRIVERS	DECODER		DRIVERS	DECODER		DRIVERS
A104	4K	000000 THRU 007777	READ	XT1, MRTY	$\overline{MOD0/1}$				U24		U9, U11, U13, U15	U22		U2, U4, U14, U16	U18		U1, U3, U5, U7	U20		U6, U8, U10, U12
			WRITE	XT2, MWTY	$\overline{MOD0/1}$				U23		U9, U11, U13, U15	U21		U2, U4 U14, U16	U17		U1, U3, U5, U7	U19		U6, U8, U10, U12
	8K	010000 THRU 017777	READ	XT2, MRTY	$\overline{MOD0/1}$				U24		U9, U11, U13, U15	U22		U2, U4 U14, U16	U17		U1, U3, U5, U7	U20		U6, U8, U10, U12
			WRITE	XT1, MWTY	$\overline{MOD0/1}$				U23		U9, U11, U13, U15	U21		U2, U4, U14, U16	U18		U1, U3, U5, U7	U19		U6, U8, U10, U12
A101	12K	020000 THRU 027777	SAME AS ABOVE	SAME AS ABOVE	$\overline{MOD2/3}$				SAME AS ABOVE											
	16K	030000 THRU 037777																		
A109	20K	040000 THRU 047777	SAME AS ABOVE	SAME AS ABOVE	$\overline{MOD4/5}$				SAME AS ABOVE											
	24K	050000 THRU 057777																		
A112	28K	060000 THRU 067777	SAME AS ABOVE	SAME AS ABOVE	$\overline{MOD6/7}$				SAME AS ABOVE											
	32K	070000 THRU 077777																		

Table 4-12. Sense Amplifier Control Signals

MEMORY ADDRESS	CARD LOCATION	CONTROL SIGNALS	TEST PINS
000000 thru 017777	A103	MOD 0 MOD 1	3 4
020000 thru 037777	A102	MOD 2 MOD 3	3 4
040000 thru 057777	A110	MOD 4 MOD 5	3 4
060000 thru 077777	A111	MOD 6 MOD 7	3 4

Table 4-13. Inhibit Driver Control Signals

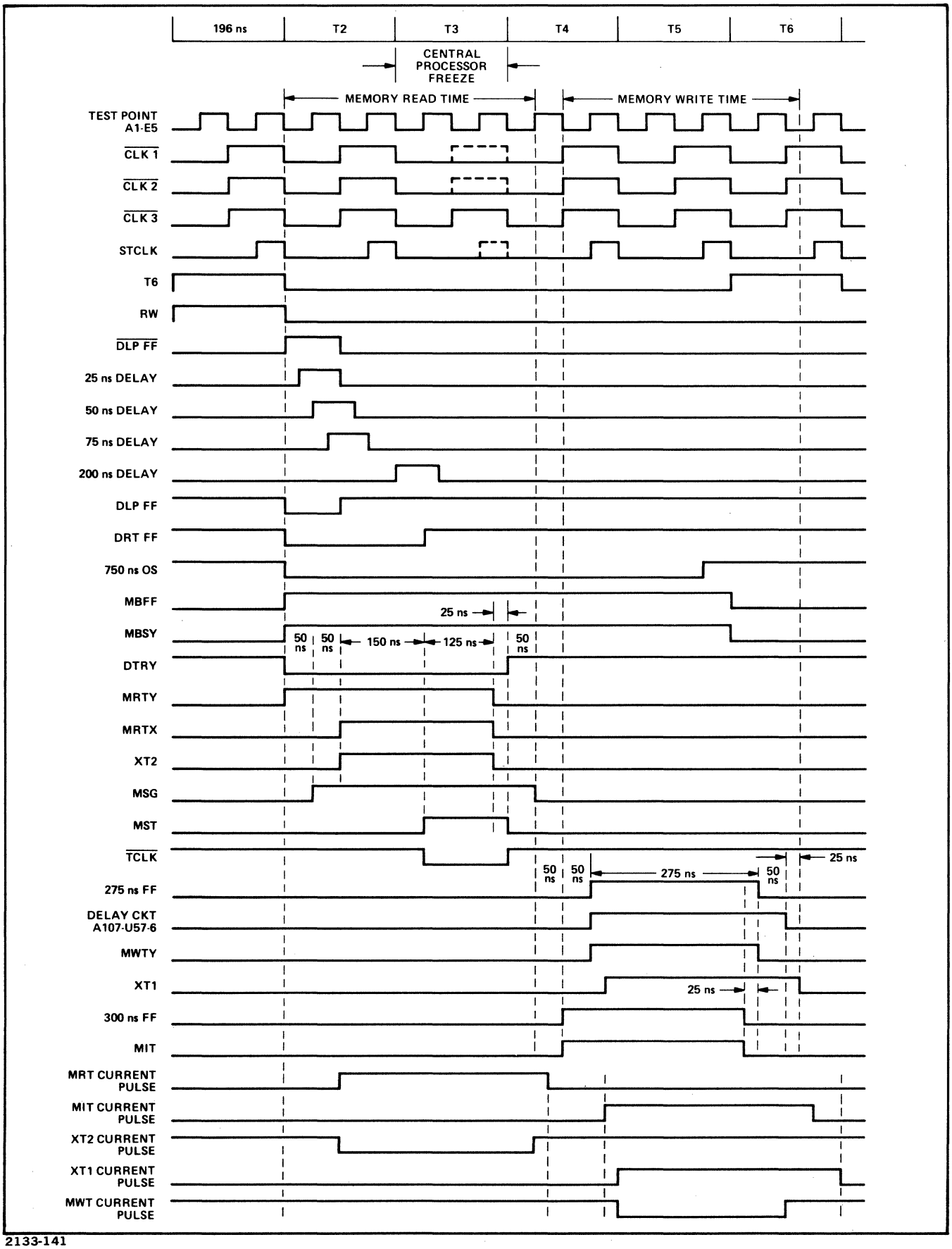
MEMORY ADDRESS	CARD LOCATION	CONTROL SIGNALS	TEST PINS
000000 thru 017777	A105	MOD 0 IDEM0-3 MOD 1	J1-47 5 J1-41
020000 thru 037777	A105	MOD 2 MOD 3	J1-45 J1-43
040000 thru 057777	A108	MOD 4 IDEM4-7 MOD 5	J1-47 5 J1-41
060000 thru 077777	A108	MOD 6 MOD 7	J1-45 J1-43

Table 4-14. Data Signal Test Points

CIRCUIT CARDS	GATING SIGNALS AND TEST POINTS (NOTE 1)	DATA SIGNALS AND TEST POINTS (NOTE 1)																
CORE STACK/ SENSE AMPLIFIER CARD A102, A103, A110, OR A111	MSG PIN 6	SA OUTPUT SIGNAL:	SA16	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
		SA OUTPUT PIN:	72	71	70	69	68	67	66	65	64	63	21	22	19	20	17	18	15
DATA CONTROL CARD A107	MST U81-3	SA INPUT PIN:	71	67	63	59	55	51	45	41	35	31	27	23	19	15	11	7	3
	NONE	TR OUTPUT SIGNAL:	TR16	TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
		TR OUTPUT PIN: J1-	31	33	37	39	35	17	23	21	19	9	11	7	5	15	13	1	3
INHIBIT DRIVER CARD A105 OR A108	MIT J1-25	TR INPUT PIN: J1-	31	33	37	39	35	17	23	21	19	9	11	7	5	15	13	1	3
		ID OUTPUT SIGNAL:	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		IDXXMX OUTPUT PIN:																	
		MODULE 0,4	15	71	70	69	71	50	49	46	31	34	33	32	37	9	8	7	10
		MODULE 1,5	16	64	63	62	65	67	66	68	72	42	41	43	38	13	12	11	14
		MODULE 2,6	17	75	74	73	76	45	51	44	52	58	59	60	53	24	25	19	26
		MODULE 3,7	18	82	83	77	84	80	81	79	78	55	56	54	57	21	22	23	20

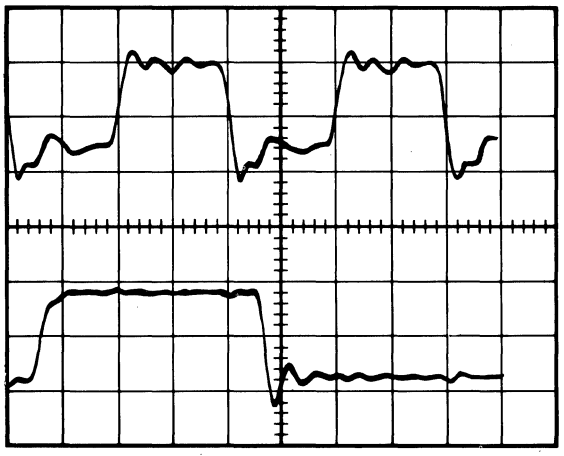
NOTES:

1. ALL TEST POINTS (PINS) ARE ON THE CIRCUIT CARD 86-PIN CONNECTOR OR ASSOCIATED BACKPLANE CONNECTOR UNLESS OTHERWISE SPECIFIED.



2133-141

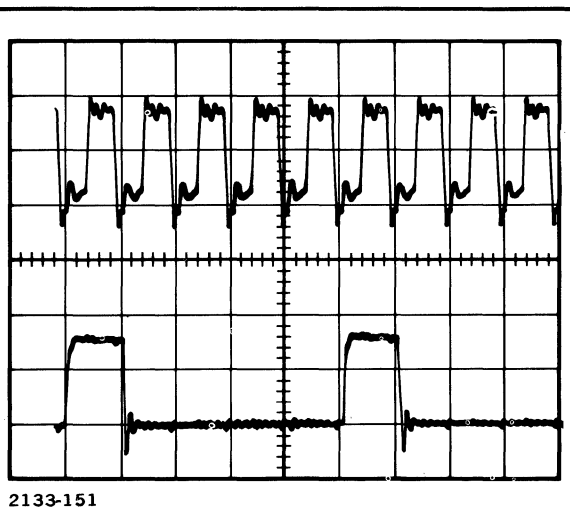
Figure 4-17. Memory Timing Specifications



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{CLK3}$):
Input A107-69
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.05 us

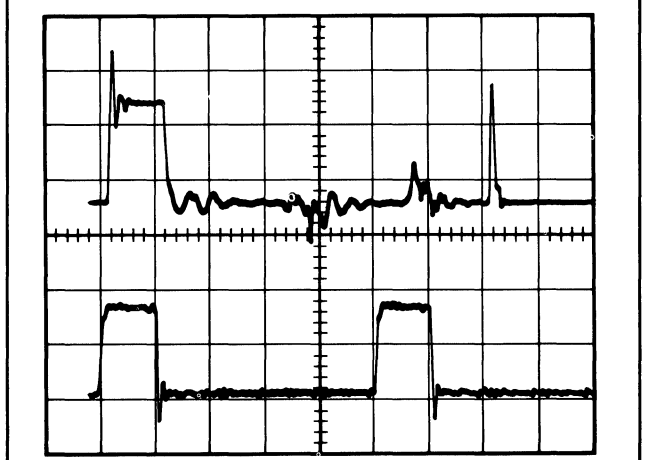
Figure 4-18. Signals $\overline{CLK3}$ and T6 Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{CLK3}$):
Input A107-69
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.2 us

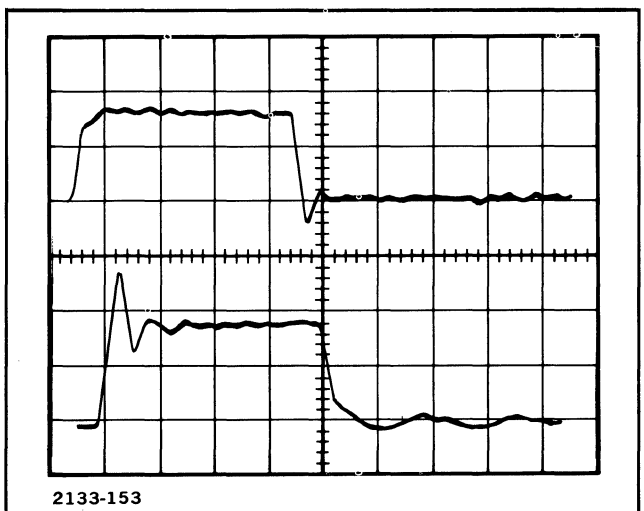
Figure 4-19. Signals $\overline{CLK3}$ and T6 Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (RW):
Input A107-75
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.2 us

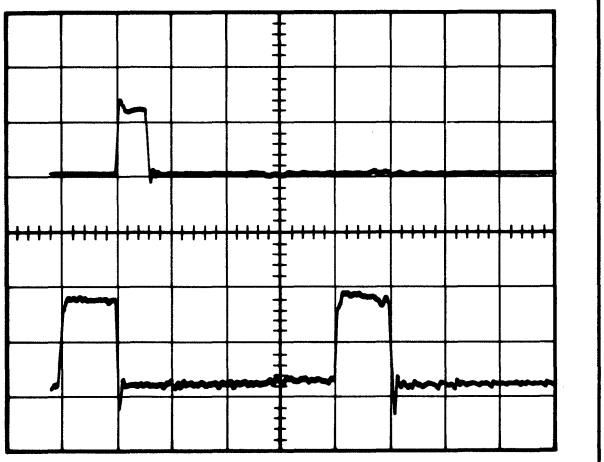
Figure 4-20. Signals RW and T6 Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (RW):
Input A107-75
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.05 us

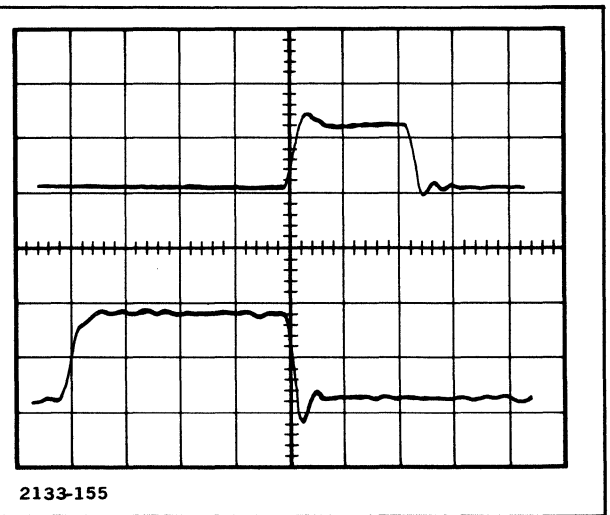
Figure 4-21. Signals T6 and RW Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.2 us

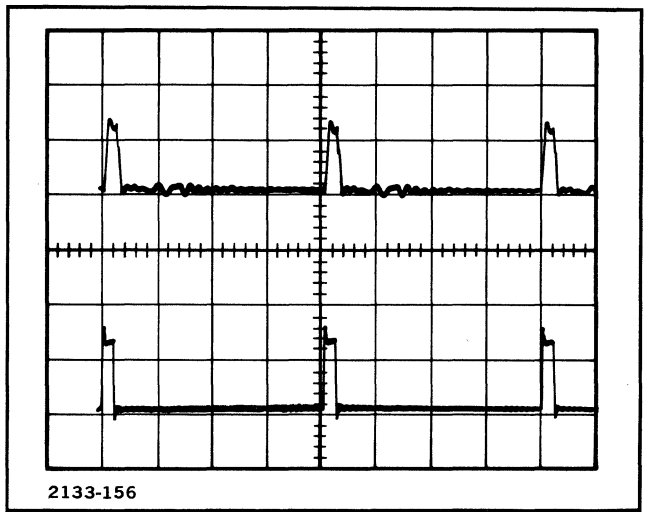
Figure 4-22. Signals $\overline{\text{DLPFF}}$ and T6 Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.05 us

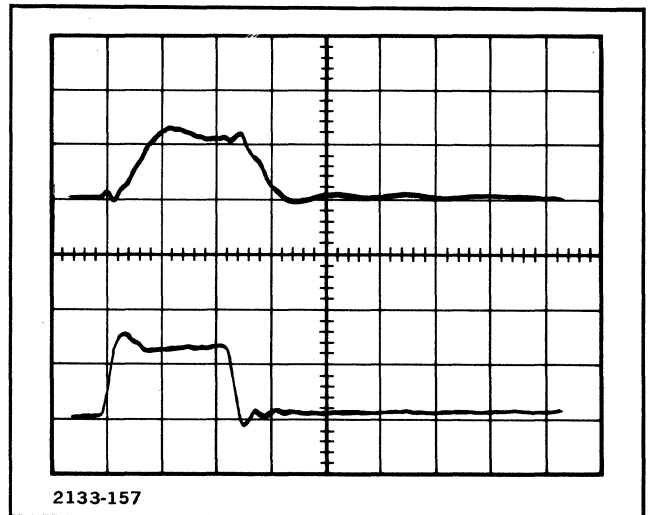
Figure 4-23. Signals $\overline{\text{DLPFF}}$ and T6 Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (25ns delay pulse):
Input A107-DL1-1
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.5 us

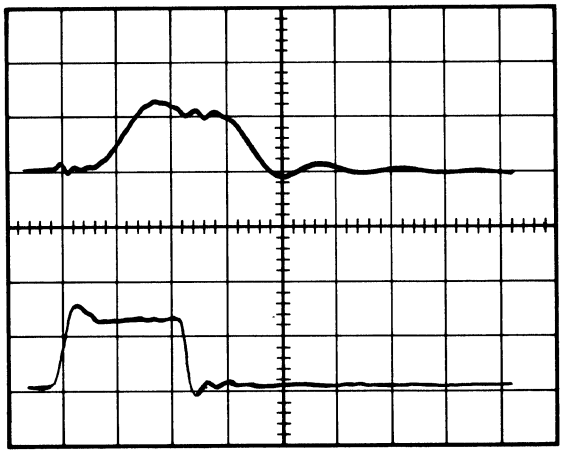
Figure 4-24. 25ns Delay Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (25ns delay pulse):
Input A107-DL1-1
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.5 us

Figure 4-25. 25ns Delay Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



2133-158

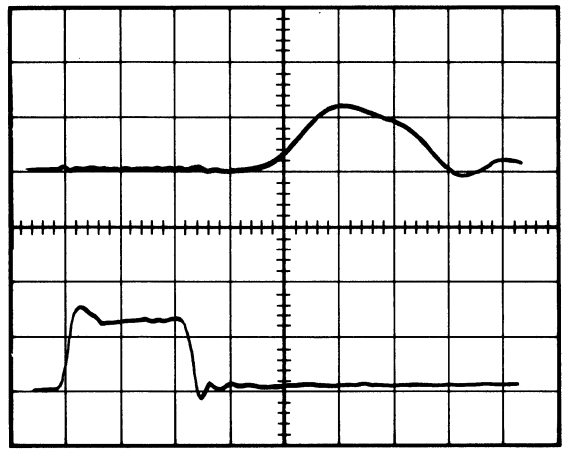
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (50ns delay pulse):
Input A107-DL1-2
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

Figure 4-26. 50ns Delay Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



2133-160

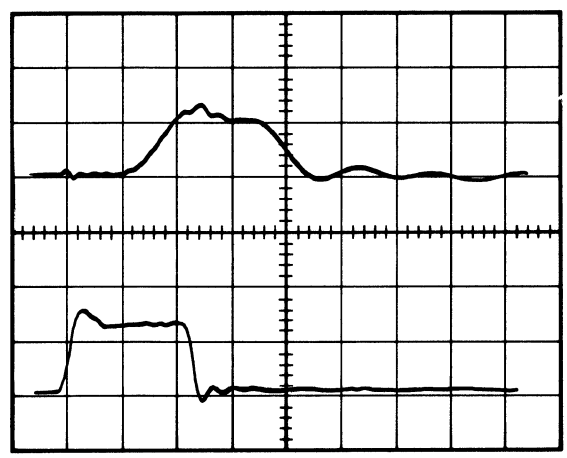
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (200ns delay pulse):
Input A107-DL1-8
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

Figure 4-28. 200ns Delay Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



2133-159

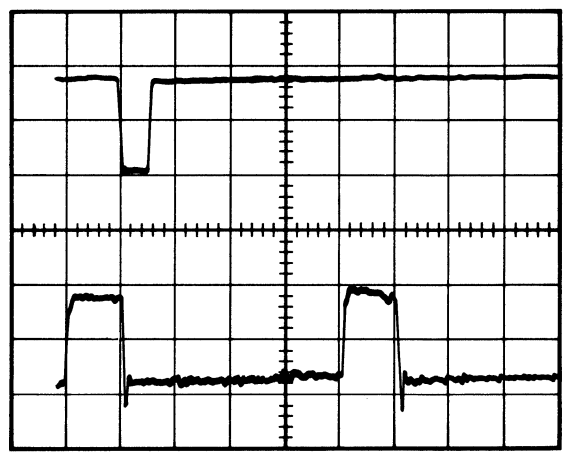
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (75ns delay pulse):
Input A107-DL1-3
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

Figure 4-27. 75ns Delay Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



2133-161

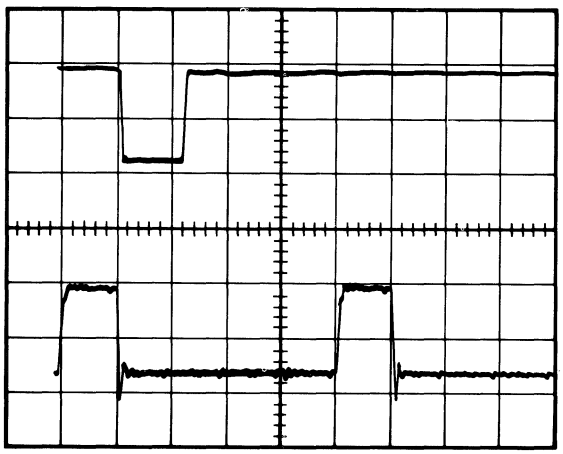
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{\text{DLPFF}}$):
Input A107-U75-5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-29. Signals $\overline{\text{DLPFF}}$ and T6 Waveforms



2133-162

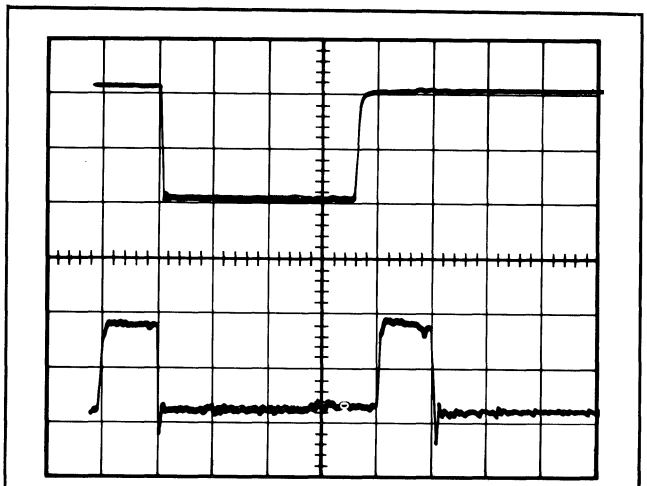
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (DRTFF):
Input A107-U102-9
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-30. Signals DRTFF and T6 Waveforms



2133-164

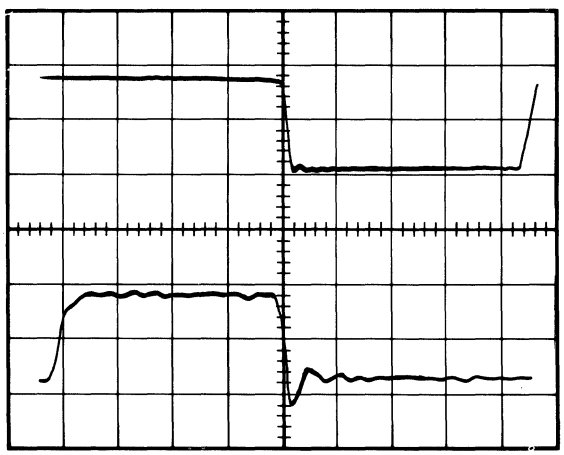
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (750 ns OS):
Input A107-U63-6
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-32. 750 ns One-Shot Output and Signal T6 Waveforms



2133-163

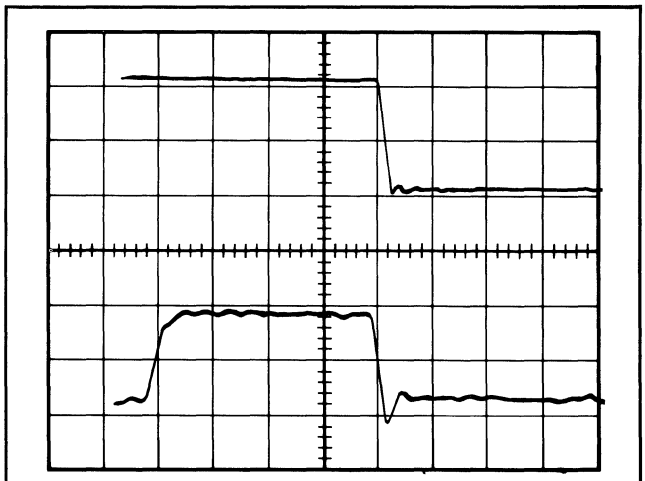
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (DRTFF):
Input A107-U102-9
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

Figure 4-31. Signals DRTFF and T6 Waveforms



2133-165

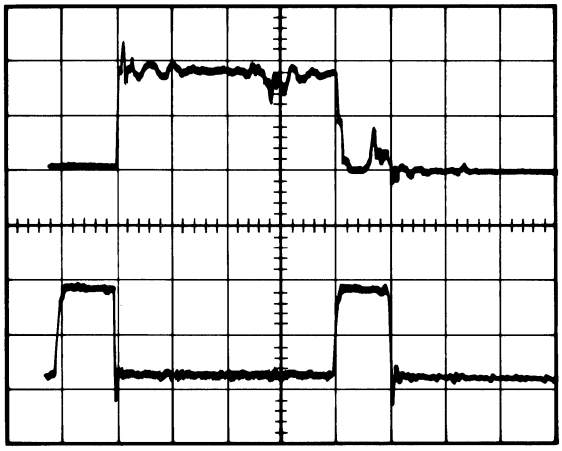
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (750 ns OS):
Input A107-U63-6
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

Figure 4-33. 750 ns One-Shot Output and Signal T6 Waveforms



2133-166

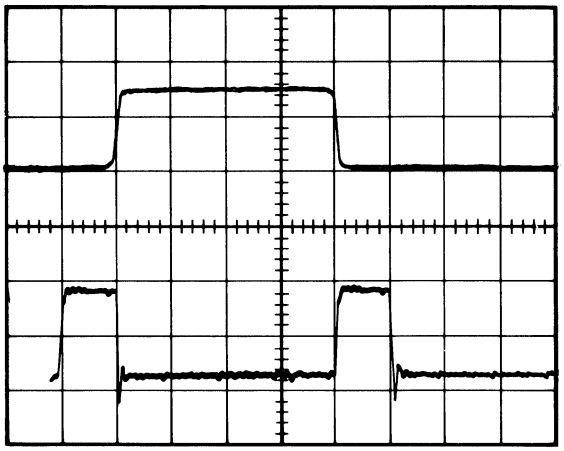
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MBSY):
Input A107-77
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-34. Signals MBSY and T6 Waveforms



2133-168

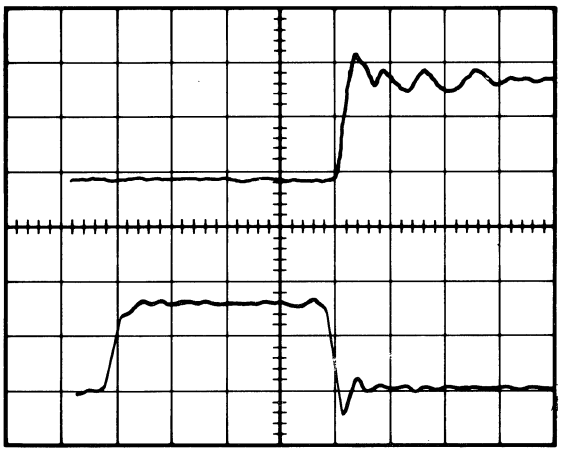
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MBFF):
Input A107-U105-5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-36. Signals MBFF and T6 Waveforms



2133-167

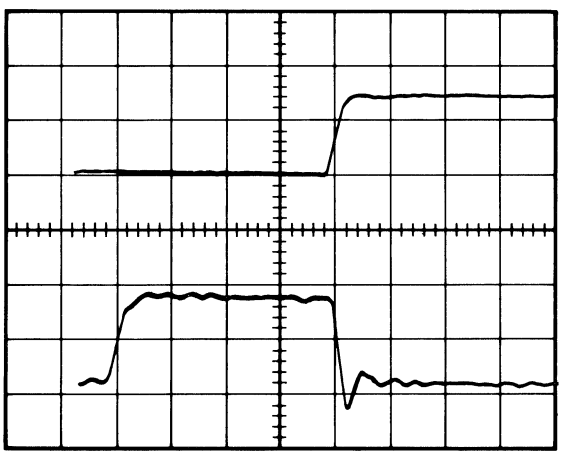
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MBSY):
Input A107-77
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-35. Signals MBSY and T6 Waveforms



2133-169

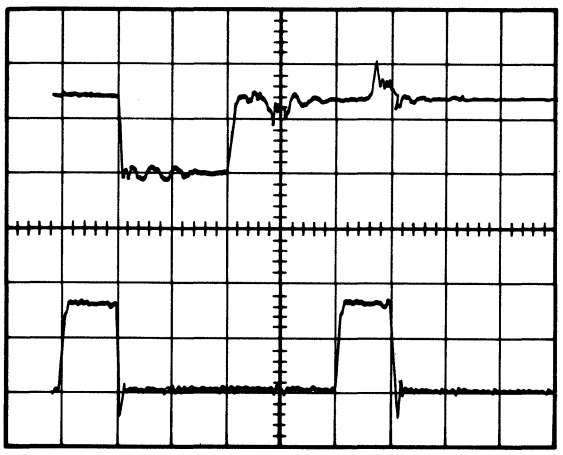
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MBFF):
Input A107-U105-5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.05 us

Figure 4-37. Signals MBFF and T6 Waveforms

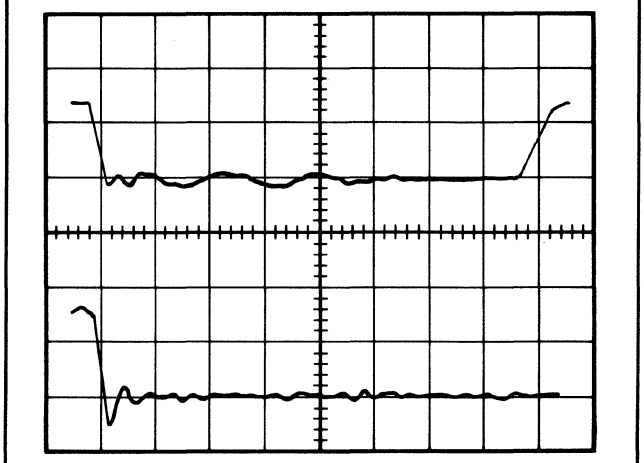


2133-170

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (DTRY):
Input A107-81
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.2 us

Figure 4-38. Signals DTRY and T6 Waveforms

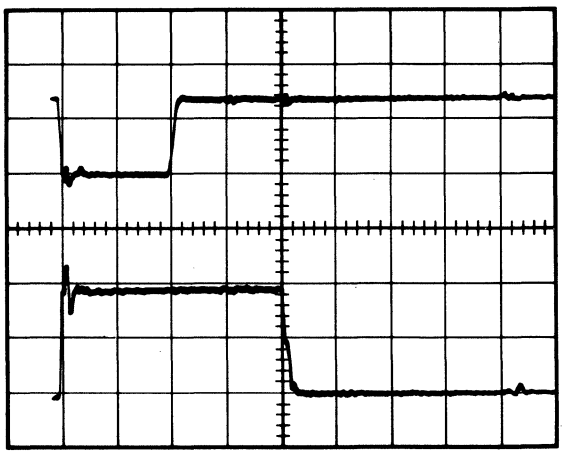


2133-172

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (DTRY):
Input A107-81
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.05 us

Figure 4-40. Signals DTRY and T6 Waveforms

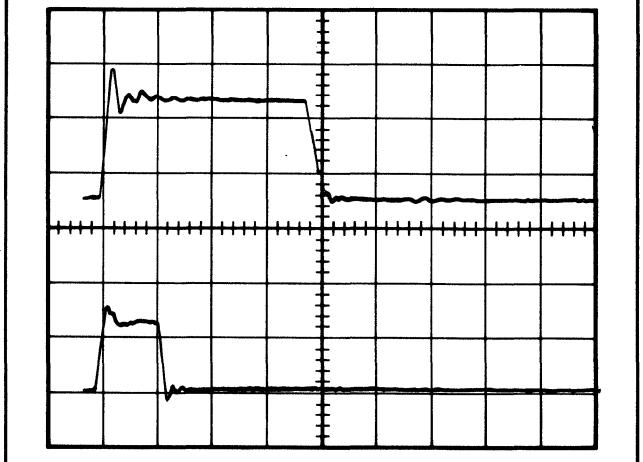


2133-171

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (DTRY):
Input A107-81
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (MBSY):
Input A107-77
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.2 us

Figure 4-39. Signals DTRY and MBSY Waveforms

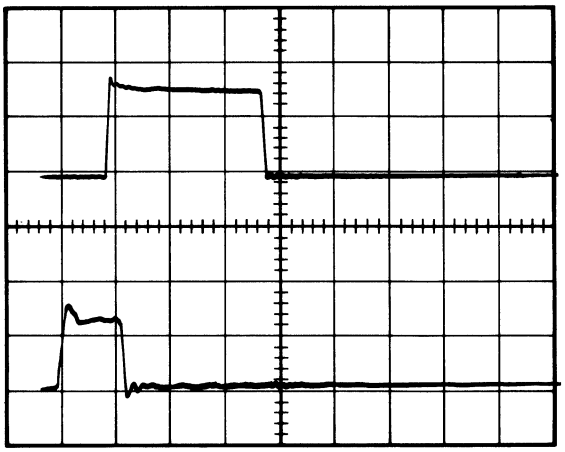


2133-173

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRTY):
Input A107-84
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

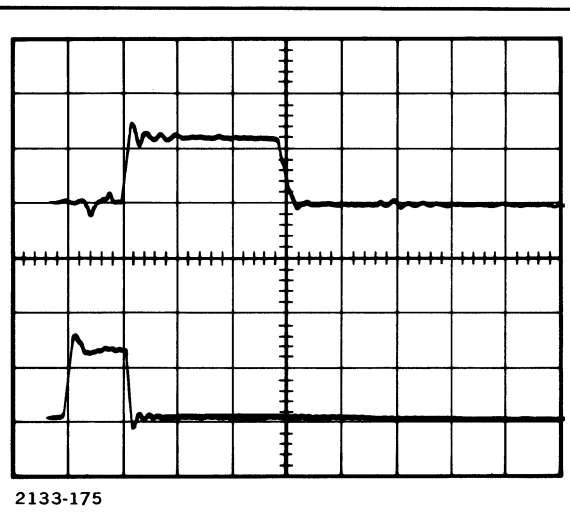
Figure 4-41. Signals MRTY and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRTX):
Input A107-U81-8
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

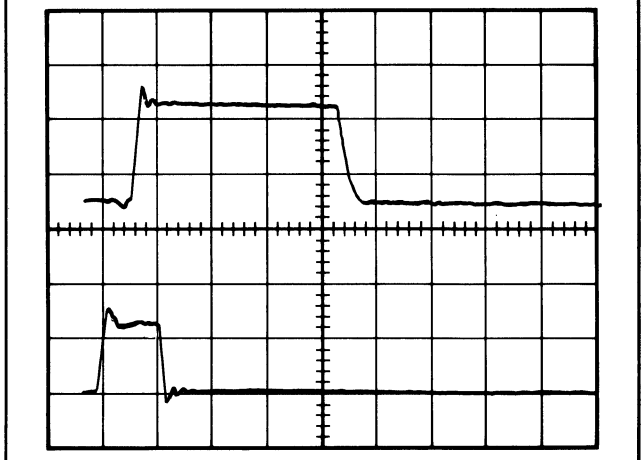
Figure 4-42. Signals MRTX and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (XT2):
Input A107-64
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

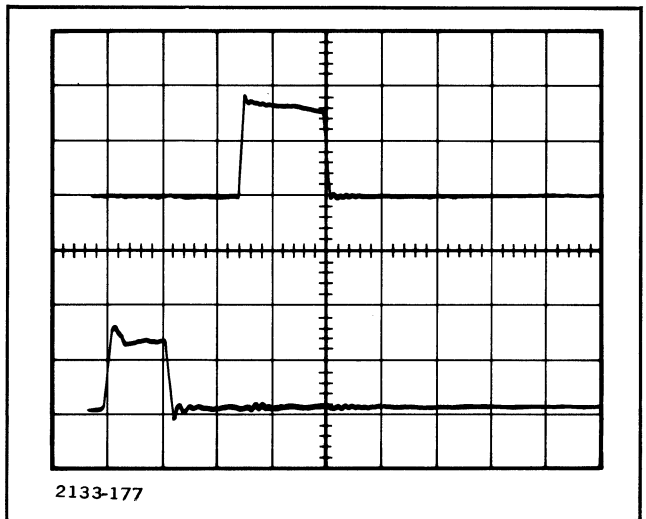
Figure 4-43. Signals XT2 and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MSG):
Input A107-83
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

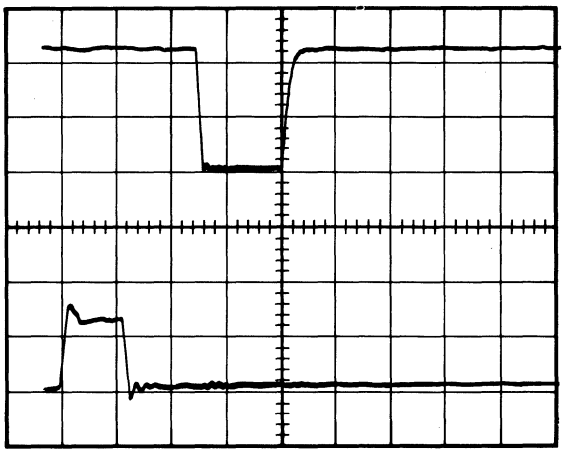
Figure 4-44. Signals MSG and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MST):
Input A107-U81-3
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

Figure 4-45. Signals MST and $\overline{\text{DLPFF}}$ Waveforms



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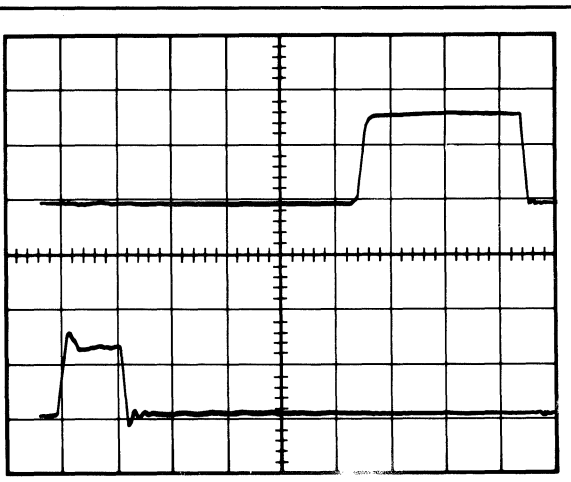
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{\text{TCLK}}$):
Input A107-U103-8
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

Figure 4-46. Signals $\overline{\text{TCLK}}$ and $\overline{\text{DLPFF}}$ Waveforms



2133-179

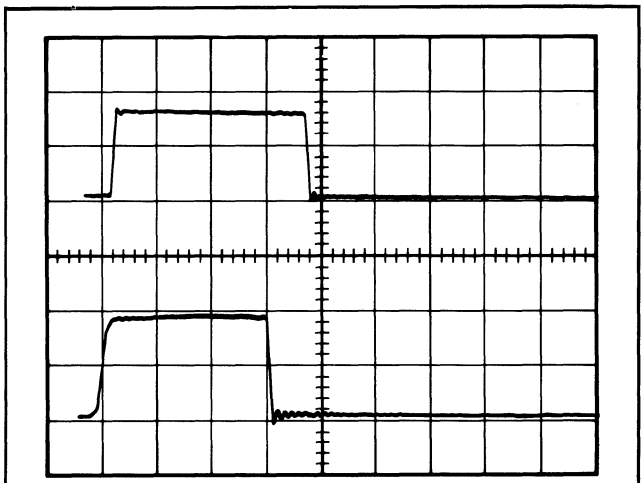
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (275ns FF):
Input A107-U43-8
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (DLPFF):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

Figure 4-47. 275ns FF Output and Signal $\overline{\text{DLPFF}}$ Waveforms



2133-180

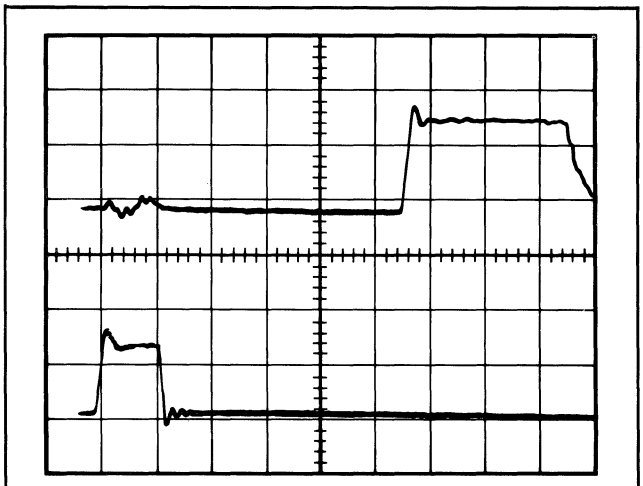
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (A107 U57-6):
Input A107-U57-6
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (275ns FF):
Input A107-U43-8
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

Figure 4-48. A107 U57-6 and 275ns FF Outputs Waveforms



2133-181

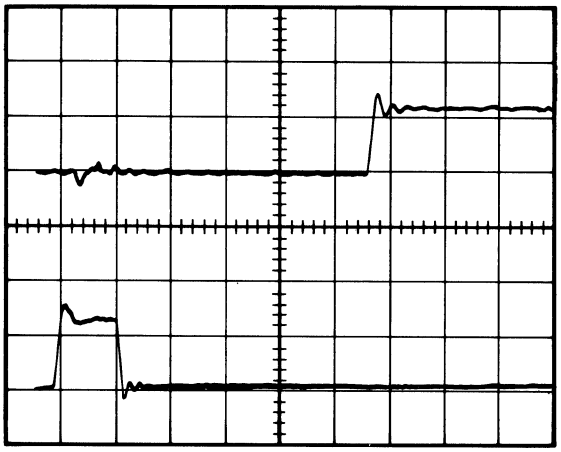
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWTY):
Input A107-28
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

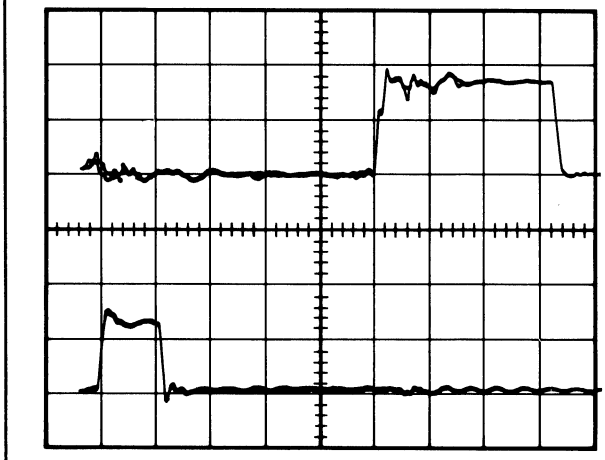
Figure 4-49. Signals MWTY and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (XT1):
Input A107-65
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

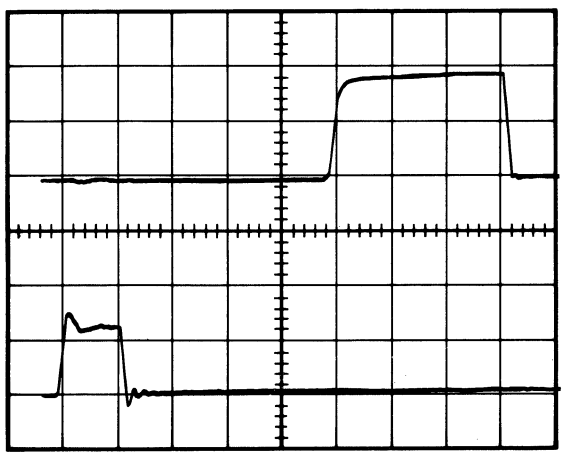
Figure 4-50. Signals XT1 and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MIT):
Input A107-U95-6
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

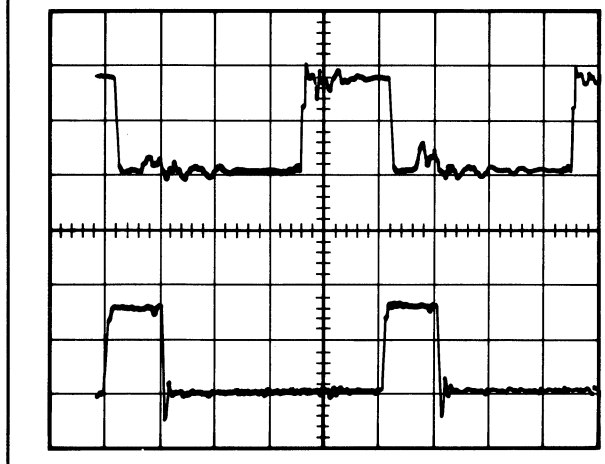
Figure 4-52. Signals MIT and $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (300ns FF):
Input A107-U53-8
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.1 us

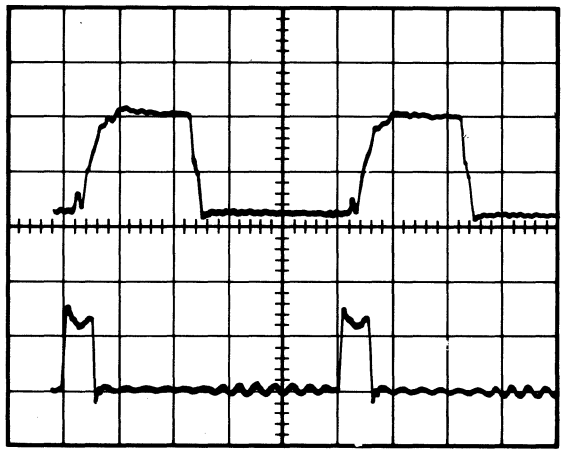
Figure 4-51. 300ns FF Output and Signal $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MIT):
Input A107-U95-6
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Channel B (T6):
Input A24-66
Volts/cm . . . . . 0.2 (if using 10:1 probe)
Time/cm . . . . . 0.2 us

Figure 4-53. Signals MIT and T6 Waveforms



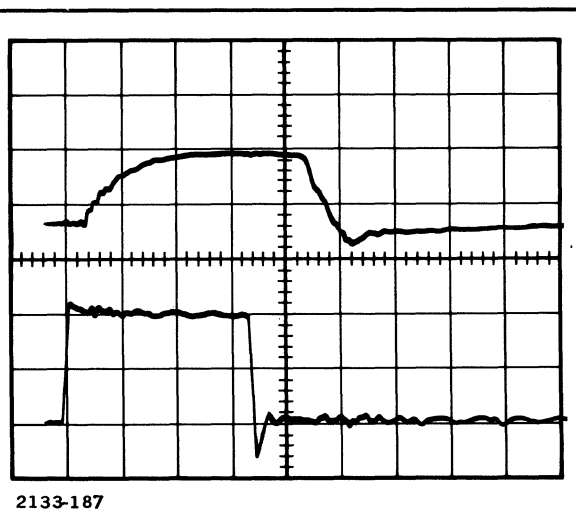
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRT Current Pulse):
Input . . . . . A104-D (48-pin connector)
Volts/cm . 0.2 (using 1mv = 1ma current probe)

Channel B ($\overline{\text{DPLFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-54. MRT Current Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



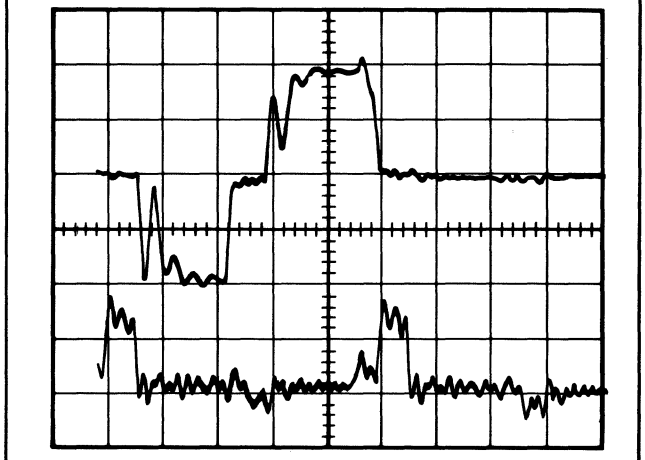
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (Inhibit Current Pulse ID16M2):
Input A107-17
Volts/cm . 0.5 (using 1mv = 1ma current probe)

Channel B (MIT): .
Input A105-U11-2
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

Figure 4-55. Inhibit Current Pulse ID16M2 and Signal MIT Waveforms



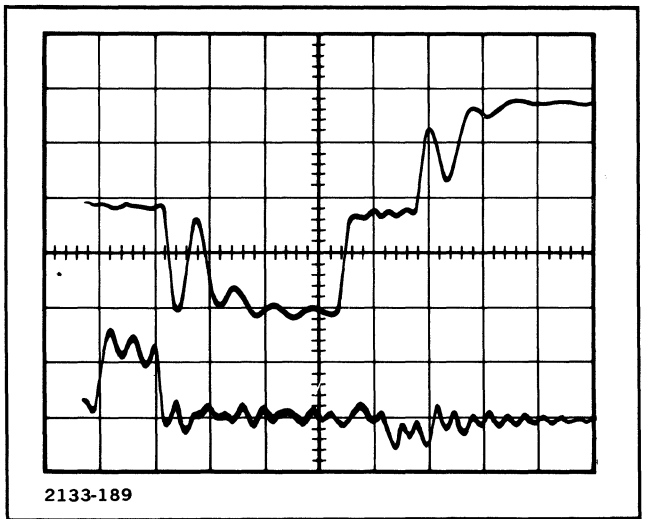
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (XT1 and XT2 Current Pulses):
Input . . . . . A104-9 (48-pin connector)
Volts/cm . 0.2 (using 1mv = 1ma current probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-56. XT1 and XT2 Current Pulses and Signal DLPFF Waveforms



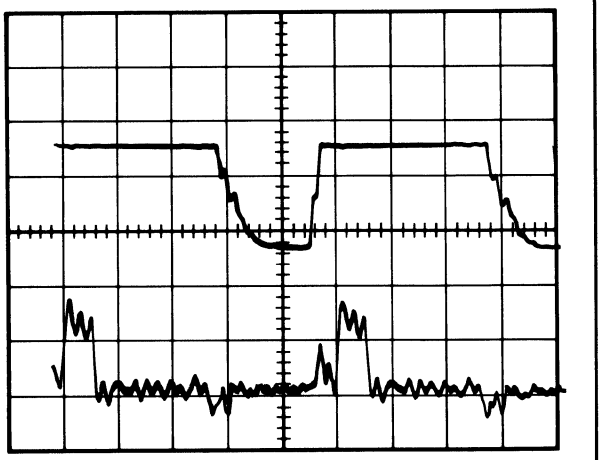
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (XT1 and XT2 Current Pulse):
Input . . . . . A104-9 (48-pin connector)
Volts/cm . 0.2 (using 1mv = 1ma current probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

Figure 4-57. XT1 and XT2 Current Pulses and Signal $\overline{\text{DLPFF}}$ Waveforms



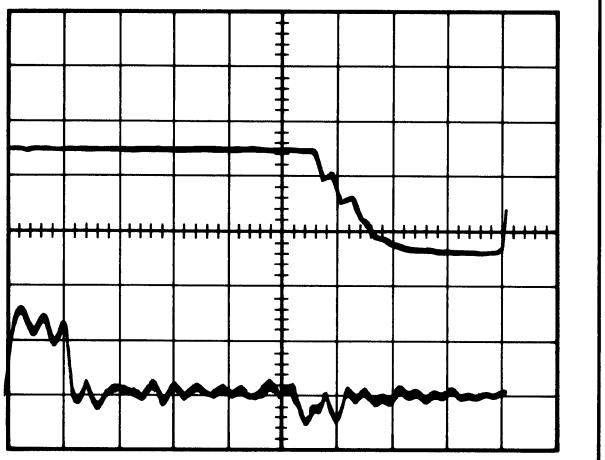
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWT Current Pulse):
Input . . . . . A104-4 (48-pin connector)
Volts/cm . 0.2 (using 1mv = 1ma current probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A107-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-58. MWT Current Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms



OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWT Current Pulse):
Input . . . . . A104-4 (48-pin connector)
Volts/cm . 0.2 (using 1mv = 1ma current probe)

Channel B ($\overline{\text{DLPFF}}$):
Input . . . . . Test Point A105-E5
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.1 us

Figure 4-59. MWT Current Pulse and Signal $\overline{\text{DLPFF}}$ Waveforms

4-156. INPUT/OUTPUT SECTION SERVICING.

4-157. GENERAL.

4-158. Input/Output section servicing information consists of an interrupt test procedure (refer to paragraph 4-161), I/O control and interrupt signals timing diagrams (see figures 4-60 and 4-61), interrupt priority servicing diagram (see figure 4-62), and an interrupt flowchart (see figure 4-63). For servicing information pertaining to special computer functions which operate through the interrupt system (such as parity error, memory protect, power fail, DMA, and floating point), refer to paragraph 4-171, Special Computer Functions Servicing.

4-159. TROUBLESHOOTING APPROACH.

4-160. When troubleshooting the I/O section, it is first necessary to determine whether the fault is in the I/O device, the I/O interface card, the I/O buffer card, or the I/O control card. Other sections of the computer must also be eliminated as the source of trouble. The following procedure is used:

a. Run diagnostic programs for all sections of the computer other than the I/O section. A list of the diagnostic program procedures for testing various sections of the computer is given in table 4-3. Usually it will not be necessary to run diagnostic programs for non-I/O options.

b. Run the diagnostic program for the I/O device that is operating improperly.

c. Run a diagnostic program for another I/O device, or for the DMA system if the I/O device uses DMA. If DMA and the second I/O device functions properly, the fault probably is in the first I/O device or its interface card. Make oscilloscope, voltmeter, and ohmmeter checks to find the defective component or faulty connection.

d. If the diagnostic program for the second I/O device also shows failures, the I/O control card or I/O buffer card is probably at fault. Make oscilloscope, voltmeter, and ohmmeter checks to find the defective component or faulty connection. Paragraph 4-164 presents a simple test program which can be run during troubleshooting. Figure 4-61 is a timing diagram of the signals found on the I/O Control and I/O Buffer cards while running the test program. Note that only the CLF, STF, STC, and NOP instructions are shown. When running the test program it is necessary to change the HLT instruction to a NOP, thereby extending the time the NOP conditions will exist. If the DMA diagnostic program was run and showed failures, troubleshoot the DMA system. For further details regarding the I/O system, refer to the detailed theory in Section III of this manual.

4-161. INTERRUPT PHASE TEST.

4-162. The following paragraphs provide a description and test procedure for the circuits used by the interrupt fetch phase (phase 1B). The processing operations are summarized in figure 4-63.

Note: If the EXTERNAL PRESET indicator is on, the interrupt fetch phase is inoperative. The priority chain is broken by the clear state of the power fail control FF. Refer to figures 4-92 and 4-93 for the operation of this indicator and related circuits.

4-163. DESCRIPTION. Any input/output device attached to the computer can interrupt computer operation by requesting to be serviced. The power-fail interrupt, memory protect, and parity error features of the basic computer and the direct memory access accessory feature can also generate the interrupt phase. When service is requested by a device, phase 1B is generated. At the end of the currently operating phase, the microroutine for phase 1B in the ROM microprogram will be activated (exceptions to this are the JMP-I and JSB instructions). The microroutine for phase 1B causes the P-register to be decremented by one and the select code of the interrupting device to be forced into the M-register forming the address of the next instruction. The next instruction is then placed in the I-register, and if the instruction is a memory reference group instruction, the operand address is placed in Scratch Pad 1. The execute phase (phase 3) is set and the computer is ready to process the instruction in the I-register.

4-164. TEST PROCEDURE. To test the interrupt fetch phase circuits, proceed as follows:

Note: If an address other than 001000 is used for the following test, modify the DISPLAY REGISTER settings accordingly. The following test requires that an input/output device interface card be plugged into slot 23 of the computer. The I/O device must be connected and in the ready state.

a. At the computer front panel, press and release the M switch and set the DISPLAY REGISTER to 001000.

b. Press and release the MEMORY DATA switch and set the DISPLAY REGISTER to 103100 (CLF-0 instruction).

c. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 102100 (STF-0 instruction).

d. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 102700 (STC-0 instruction).

e. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 102110 (STF-10 instruction).

f. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 102710 (STC-10 instruction).

g. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 102000 (HLT instruction).

h. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 000000 (NOP instruction).

i. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 027000 (JMP instruction).

j. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 000010 (interrupt location).

k. Press and release the INCREMENT M switch and set the DISPLAY REGISTER to 002004 (INA instruction).

l. Press and release the P switch and set the DISPLAY REGISTER to 001000.

m. Continuously press and release the RUN switch. The A-register will increment by one if the interrupt circuits are operating correctly.

Note: Refer to Section III of this manual for additional input/output section information.

4-165. If the A-register does not increment by one, indicating the interrupt circuits are not operating properly, proceed as follows:

a. Press and release the M switch and set the DISPLAY REGISTER to 001005.

b. Press and release the MEMORY DATA switch and set the DISPLAY REGISTER to 000000 (NOP instruction).

c. Press and release the P switch and set the DISPLAY REGISTER to 001000.

d. Press and release the RUN switch.

4-166. The computer is now in the run mode continuously looping the program beginning at location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-61. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T6 at pin 43 of I/O Buffer Card A8 and use channel B as the triggering source. Set oscilloscope time/cm for 2 μs per division.

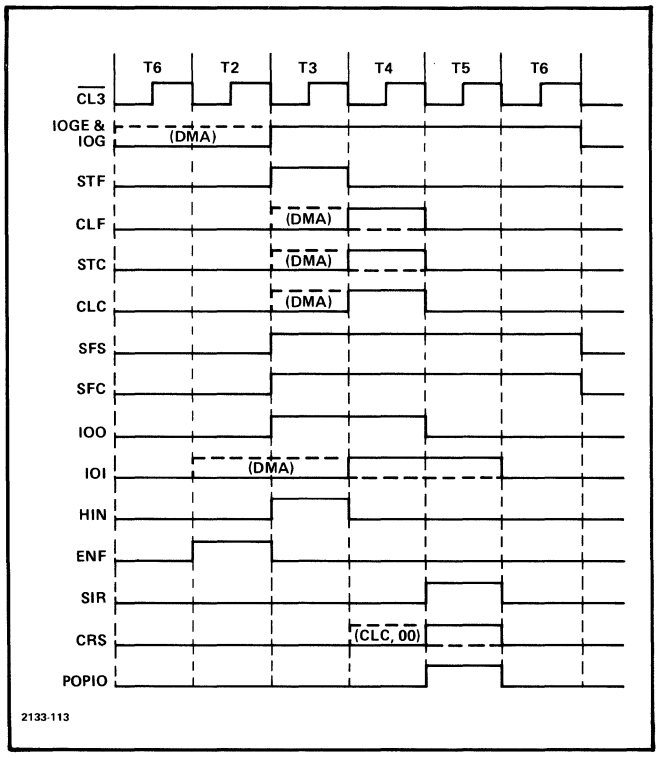
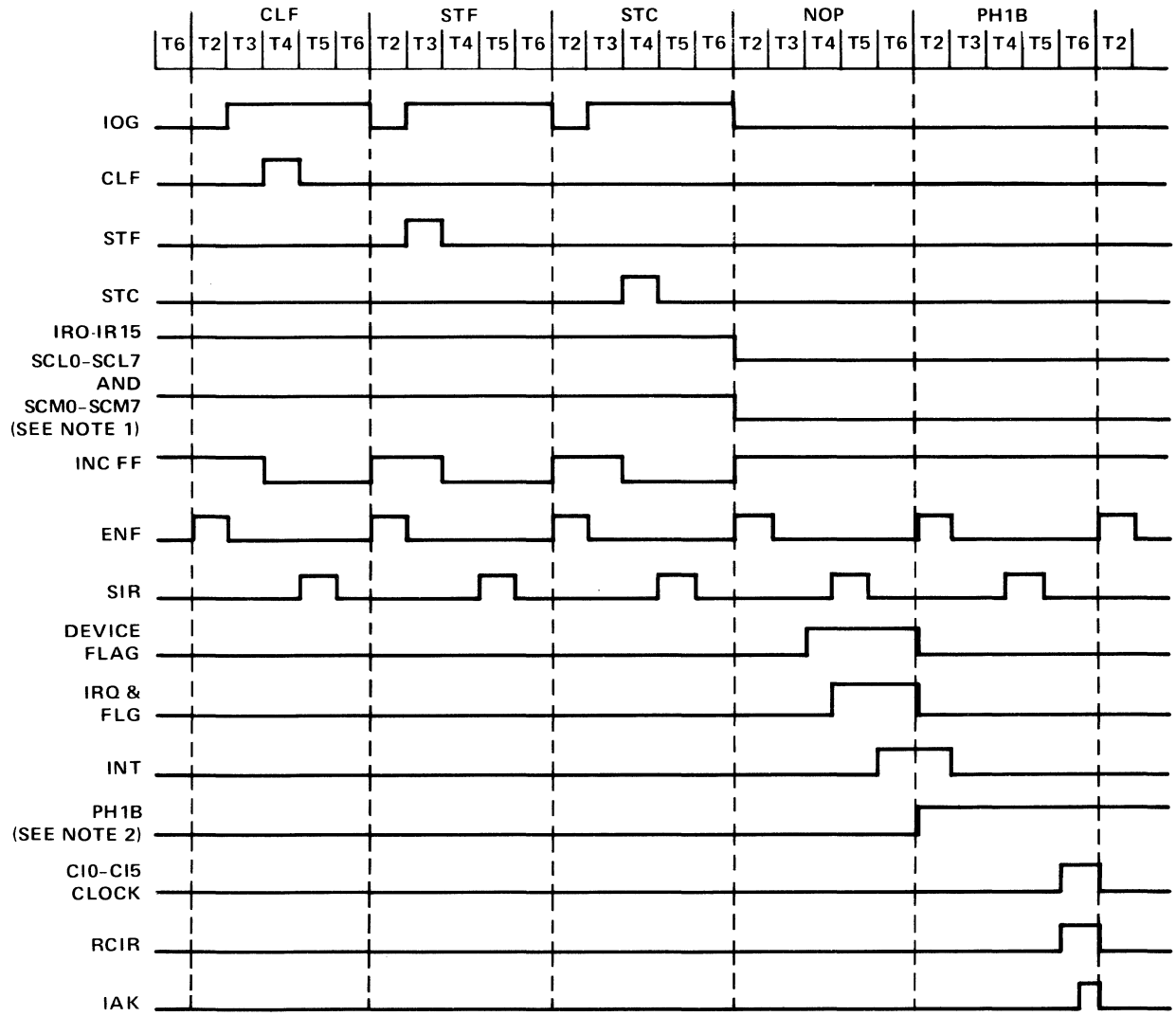


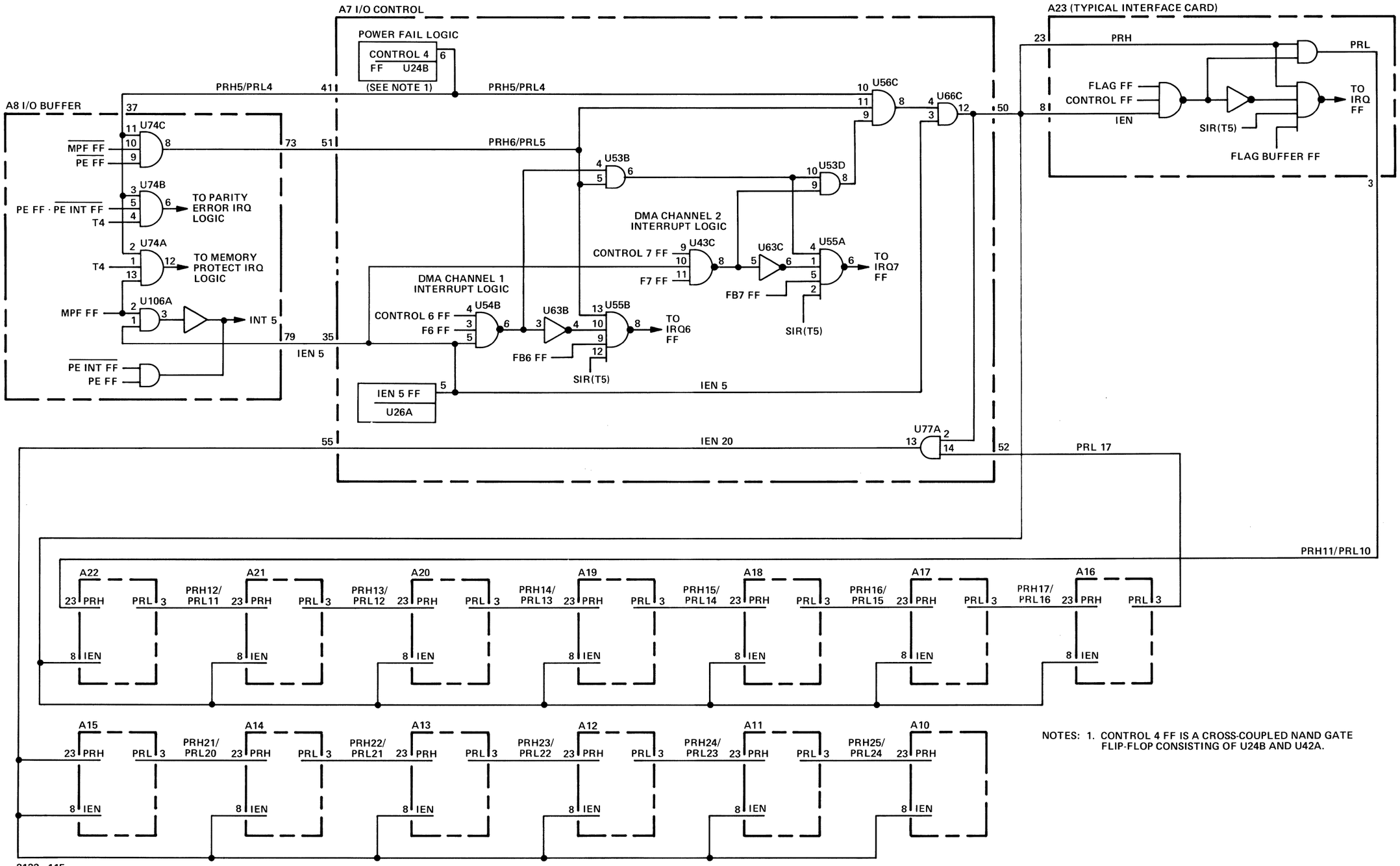
Figure 4-60. I/O Control Signals Timing



NOTES:
1. IF THE I/O INSTRUCTION BEING EXECUTED IS IN THE A- OR B-REGISTER, THE SELECT CODE BECOMES VALID 150 NANOSECONDS AFTER THE START OF TIME T2 OF PHASE 1A. IF THE INSTRUCTION IS IN MEMORY, THE SELECT CODE BECOMES VALID 150 NANOSECONDS AFTER THE START OF TIME T4 OF PHASE 1A.
2. THE I/O TIME OF SETTING OF PHASE 1B WILL DEPEND UPON WHAT I/O TIME IS PRESENT WHEN EOP IS DETECTED IN THE SKIP FIELD. THE PH1B MICRO-ROUTINE EXECUTION DOES NOT START UNTIL TIME T6.

2133-114

Figure 4-61. Interrupt Signals Timing



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NOTES: 1. CONTROL 4 FF IS A CROSS-COUPLED NAND GATE FLIP-FLOP CONSISTING OF U24B AND U42A.

Figure 4-62. Interrupt Priority Continuity Servicing Diagram

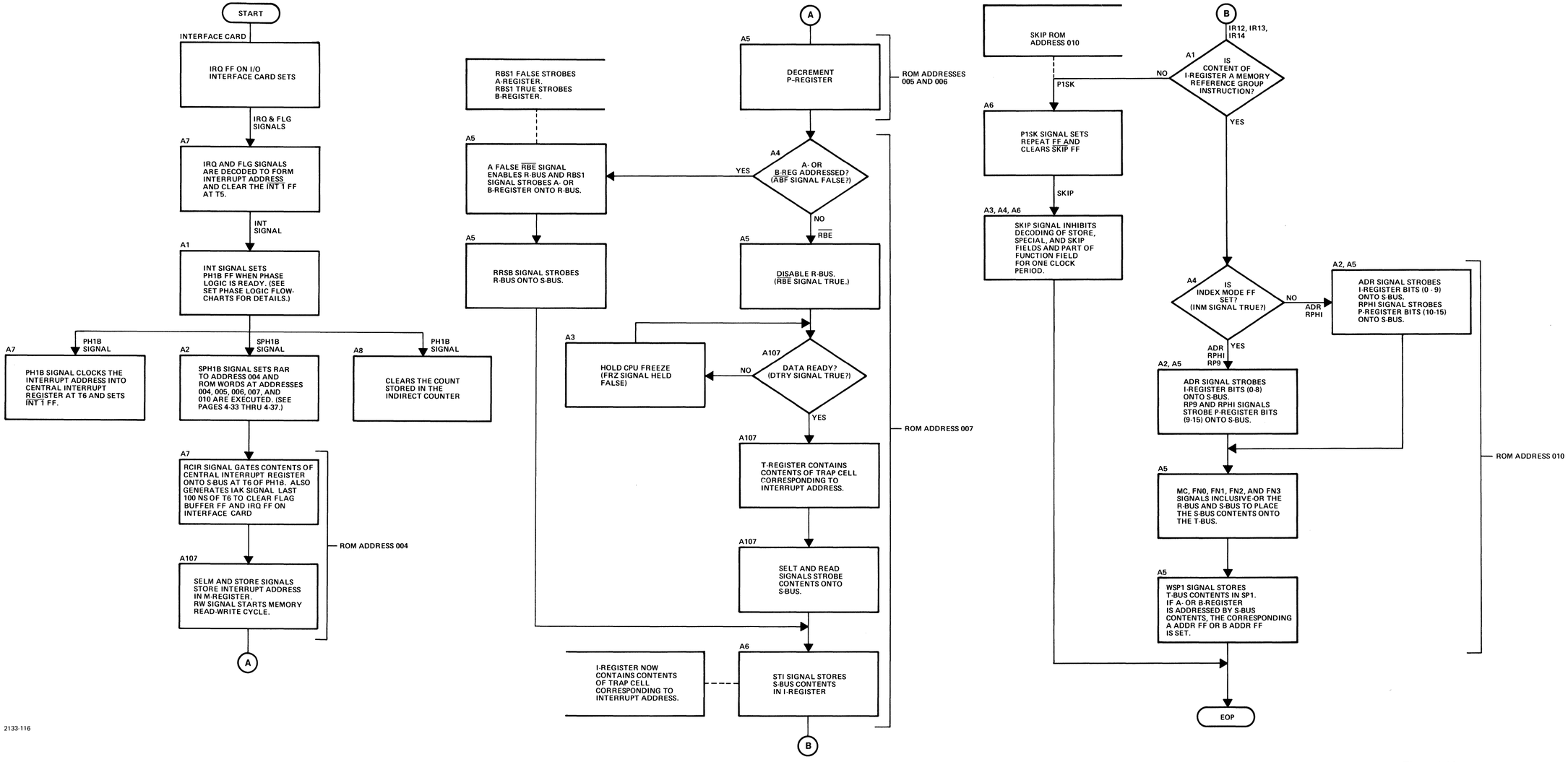
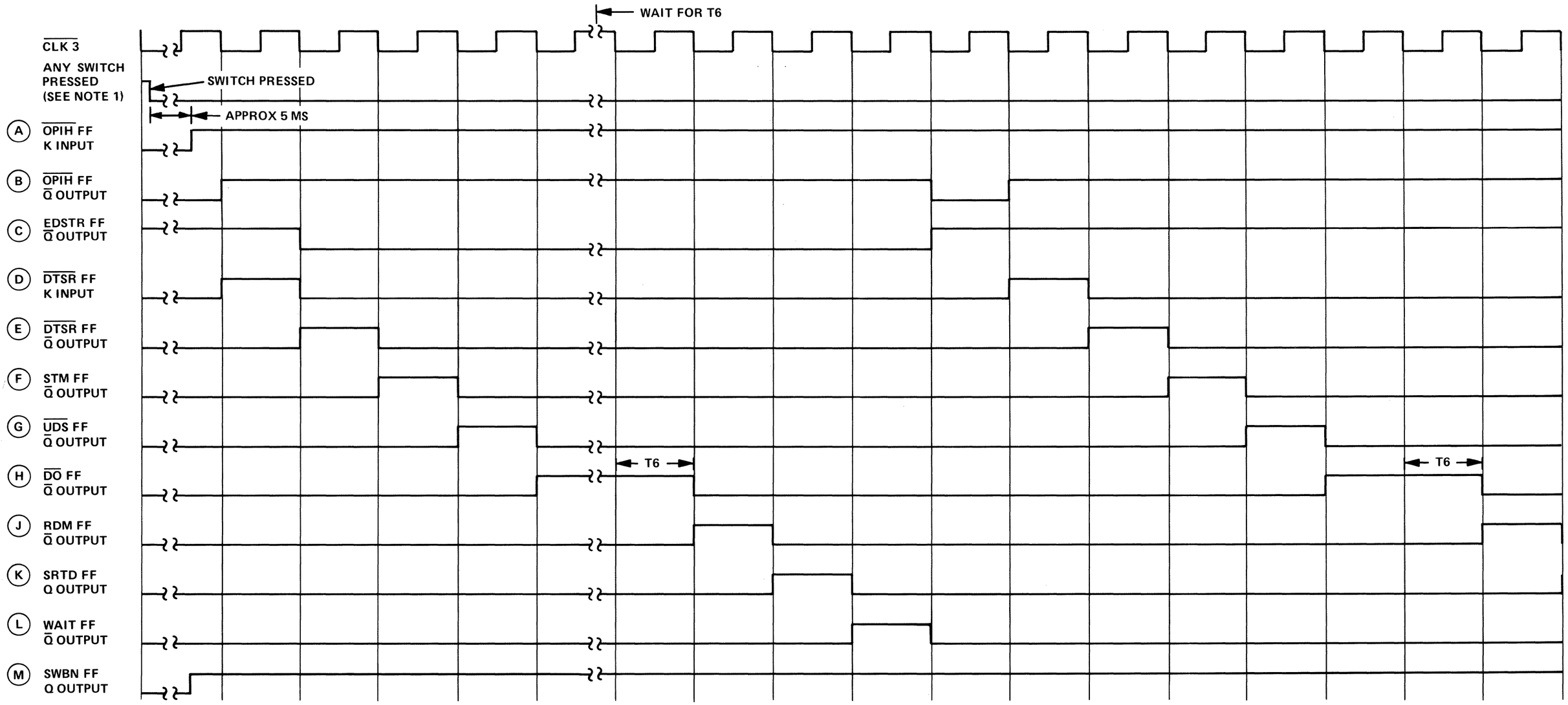


Figure 4-63. Interrupt Flowchart

4-167. OPERATOR PANEL SERVICING.

4-168. Operator panel servicing information consists of timing and servicing diagrams for each switch on the operator panel. The timing of the switch circuits is controlled by the timing of the control logic circuits. Figure 4-64 shows sample timing associated with the control logic circuits which are shown in figure 4-65. Figures 4-66 through 4-101 show the timing and logic circuits associated with each operator panel switch. A list of the figures with their corresponding page numbers is given below.

OPERATOR PANEL CONTROL LOGIC TIMING WITH OPERATION SWITCH S39 IN LOOP POSITION



NOTES:
1. ANY SWITCH DOES NOT INCLUDE MEMORY DATA, RUN, HALT/CYCLE, CLEAR DISPLAY, OR DISPLAY REGISTER SWITCHES.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM. (LETTER "I" IS NOT USED).

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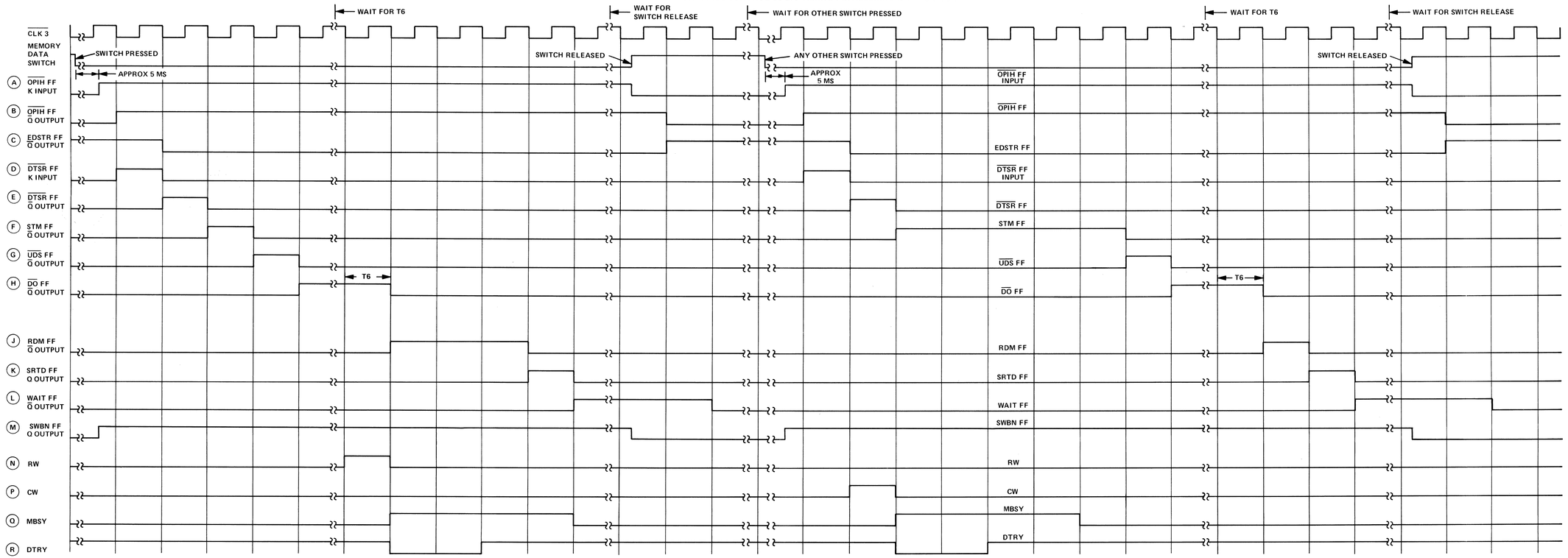
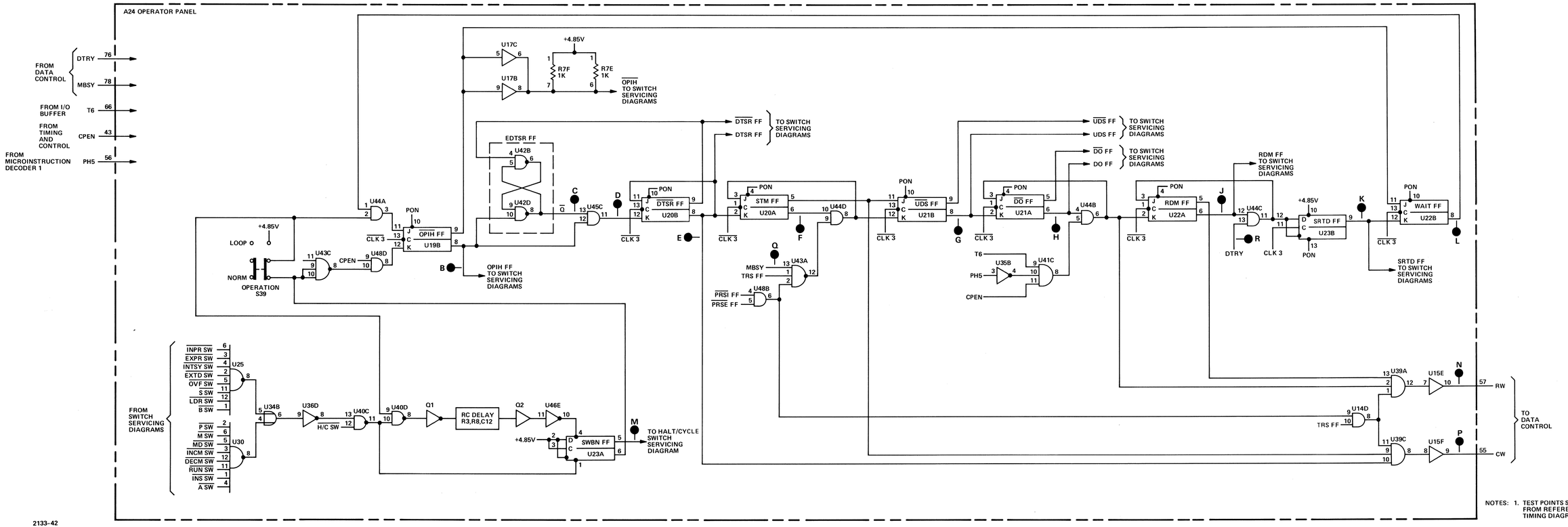
Figure 4-64. Operator Panel Control Logic Timing Diagram (Sheet 1 of 2)

OPERATOR PANEL CONTROL LOGIC TIMING FOR MEMORY DATA SWITCH



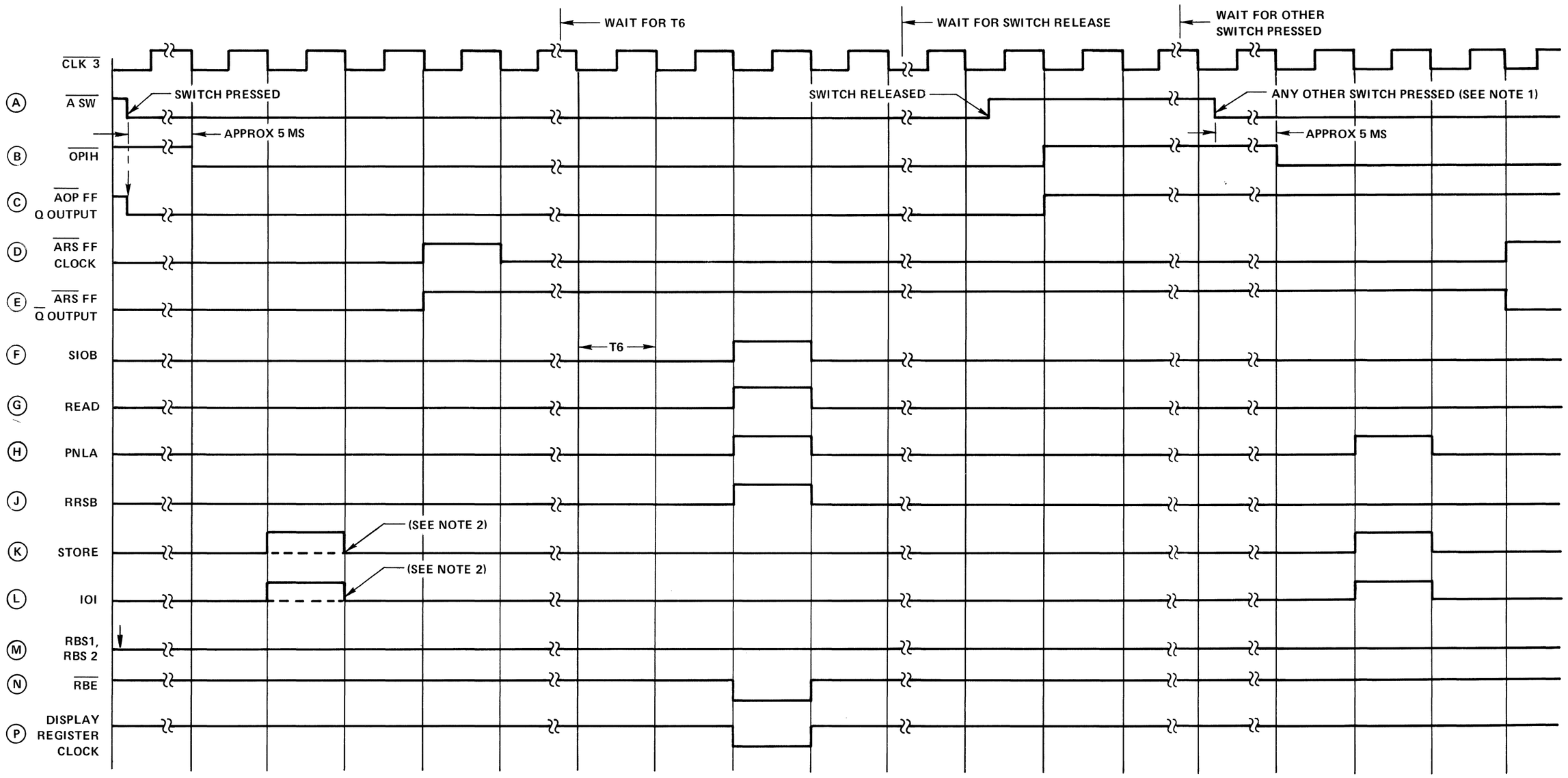
NOTES: 1. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTERS "I" AND "O" ARE NOT USED).

Figure 4-64. Operator Panel Control Logic Timing Diagram (Sheet 2 of 2)



NOTES: 1. TEST POINTS SHOWN ARE FROM REFERENCE TO TIMING DIAGRAM ONLY.

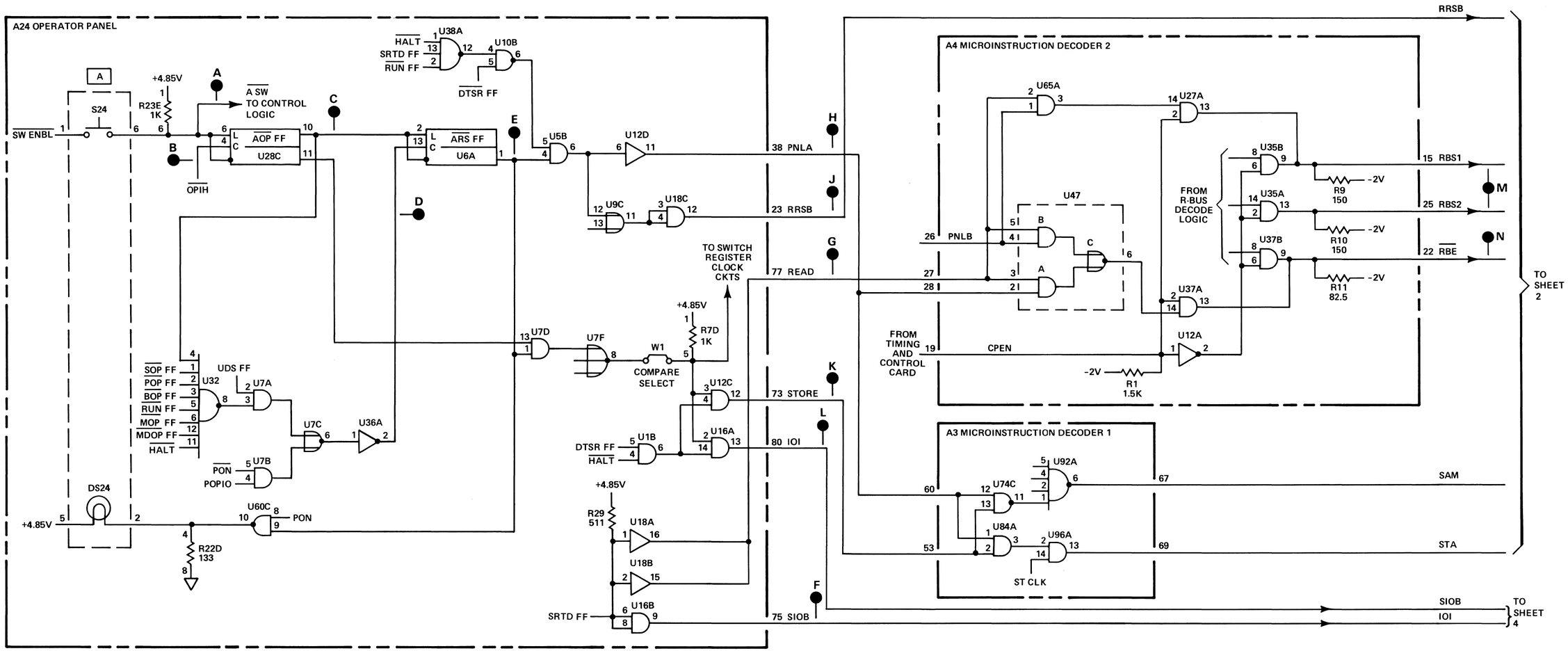
Figure 4-65. Operator Panel Control Logic Servicing Diagram



NOTES: 1. ANY OTHER SWITCH IS DEFINED AS REGISTER SELECT SWITCHES: B, P, M, S, OR MEMORY DATA; OR OPERATION MODE SWITCHES: RUN, INSTR STEP, OR HALT/ CYCLE.
2. STORE AND IOI SIGNALS ARE INHIBITED IF A-REGISTER WAS SELECTED PREVIOUSLY.
3. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTERS "I" AND "O" ARE NOT USED).

2133-43

Figure 4-66. A Switch Timing Diagram

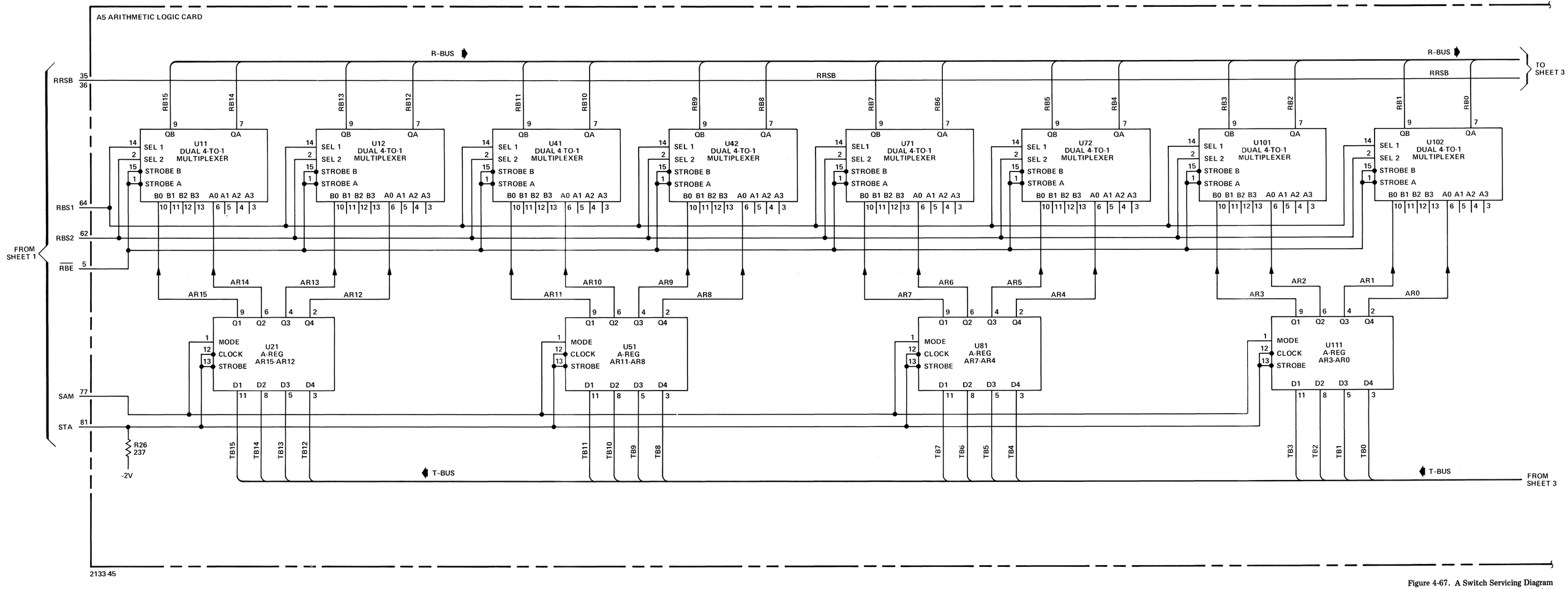


NOTES:

1. TEST POINTS ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.
2. REFER TO TYPICAL DISPLAY REGISTER SWITCH SERVICING DIAGRAM FOR COMPLETE SWITCH AND DISPLAY REGISTER LOGIC.

2133-44

Figure 4-67. A Switch Servicing Diagram (Sheet 1 of 4)



2133-45

Figure 4-67. A Switch Servicing Diagram (Sheet 2 of 4)

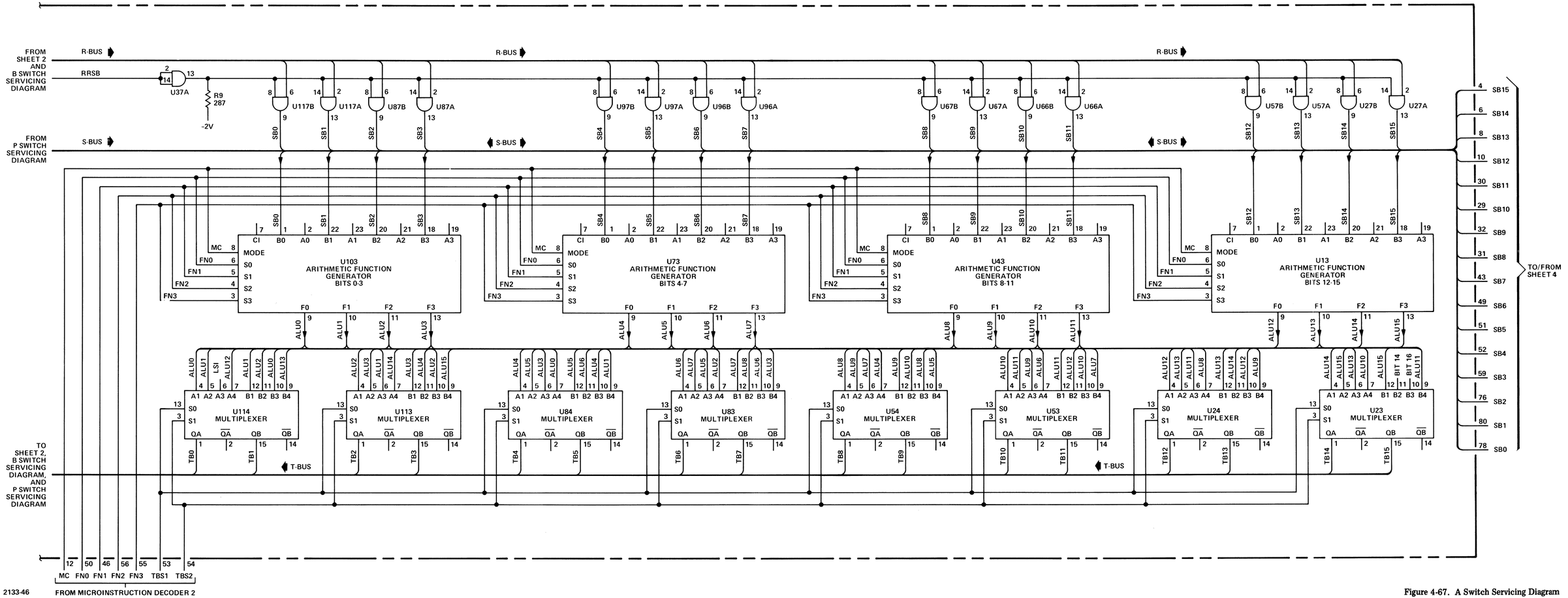


Figure 4-67. A Switch Servicing Diagram (Sheet 3 of 4)

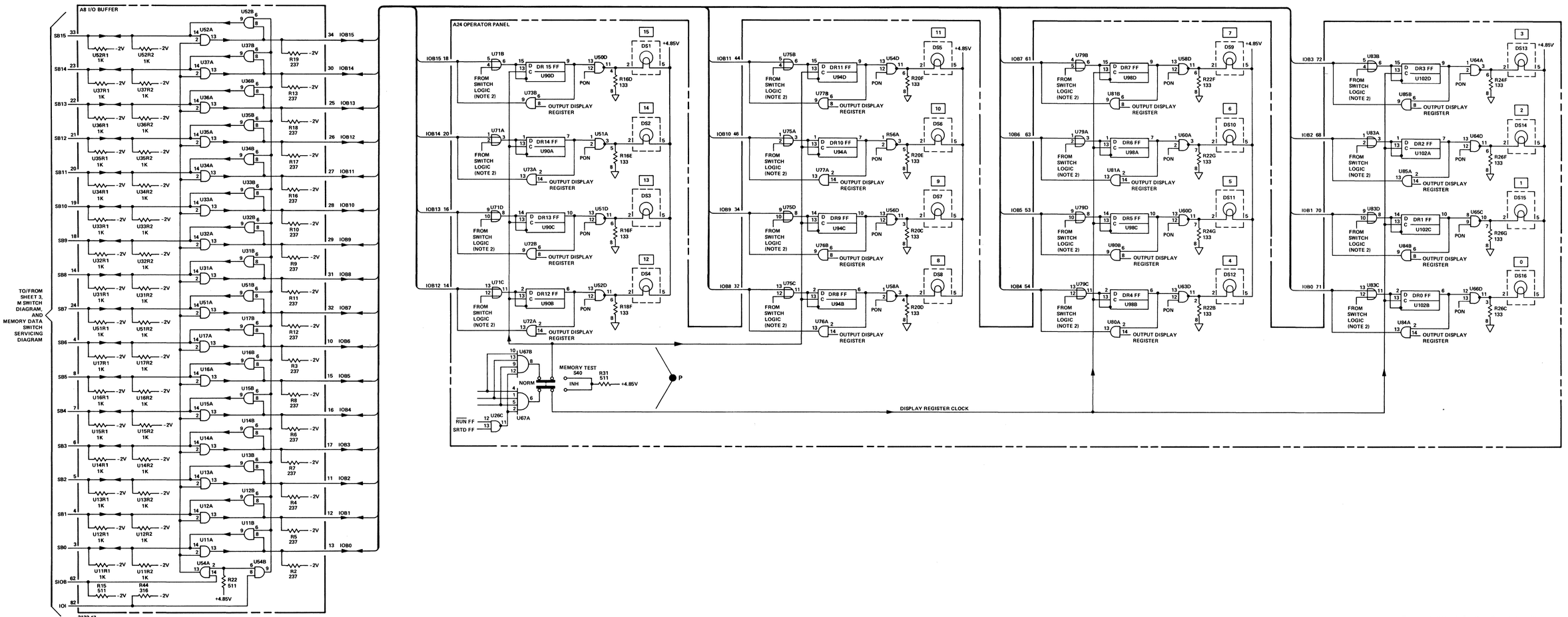
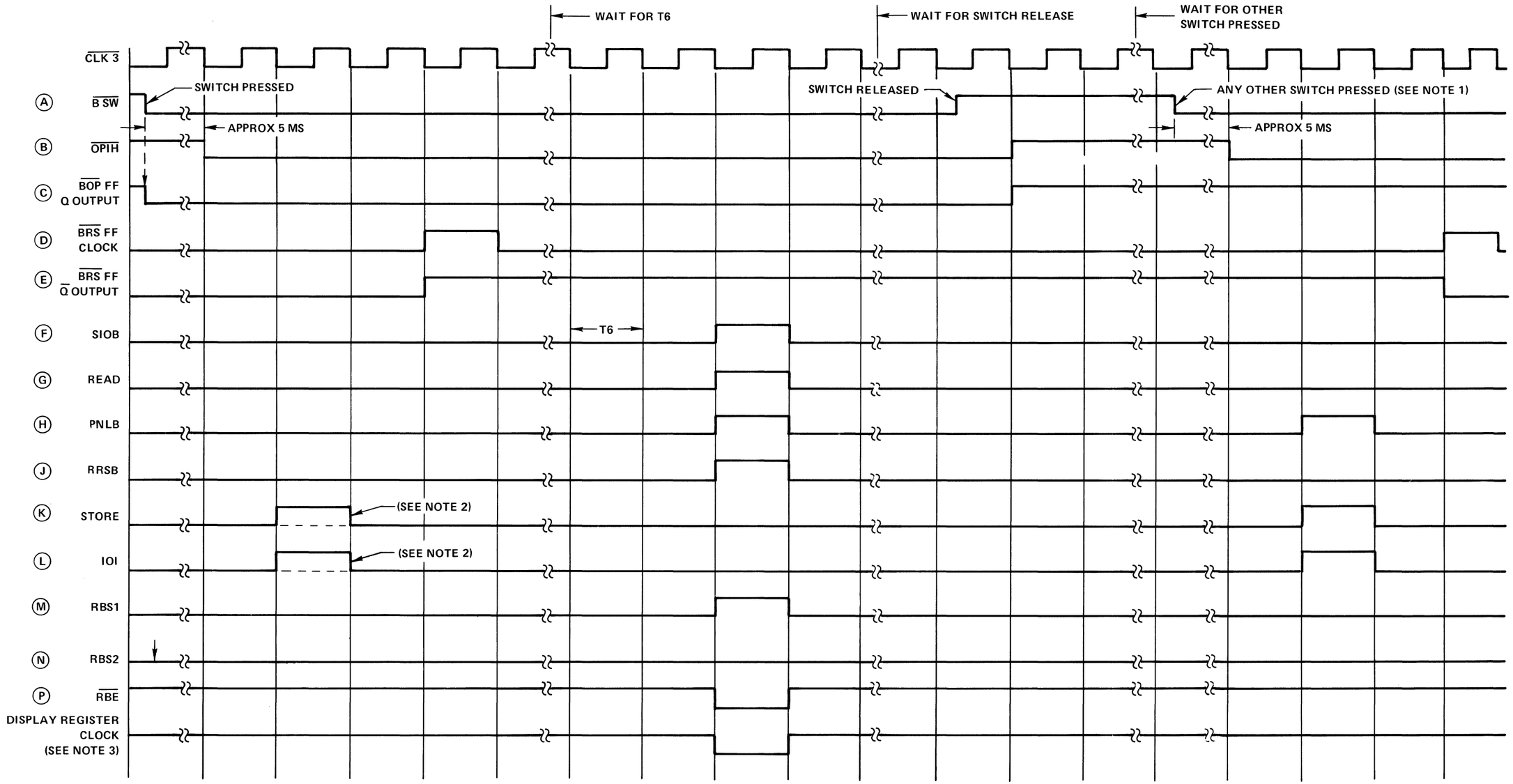


Figure 4-67. A Switch Servicing Diagram (Sheet 4 of 4)



NOTES: 1. ANY OTHER SWITCH IS DEFINED AS REGISTER SELECT SWITCHES: A, P, M, S, OR MEMORY DATA; OR OPERATION MODE SWITCHES: RUN, INSTR STEP, OR HALT/CYCLE.
2. STORE AND IOI SIGNALS ARE INHIBITED IF B-REGISTER WAS SELECTED PREVIOUSLY.
3. DISPLAY REGISTER CLOCK IS SHOWN ON "A" SWITCH SERVICING DIAGRAM (SHEET 4).
4. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTERS "I" AND "O" ARE NOT USED).

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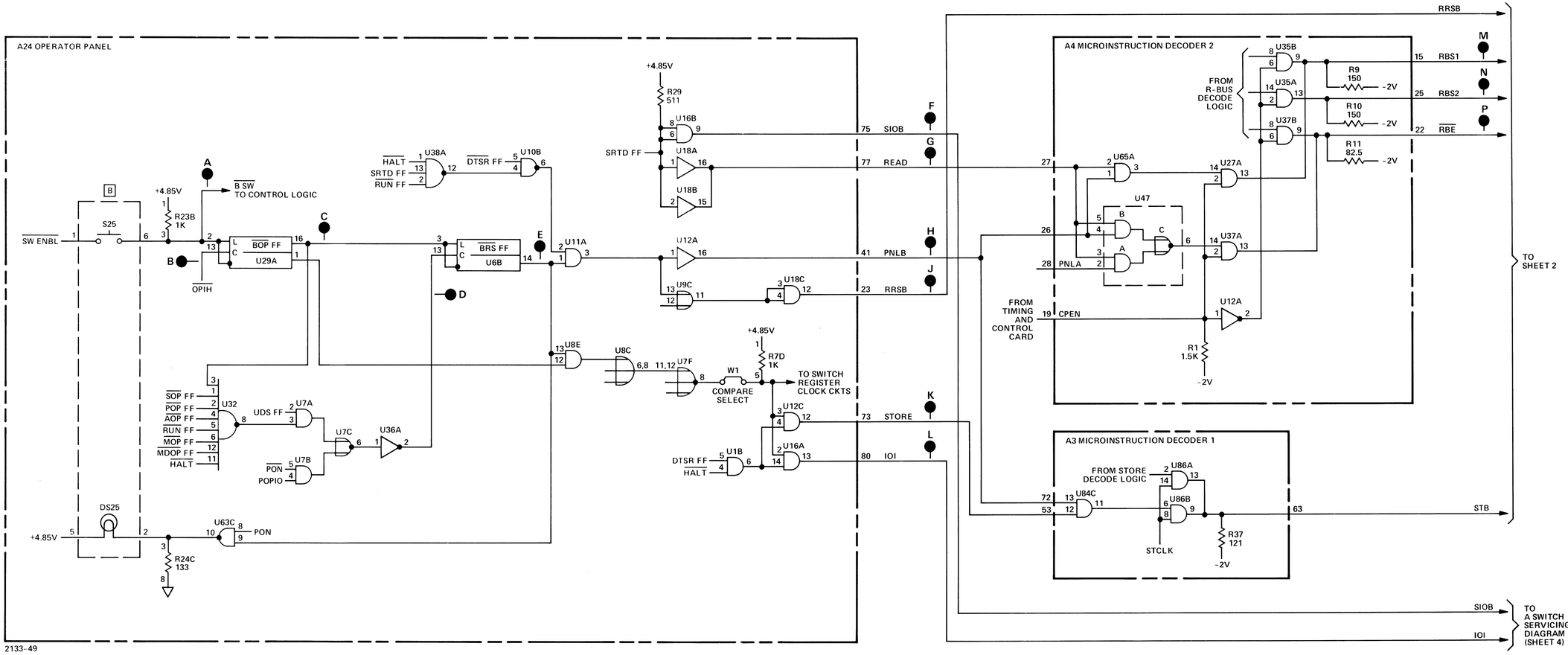
Figure 4-68. B Switch Timing Diagram



NOTES: 1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

Figure 4-69. B Switch Servicing Diagram (Sheet 1 of 2)

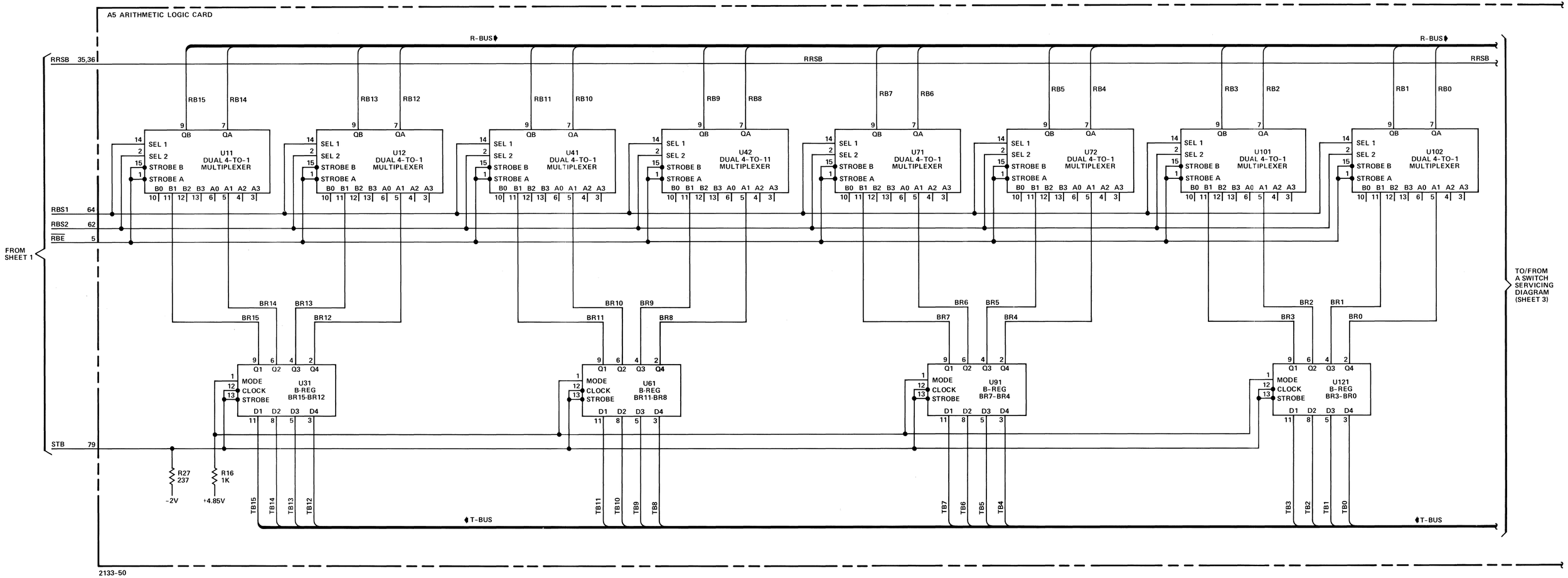
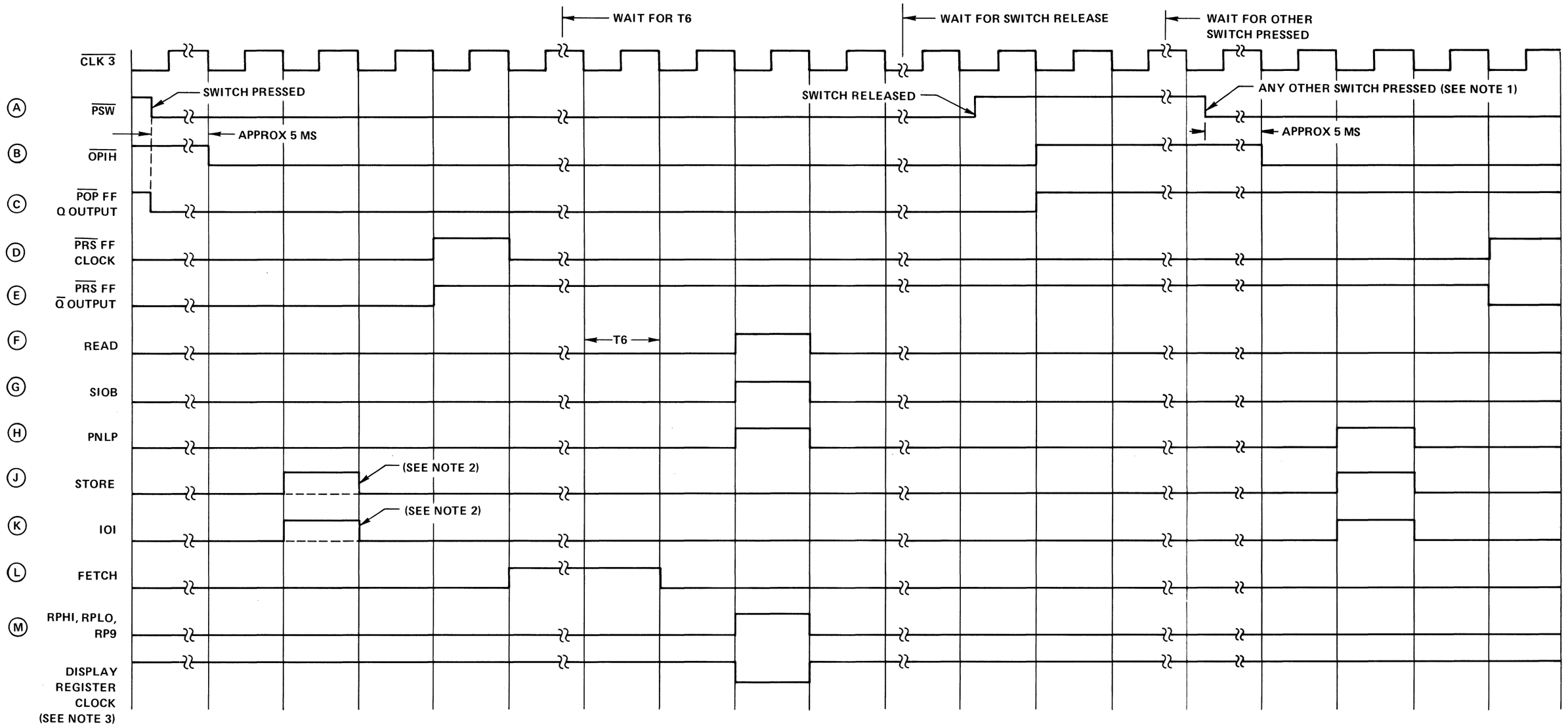


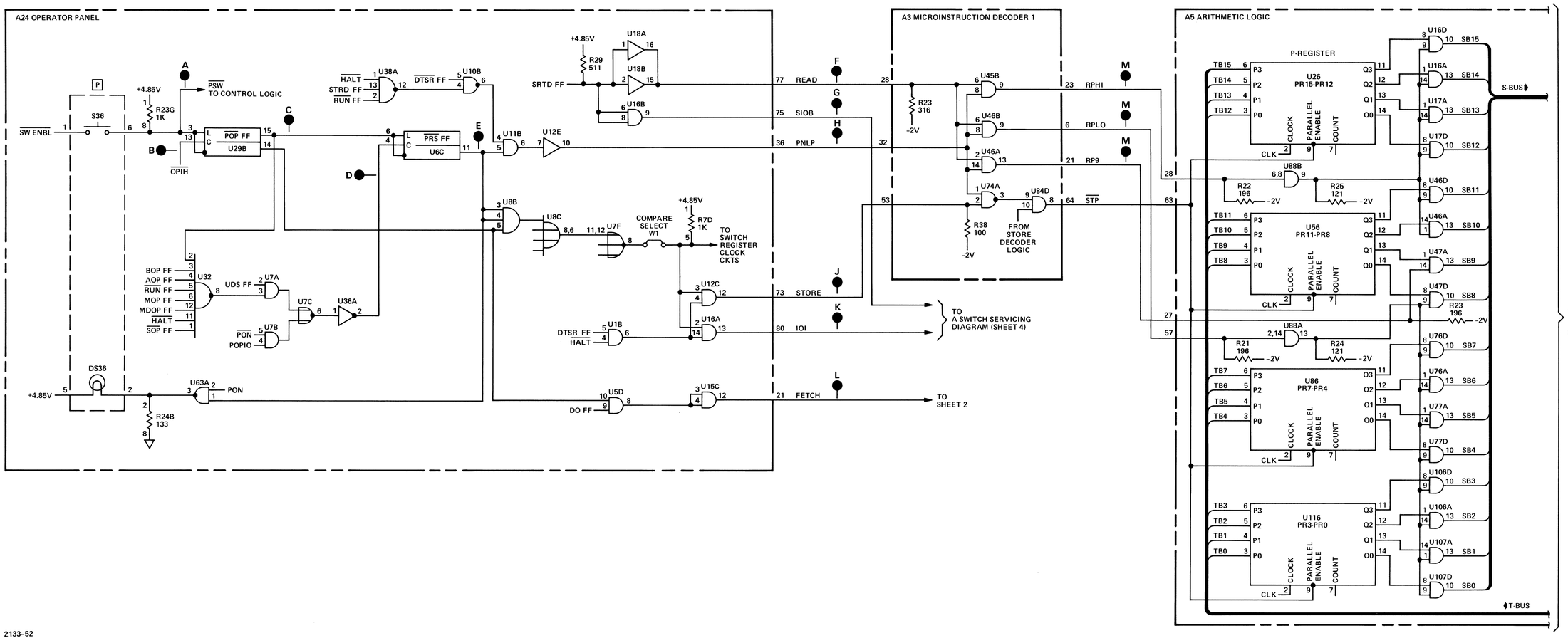
Figure 4-69. B Switch Servicing Diagram (Sheet 2 of 2)



NOTES: 1. ANY OTHER SWITCH IS DEFINED AS REGISTER SELECT SWITCHES: A, B, M, S, OR MEMORY DATA; OR OPERATION MODE SWITCHES: RUN, INSTR STEP, OR HALT/CYCLE.
2. STORE AND IOI SIGNALS ARE INHIBITED IF P-REGISTER WAS SELECTED PREVIOUSLY.
3. DISPLAY REGISTER CLOCK SIGNAL IS SHOWN ON "A" SWITCH SERVICING DIAGRAM (SHEET 4).
4. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

2133-51

Figure 4-70. P Switch Timing Diagram



NOTES:

1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-52

Figure 4-71. P Switch Servicing Diagram (Sheet 1 of 2)

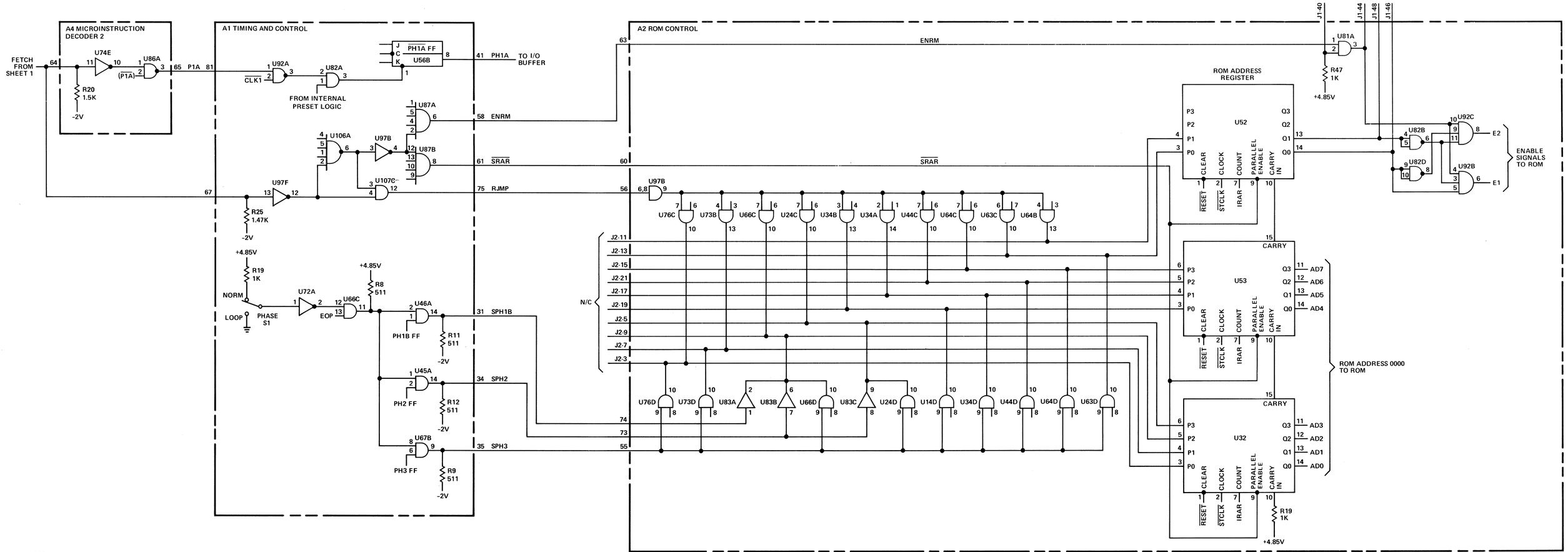
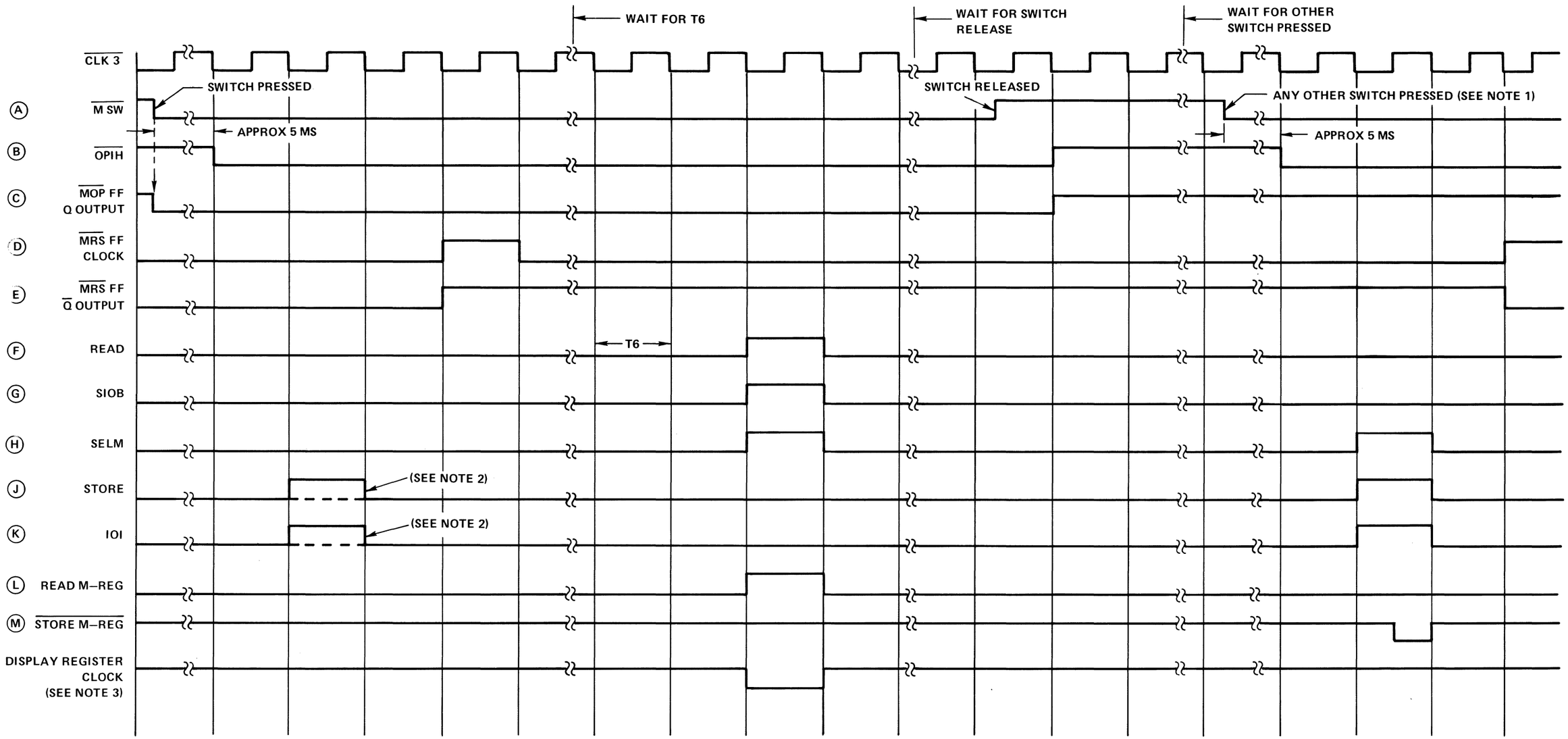


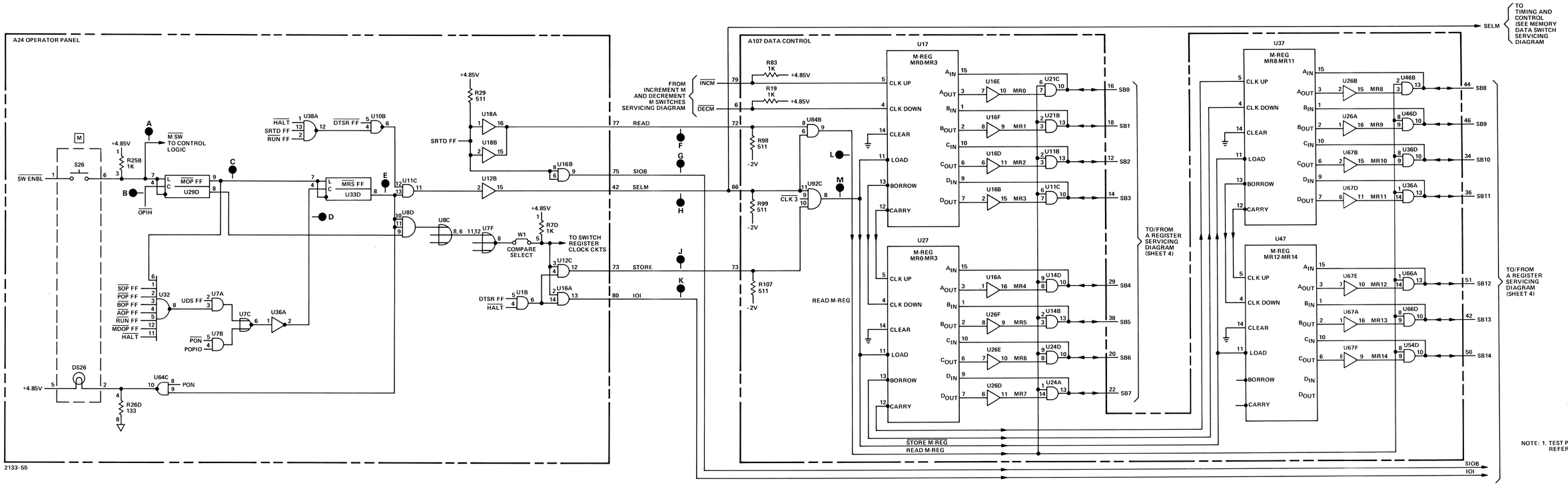
Figure 4-71. P Switch Servicing Diagram (Sheet 2 of 2)



NOTES: 1. ANY OTHER SWITCH IS DEFINED AS REGISTER SELECT SWITCHES: A, B, P, S, OR MEMORY DATA; OR OPERATIONAL MODE SWITCHES: RUN, INSTR STEP, OR HALT/CYCLE.
2. STORE AND IOI SIGNALS ARE INHIBITED IF M–REGISTER WAS SELECTED PREVIOUSLY.
3. DISPLAY REGISTER CLOCK SIGNAL IS SHOWN ON "A" SWITCH SERVICING DIAGRAM (SHEET 4).
4. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

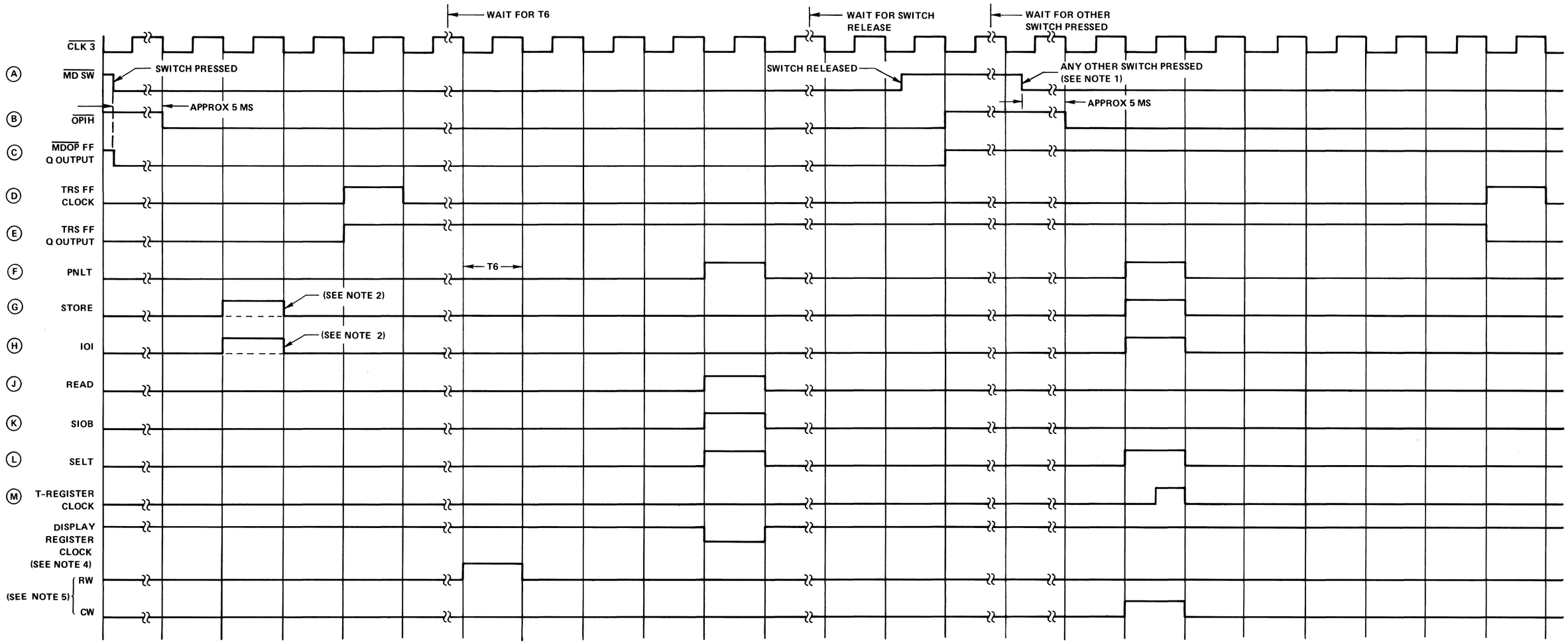
2133-54

Figure 4-72. M Switch Timing Diagram



NOTE: 1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

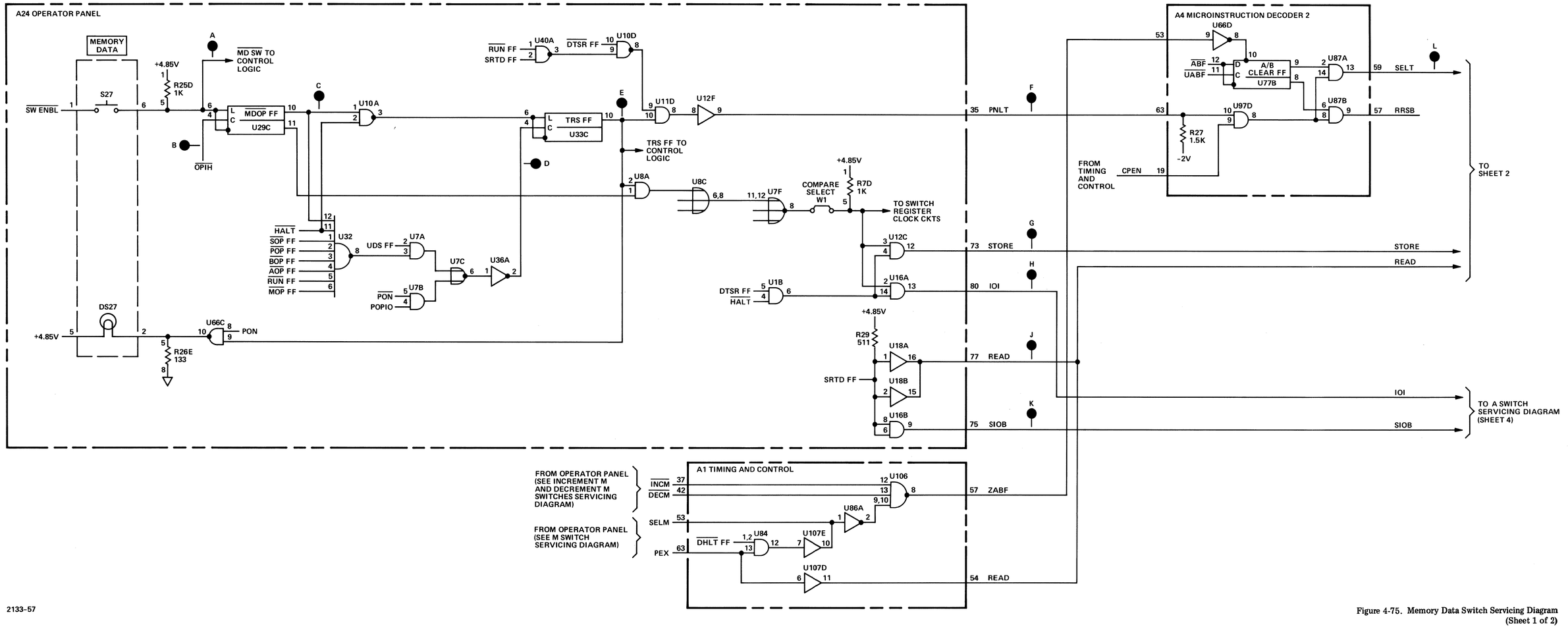
Figure 4-73. M Switch Servicing Diagram



NOTES: 1. ANY OTHER SWITCH IS DEFINED AS REGISTER SELECT SWITCHES: A, B, P, M, OR S; OR OPERATIONAL MODE SWITCHES: RUN, INSTR STEP, OR HALT/CYCLE.
2. STORE AND IOI SIGNALS ARE INHIBITED IF T-REGISTER (MEMORY DATA) WAS SELECTED PREVIOUSLY.
3. FOR ADDITIONAL OPERATOR PANEL CONTROL LOGIC TIMING, SEE FIG. 4-11.
4. DISPLAY REGISTER CLOCK SIGNAL IS SHOWN ON "A" SWITCH SERVICING DIAGRAM (SHEET 4).
5. RW AND CW SIGNALS ARE SHOWN ON OPERATOR PANEL CONTROL LOGIC SERVICING DIAGRAM.
6. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

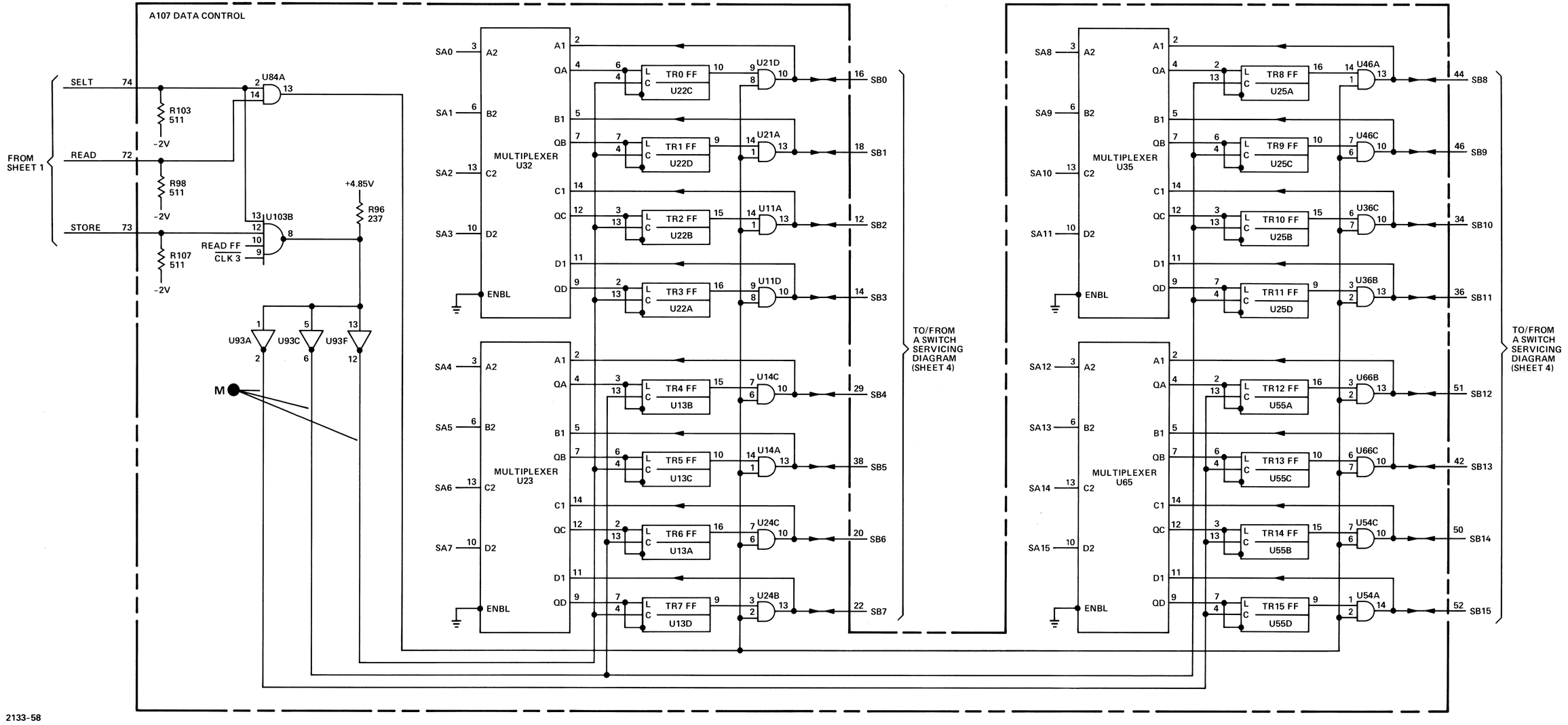
2133-56

Figure 4-74. Memory Data Switch Timing Diagram



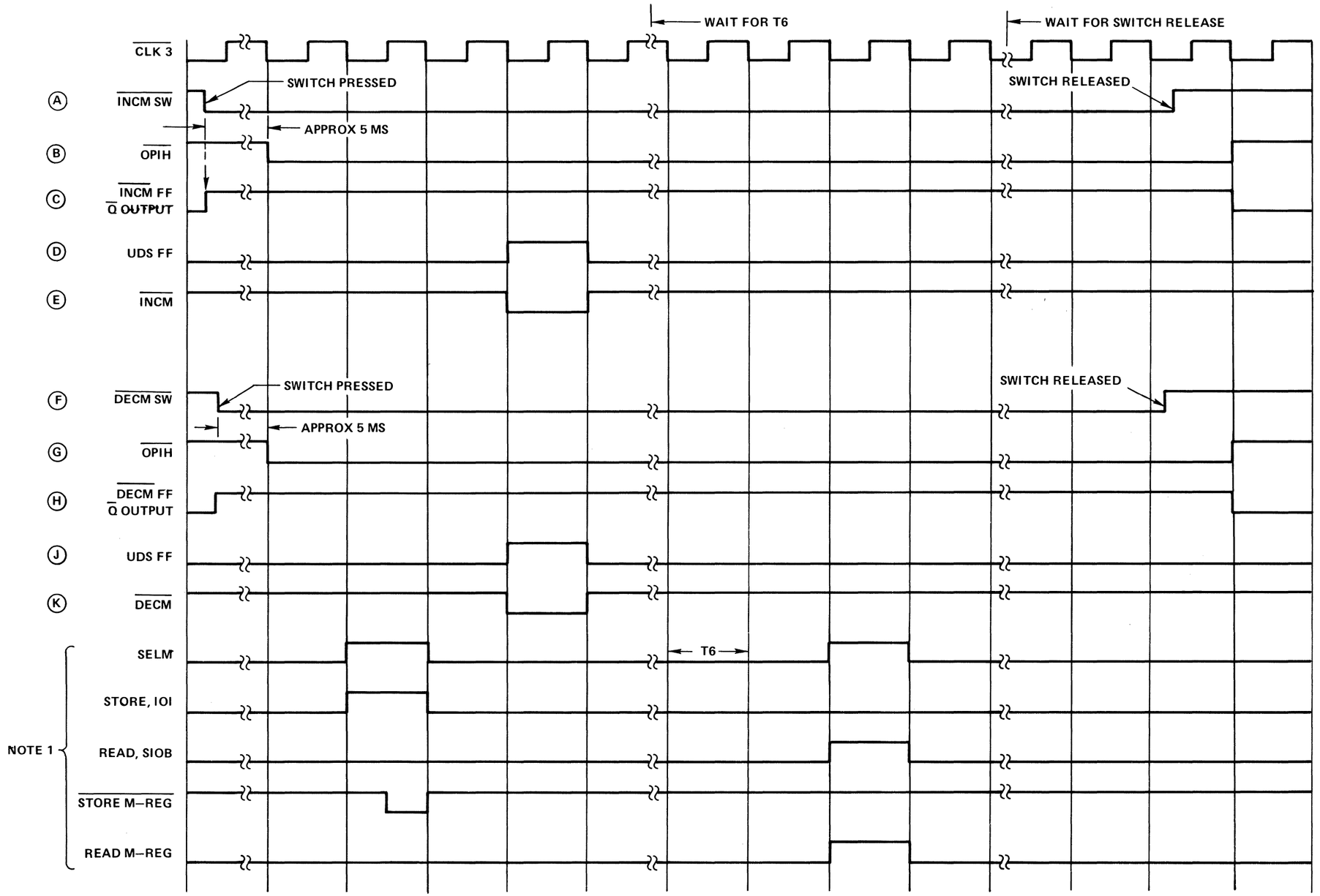
2133-57

Figure 4-75. Memory Data Switch Servicing Diagram (Sheet 1 of 2)



2133-58

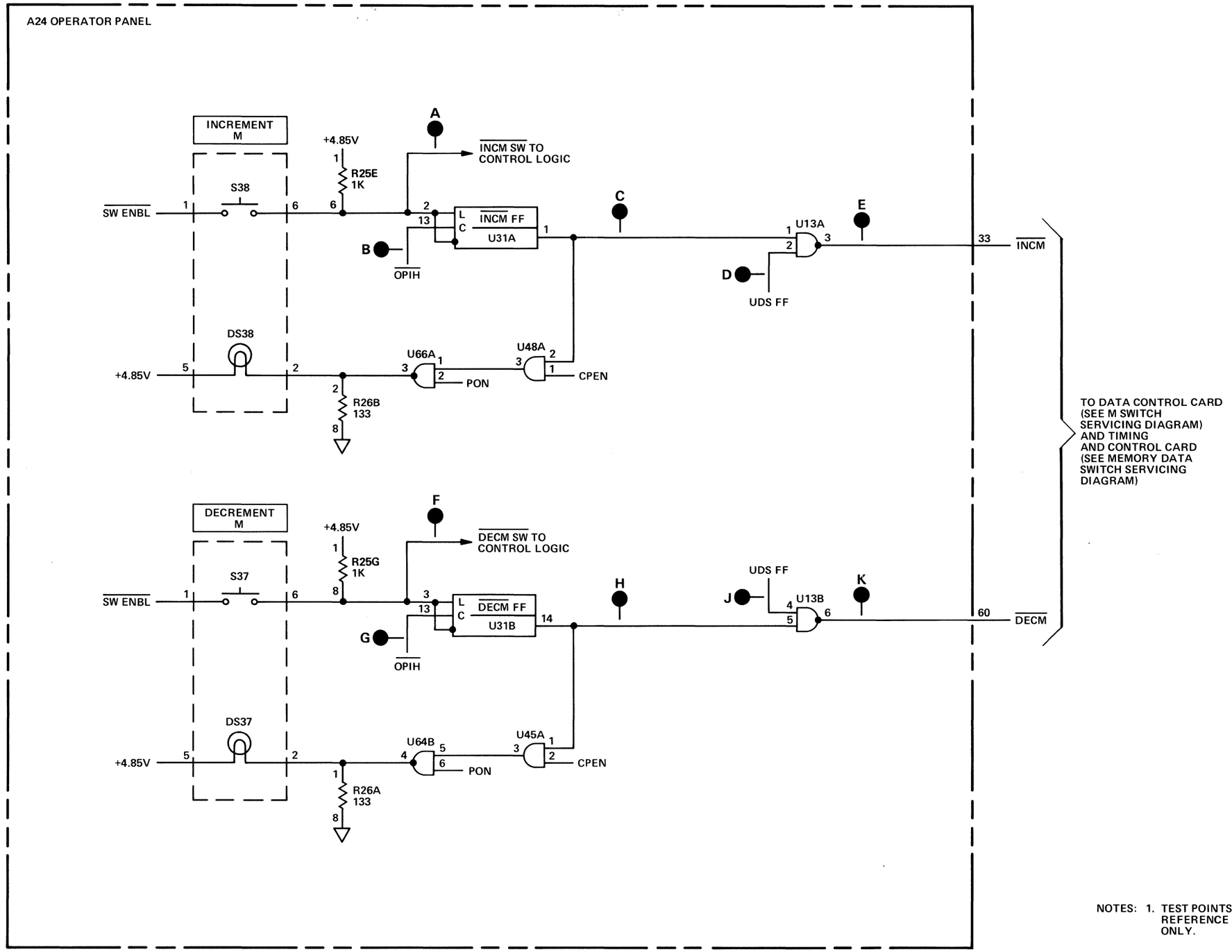
Figure 4-75. Memory Data Switch Servicing Diagram (Sheet 2 of 2)



NOTES: 1. THESE SIGNALS ARE LOCATED ON THE M SWITCH SERVICING DIAGRAM.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

2133-59

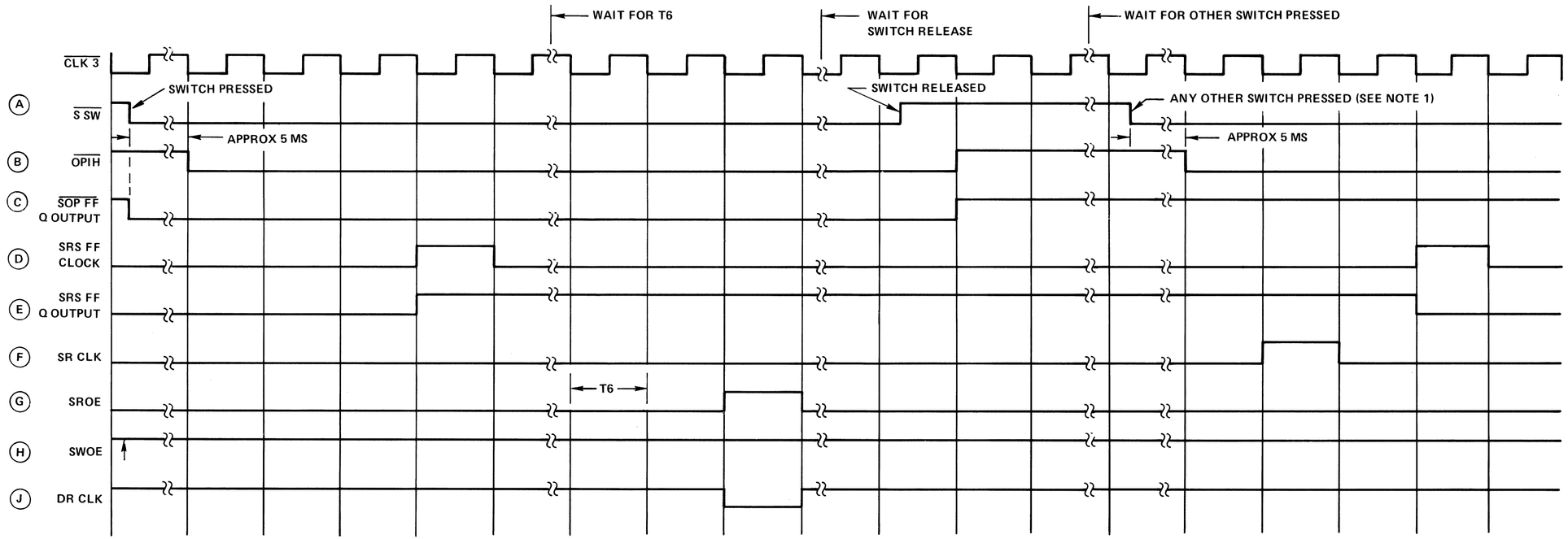
Figure 4-76. Increment M and Decrement M Switches Timing Diagram



2133-60

NOTES: 1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

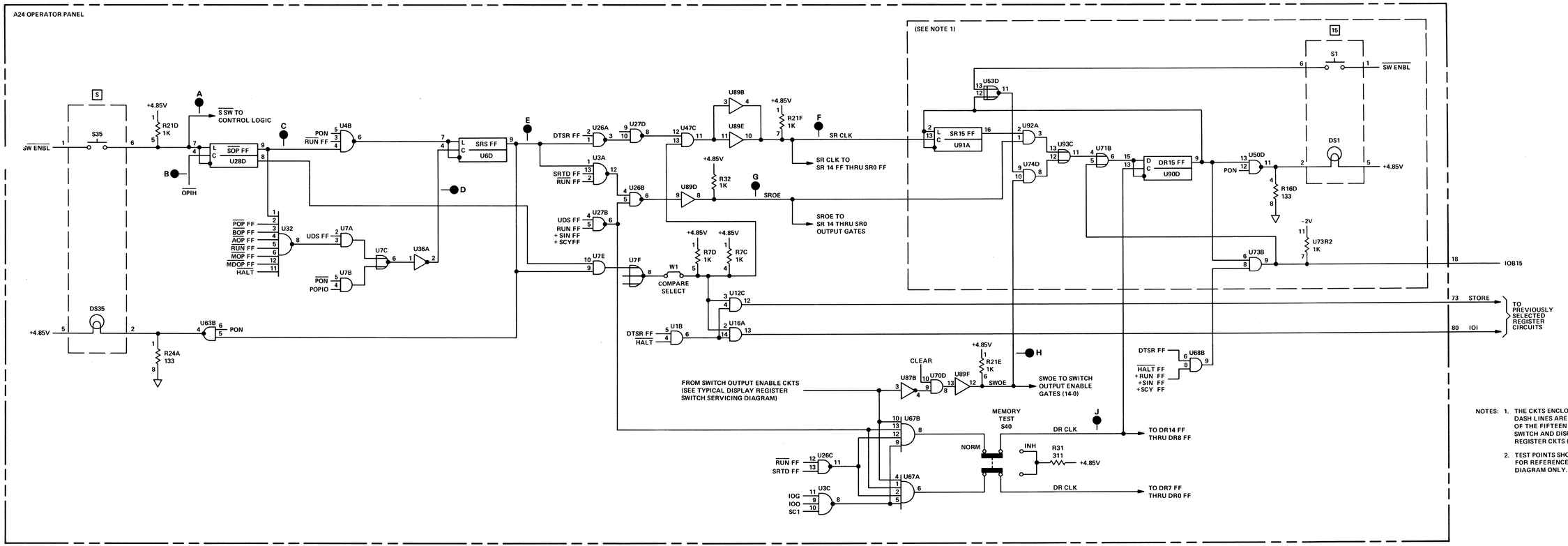
Figure 4-77. Increment M and Decrement M Switches Servicing Diagram



NOTES:
1. ANY OTHER SWITCH IS DEFINED AS REGISTER SELECT SWITCHES: A, B, P, M, OR MEMORY DATA; OR OPERATIONAL MODE SWITCHES: RUN, INSTR STEP, OR HALT/CYCLE.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

2133-61

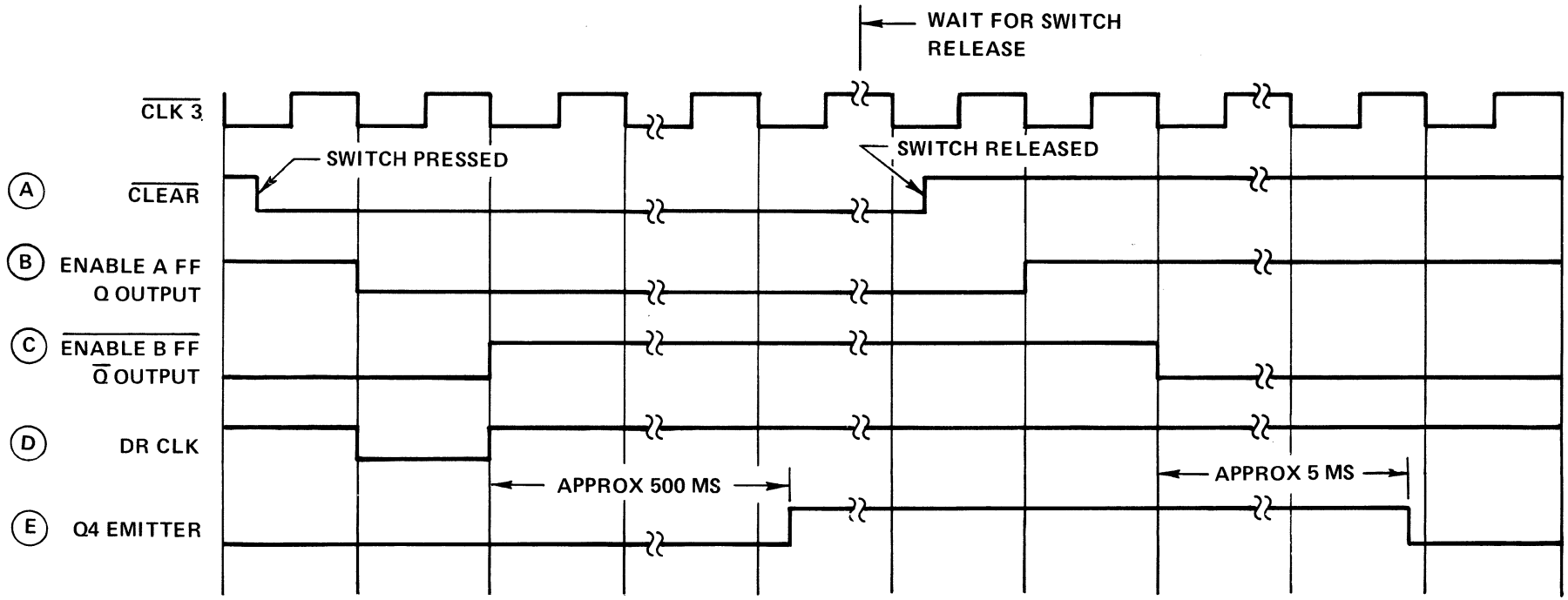
Figure 4-78. S Switch Timing Diagram



NOTES:
1. THE CKTS ENCLOSED IN DASH LINES ARE TYPICAL OF THE FIFTEEN OTHER SWITCH AND DISPLAY REGISTER CKTS (14-0).
2. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-62

Figure 4-79. S Switch Servicing Diagram



NOTES: 1. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM.

2133-63

Figure 4-80. Clear Display Switch Timing Diagram

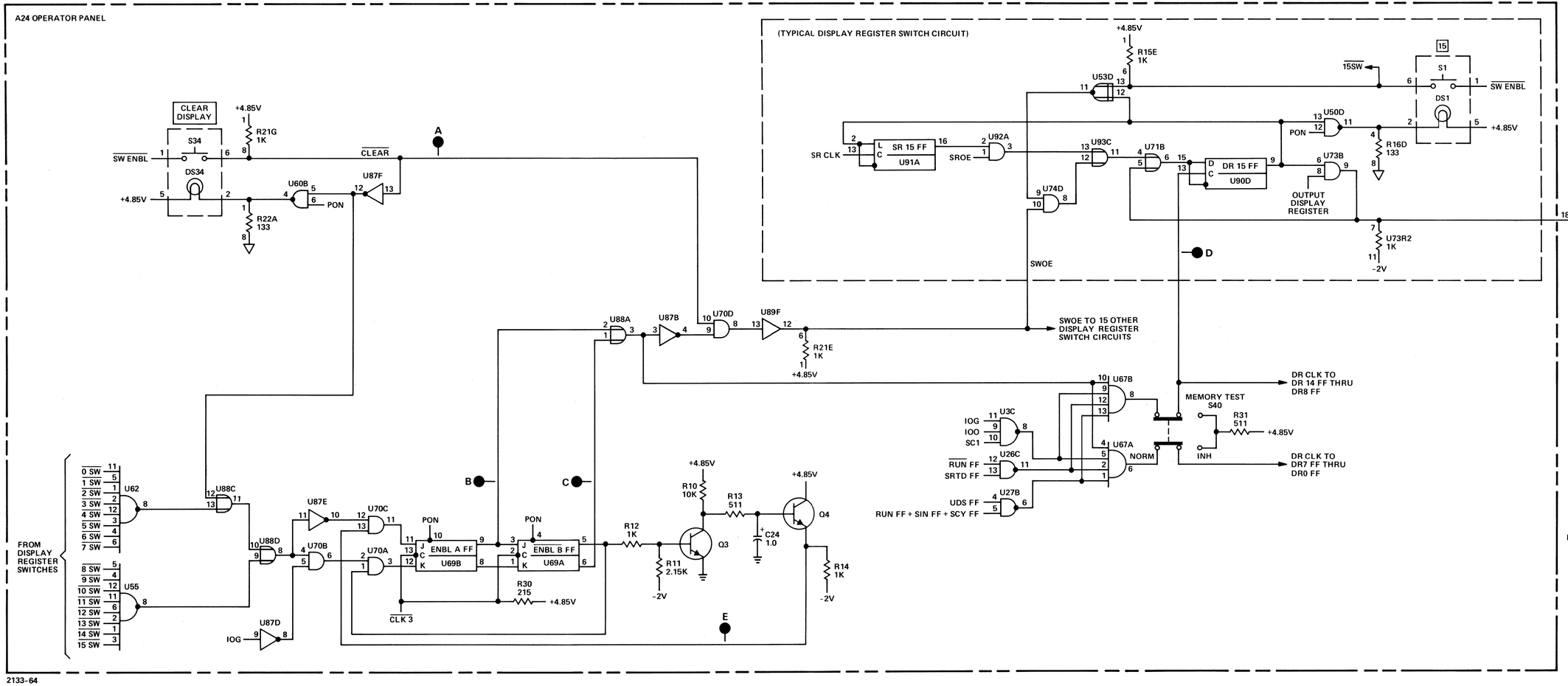
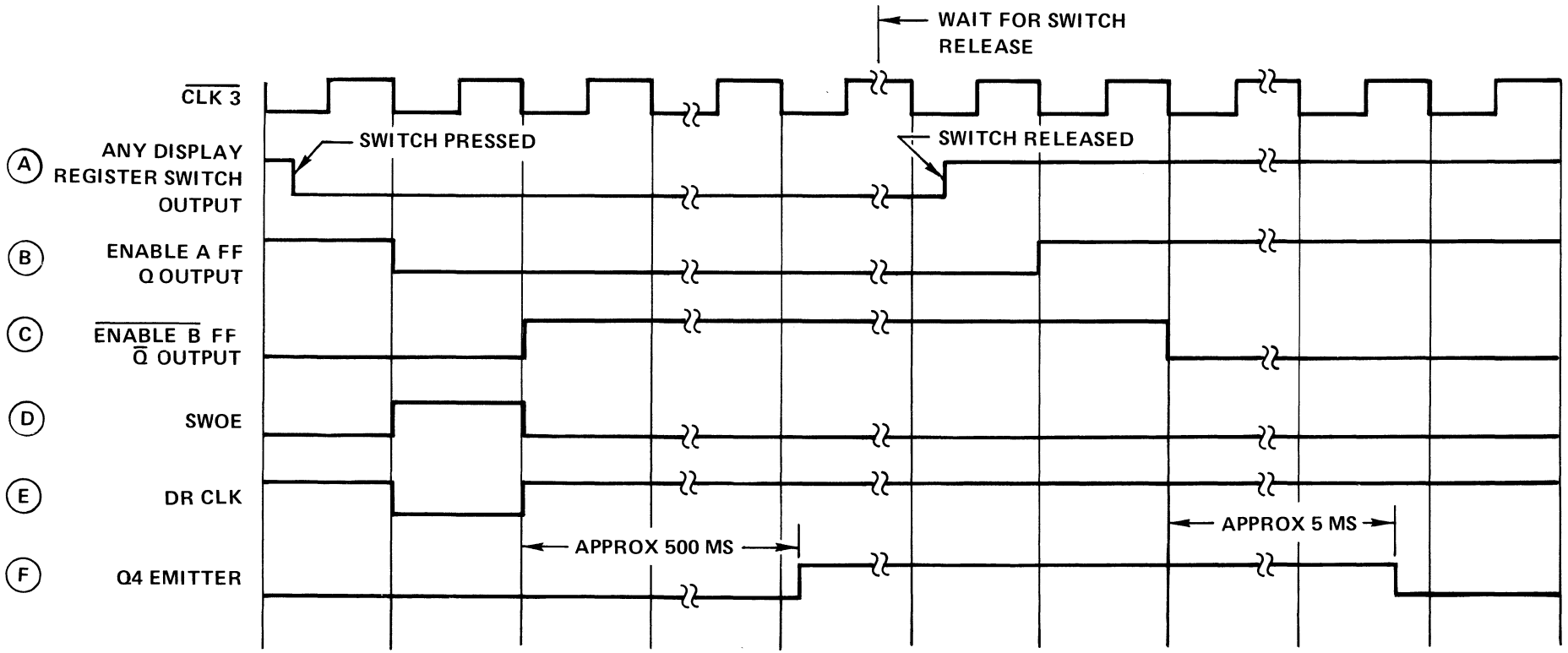


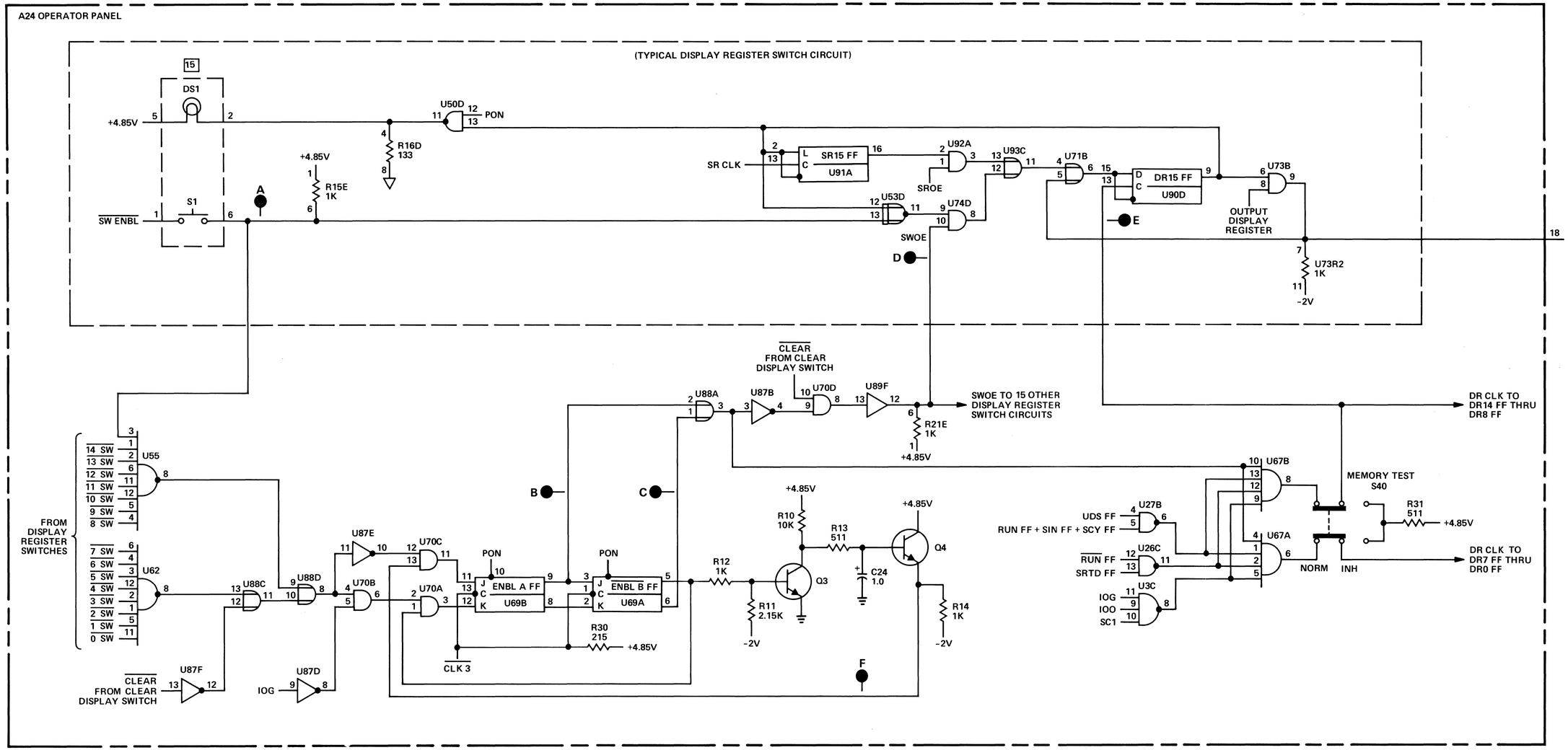
Figure 4-81. Clear Display Switch Servicing Diagram



NOTES: 1. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM.

2133-65

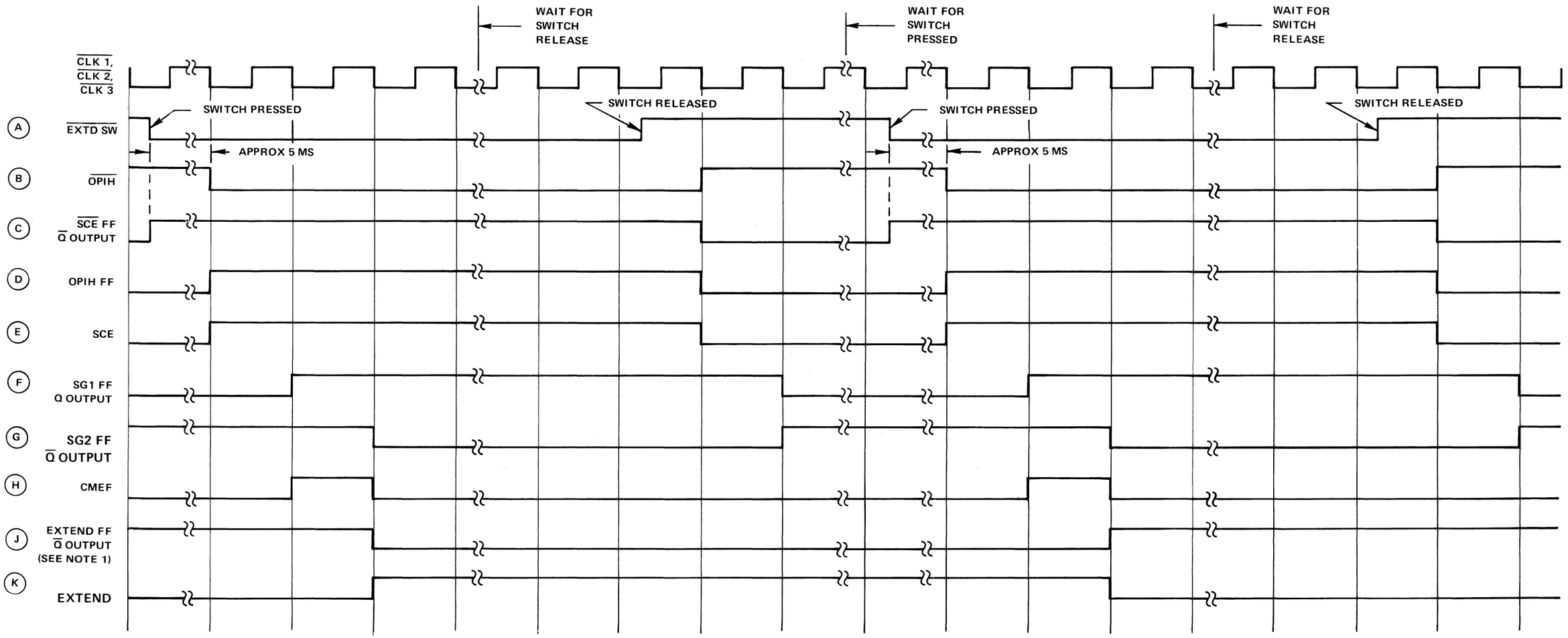
Figure 4-82. Typical Display Register Switch Timing Diagram



NOTES: 1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-66

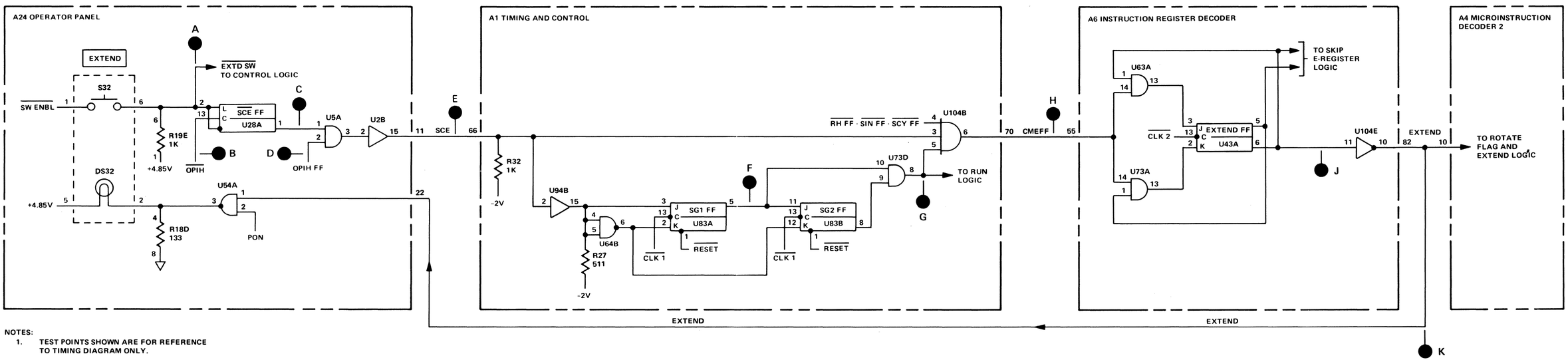
Figure 4-83. Typical Display Register Switch Servicing Diagram



NOTES: 1. ASSUME THAT EXTEND FF IS CLEARED INITIALLY.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

2133-67

Figure 4-84. Extend Switch Timing Diagram

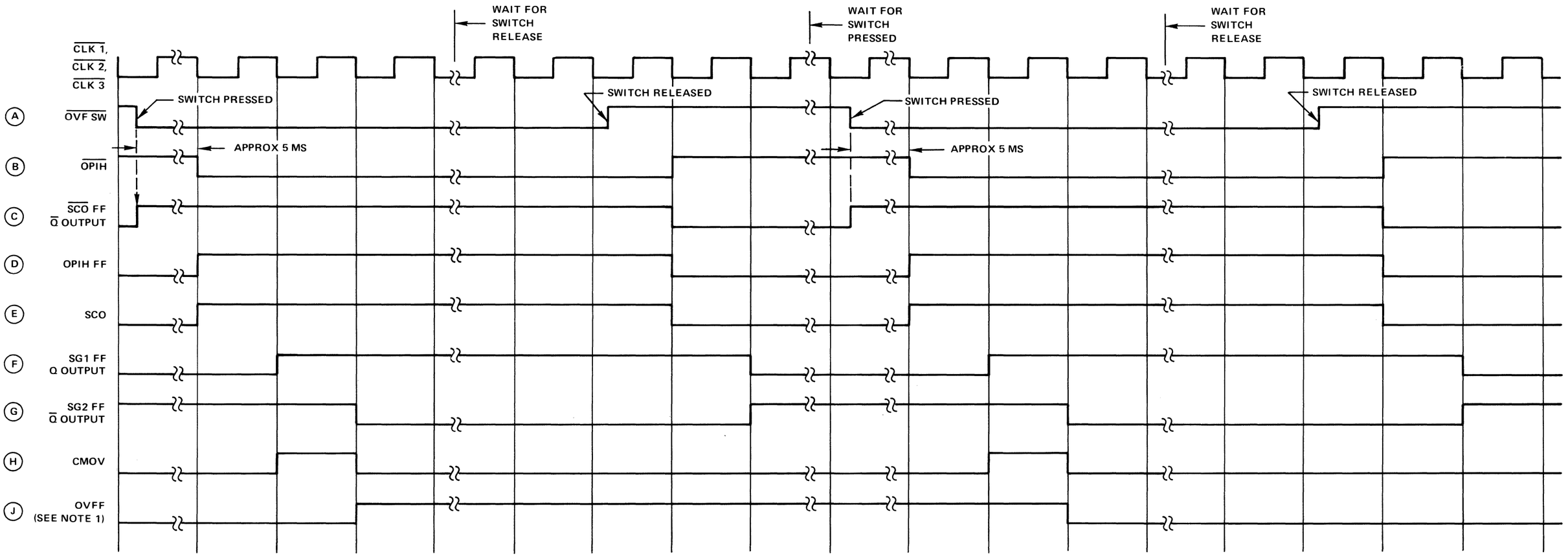


NOTES:

1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-68

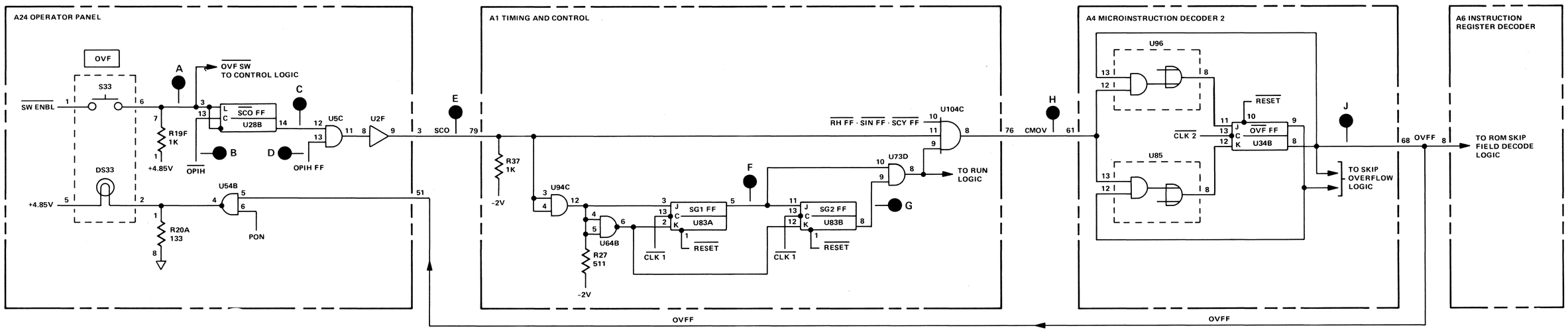
Figure 4-85. Extend Switch Servicing Diagram



NOTES: 1. ASSUME THAT $\overline{\text{OVF}}$ FF IS SET INITIALLY.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

2133-69

Figure 4-86. OVF Switch Timing Diagram

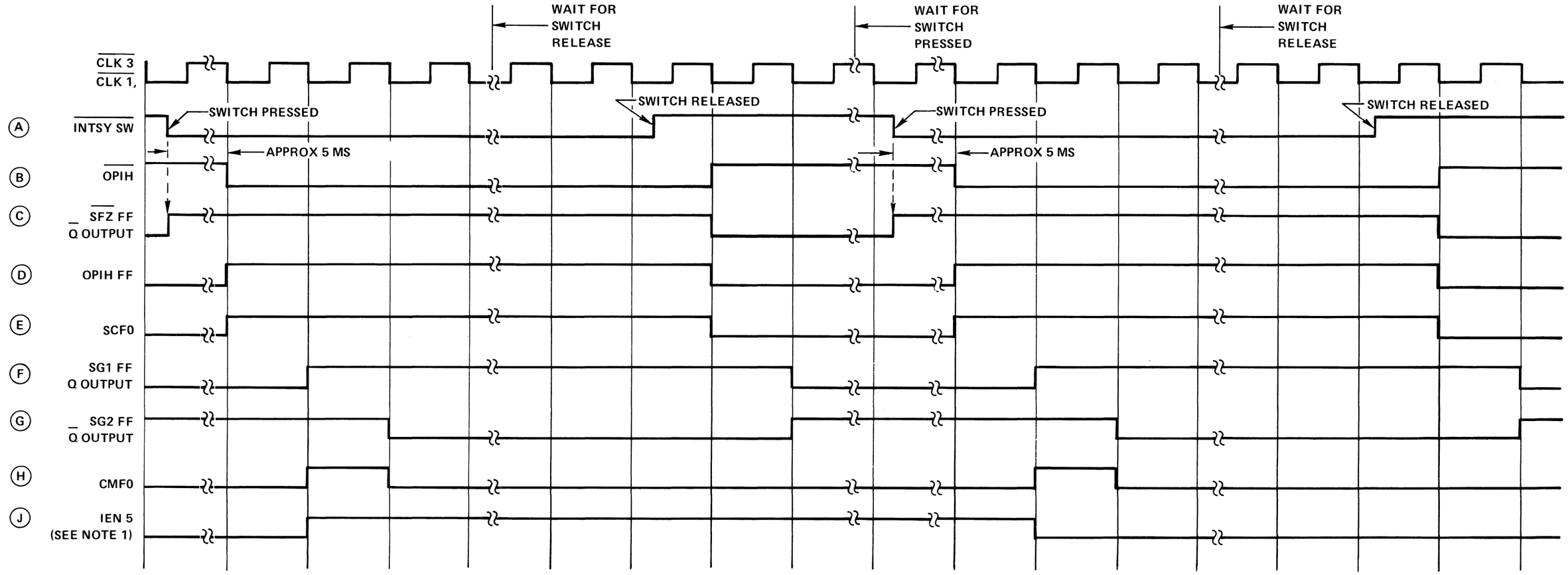


NOTES:

1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-70

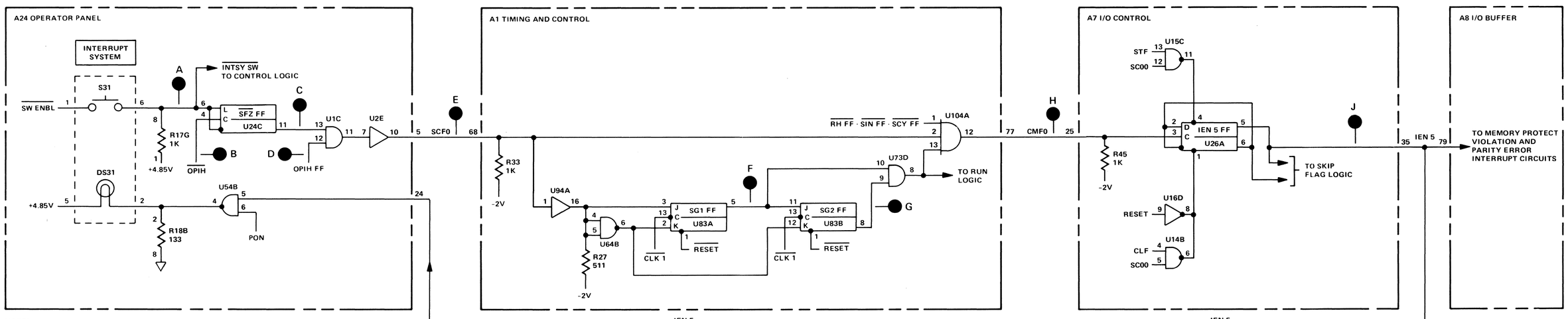
Figure 4-87. OVF Switch Servicing Diagram



NOTES: 1. ASSUME THAT IEN 5 FF IS CLEARED INITIALLY.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTER "I" IS NOT USED).

2133-71

Figure 4-88. Interrupt System Switch Timing Diagram

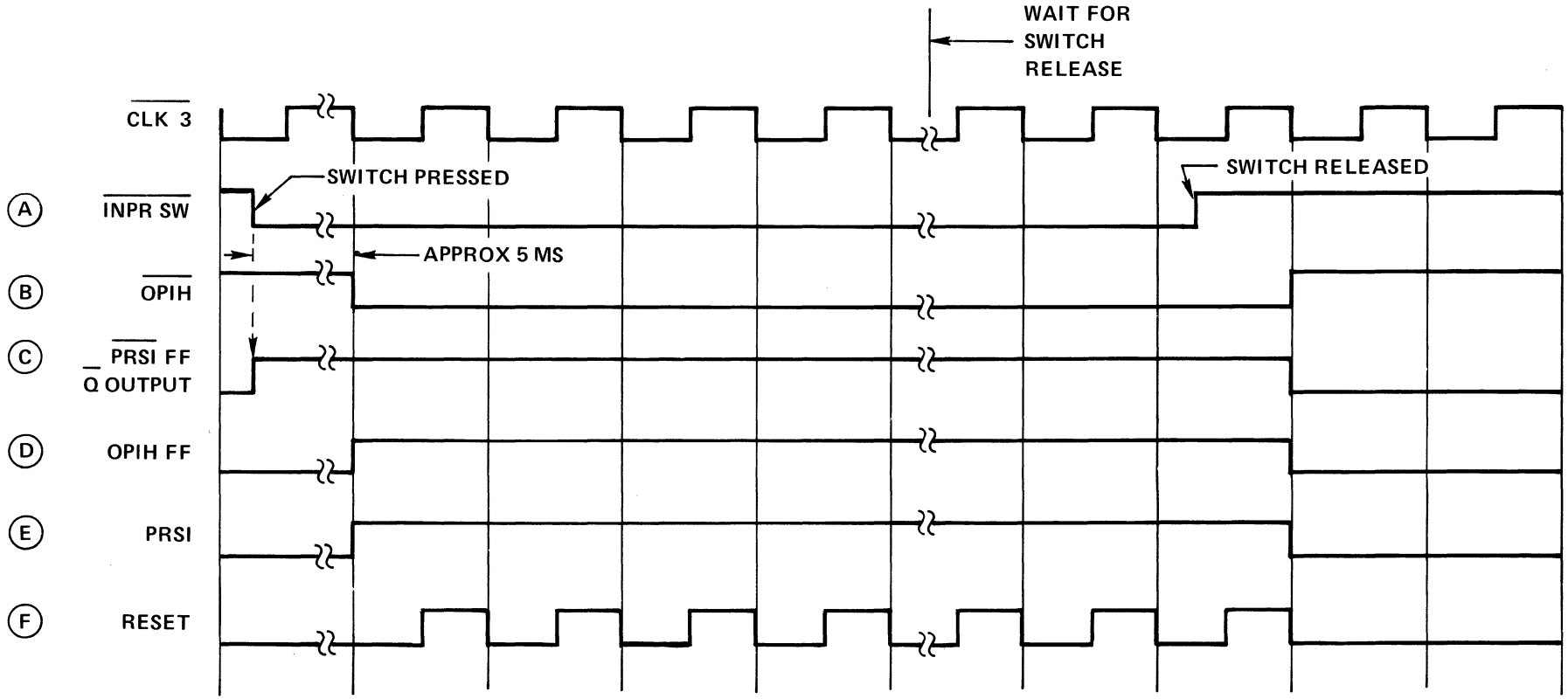


NOTES:

1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-72

Figure 4-89. Interrupt System Switch Servicing Diagram



NOTES: 1. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM.

2133-73

Figure 4-90. Internal Preset Switch Timing Diagram

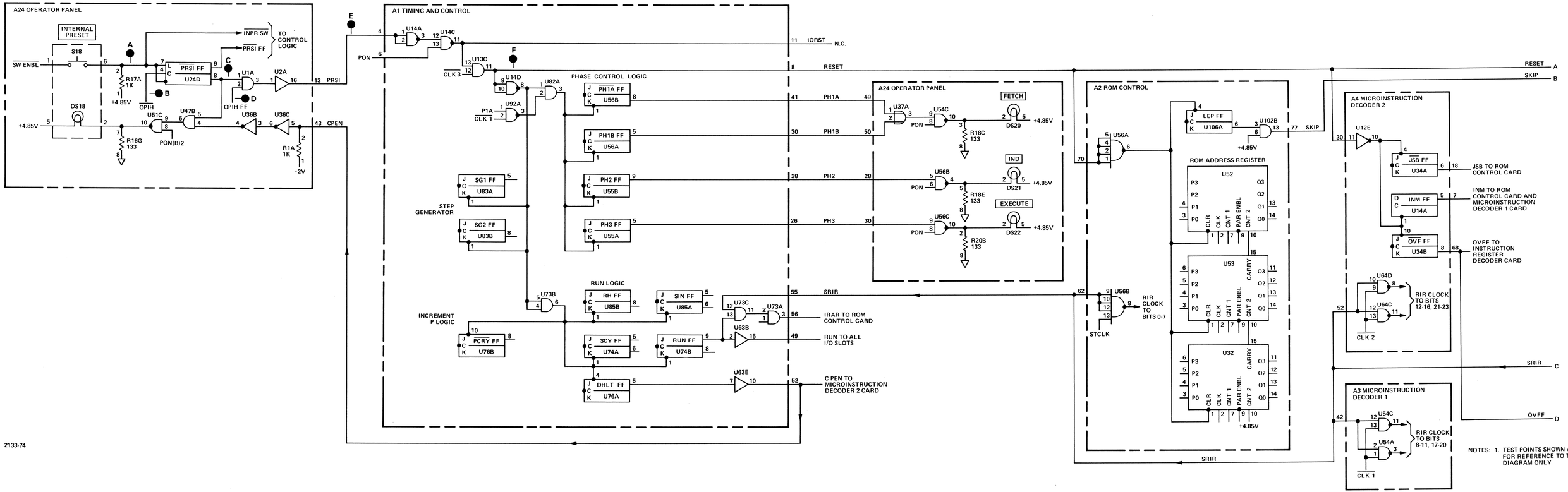


Figure 4-91. Internal Preset Switch Servicing Diagram (Sheet 1 of 2)

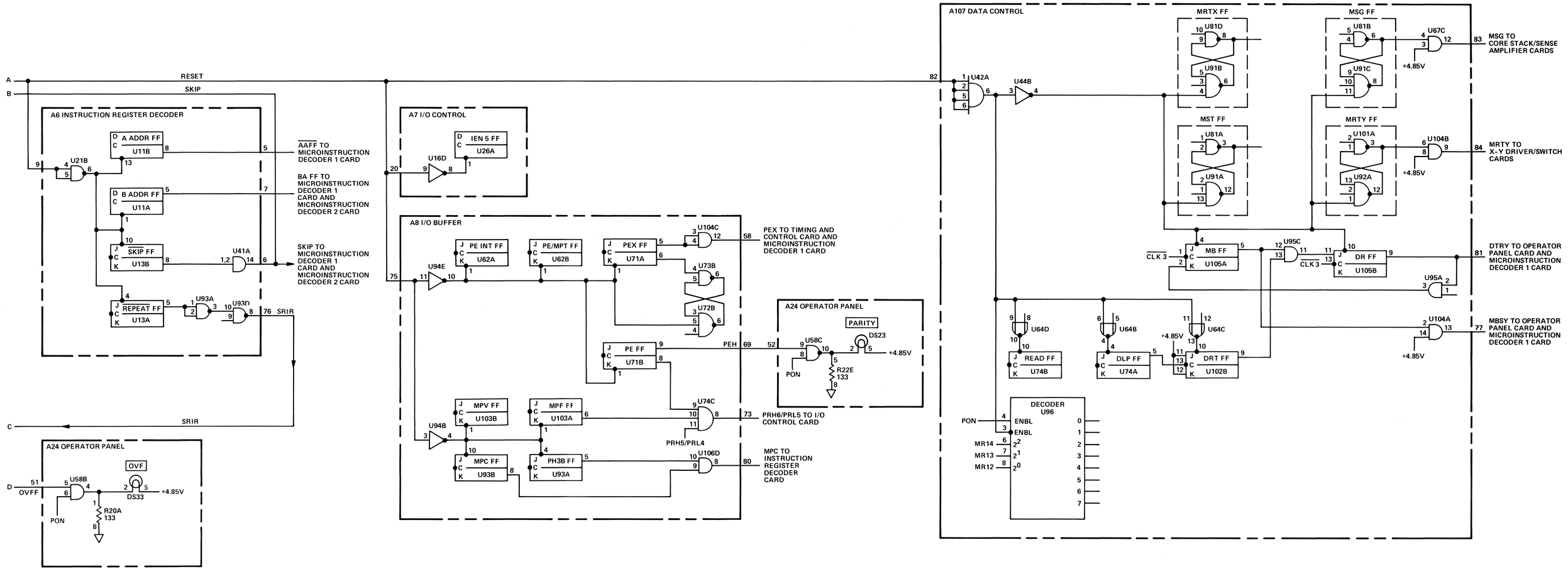
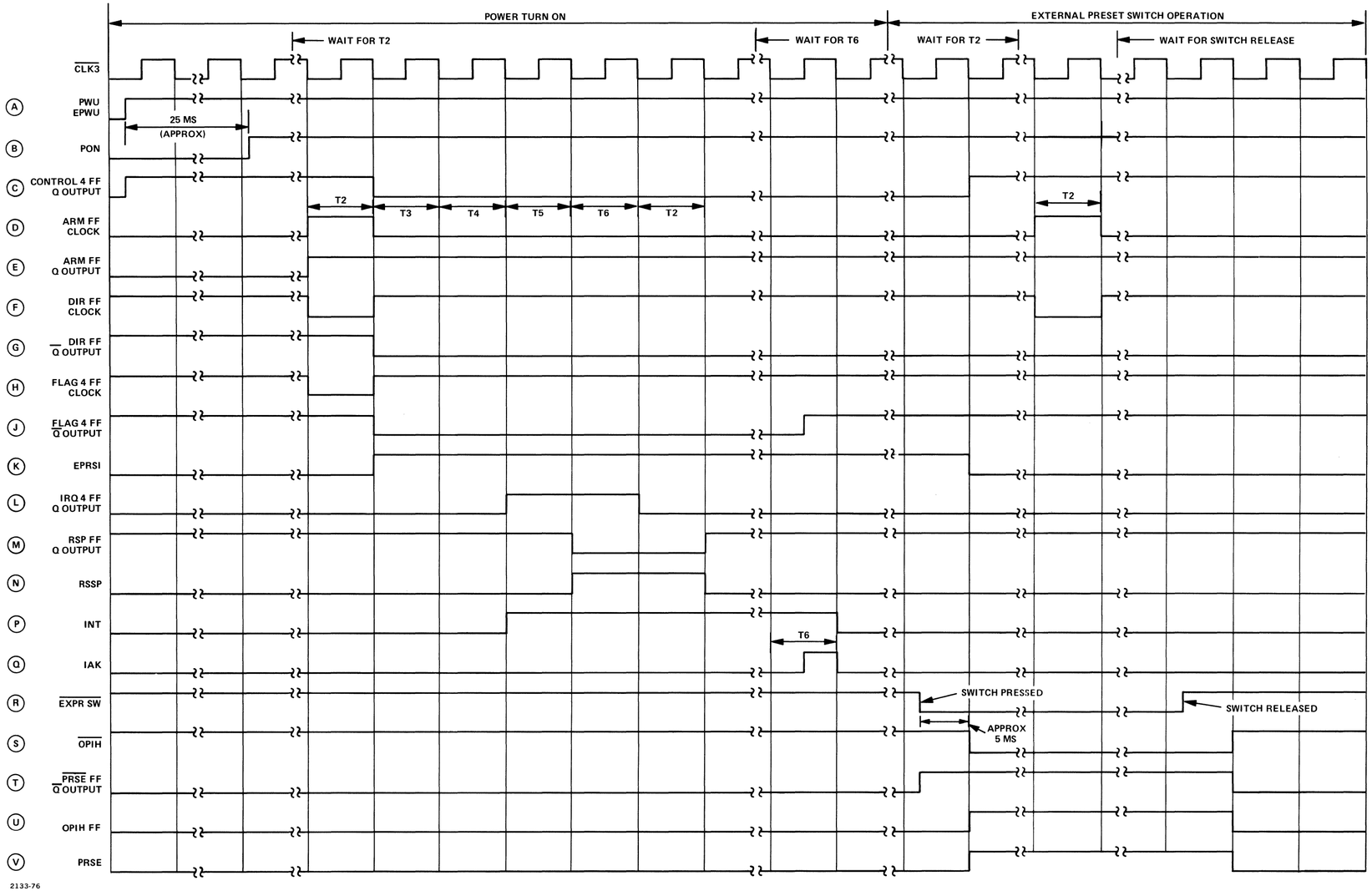


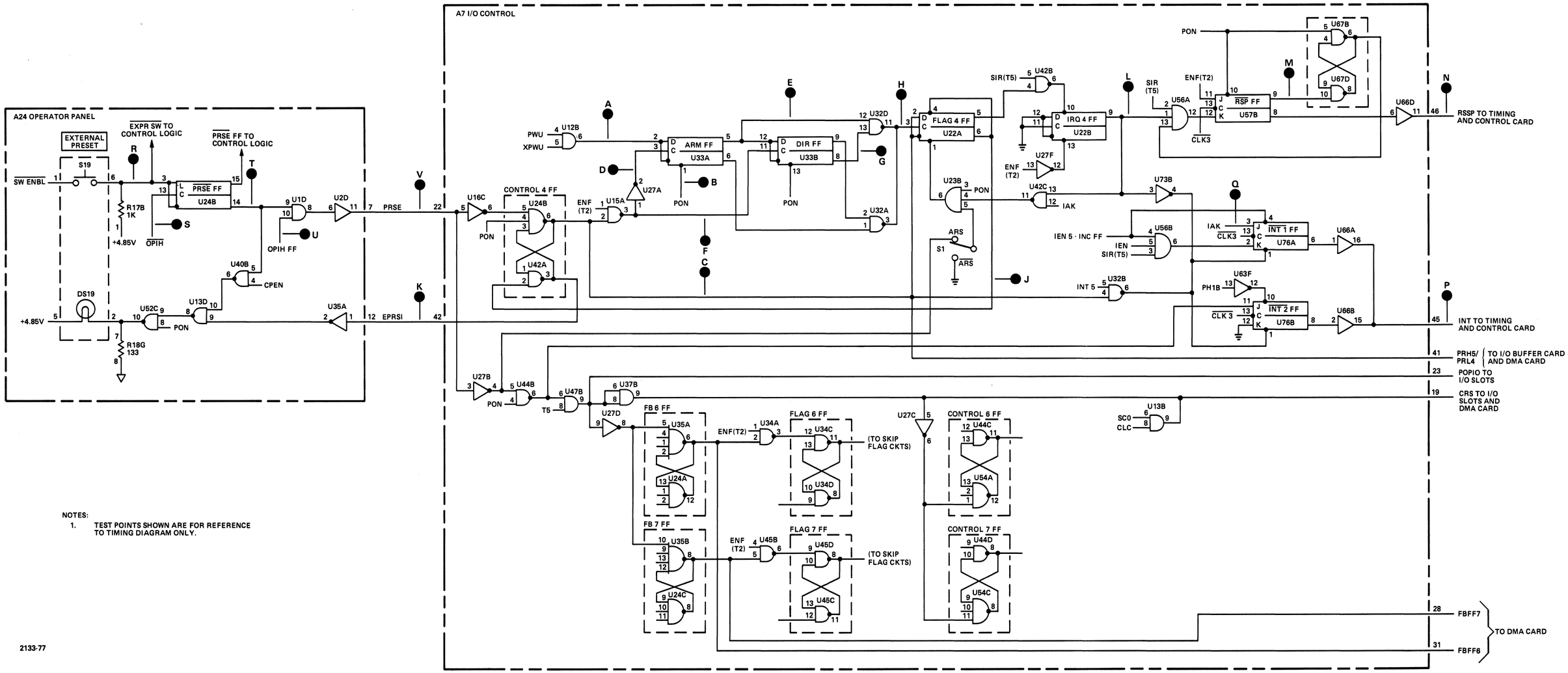
Figure 4-91. Internal Preset Switch Servicing Diagram (Sheet 2 of 2)



NOTES:

1. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTERS "I" AND "O" NOT USED).

Figure 4-92. External Preset Switch Timing Diagram

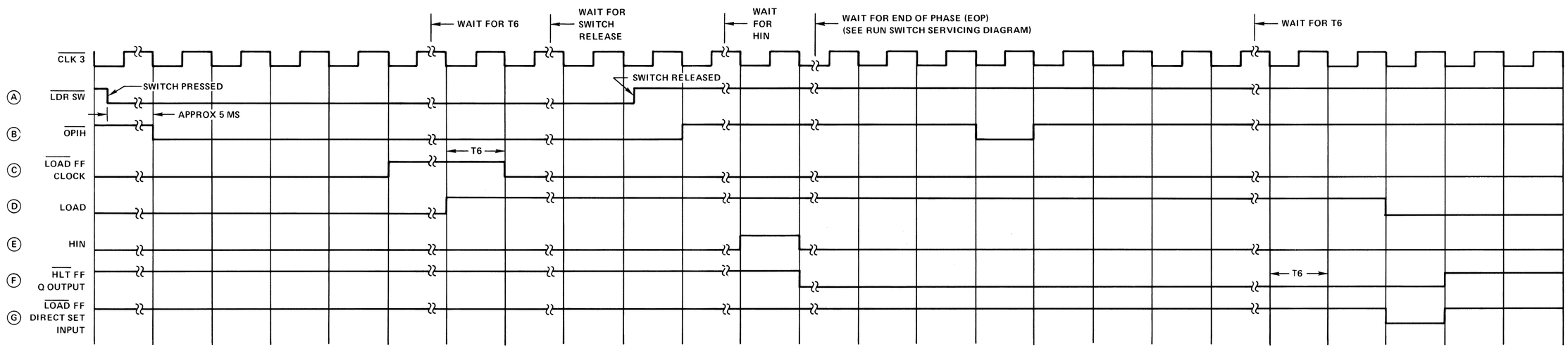


NOTES:

1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

2133-77

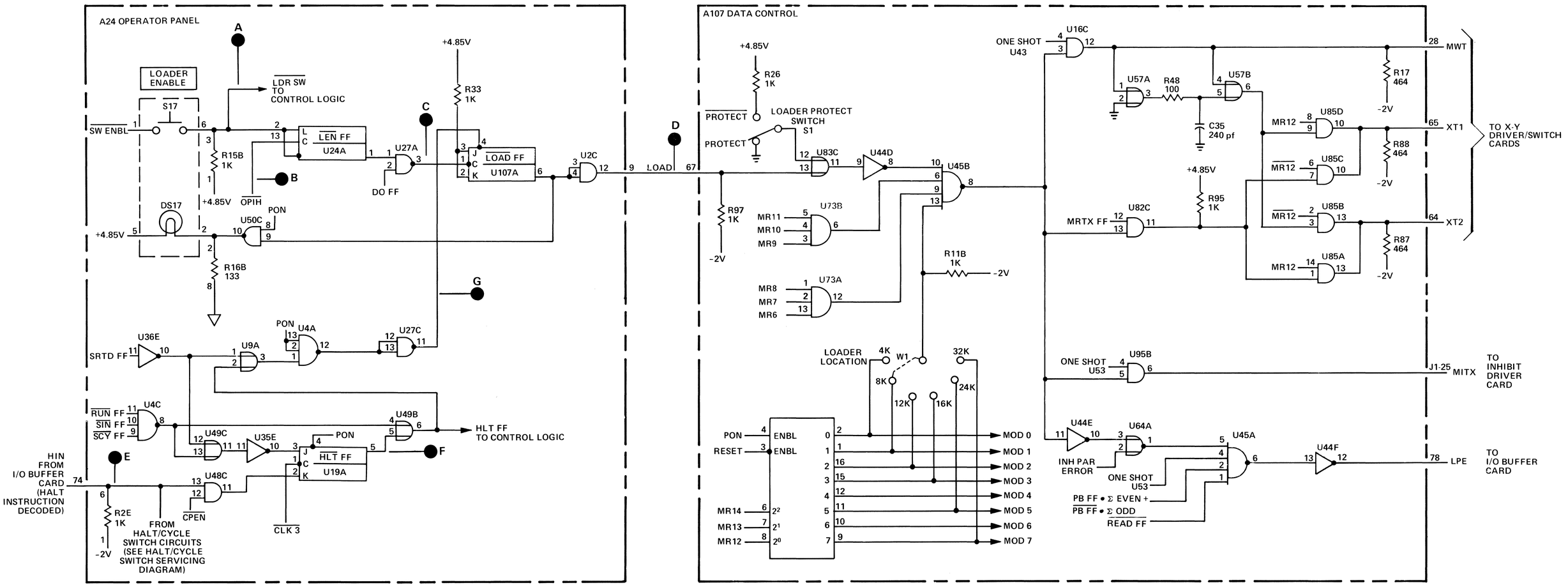
Figure 4-93. External Preset Switch Servicing Diagram



NOTES: 1. REFER TO RUN SWITCH TIMING DIAGRAM FOR ADDITIONAL INFORMATION.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGAGRM.

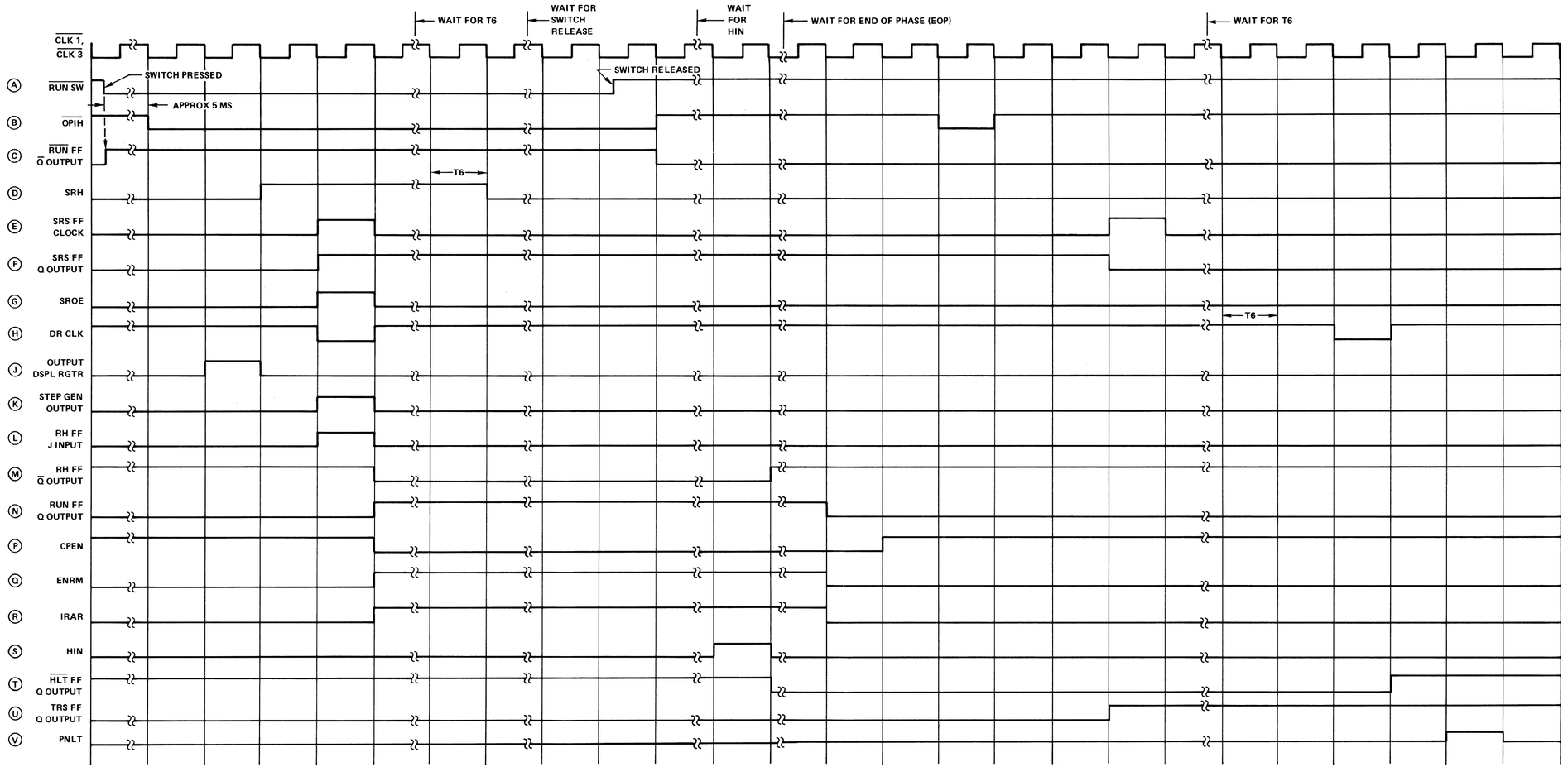
2133-78

Figure 4-94. Loader Enable Switch Timing Diagram



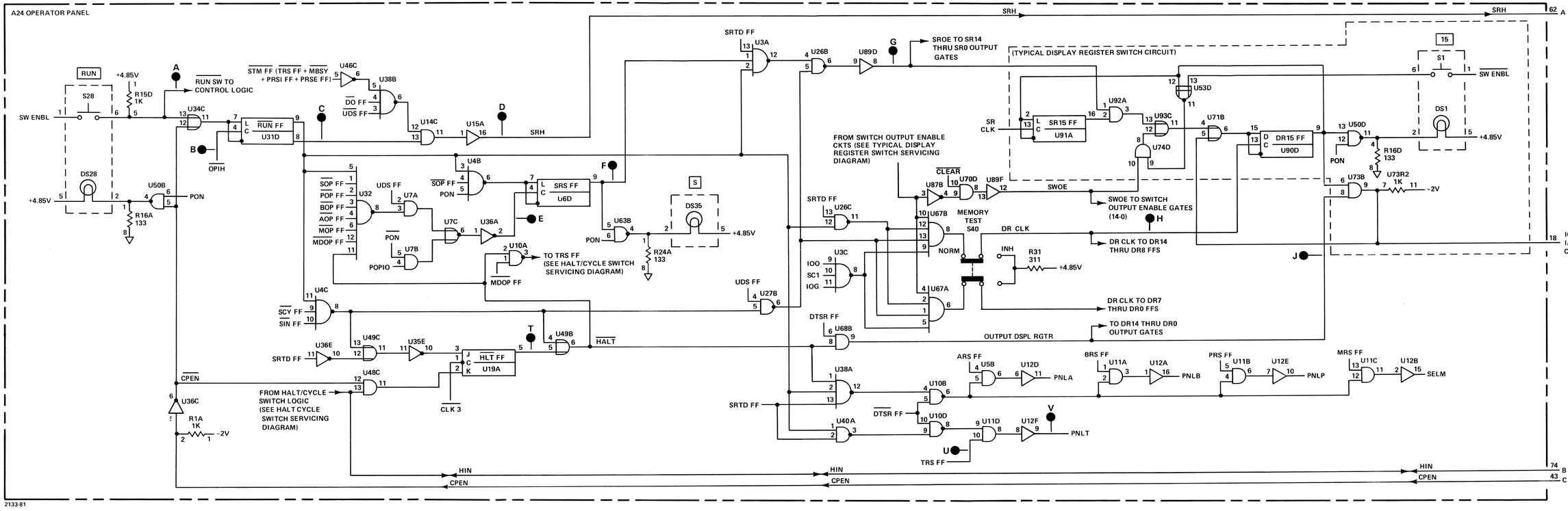
NOTES: 1. TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

Figure 4-95. Loader Enable Switch Servicing Diagram



NOTES: 1. FOR ADDITIONAL SIGNAL TIMING OF MEMORY DATA, REFER TO MEMORY DATA SWITCH SERVICING DIAGRAM WAVEFORMS.
2. CIRCLED LETTERS ADJACENT TO SIGNAL NAMES CORRESPOND TO TEST POINT DESIGNATIONS SHOWN ON SERVICING DIAGRAM (LETTERS "I" AND "O" ARE NOT USED).

Figure 4-96. Run Switch Timing Diagram



NOTES:
TEST POINTS SHOWN ARE FOR REFERENCE TO TIMING DIAGRAM ONLY.

Figure 4-97. Run Switch Servicing Diagram (Sheet 1 of 2)

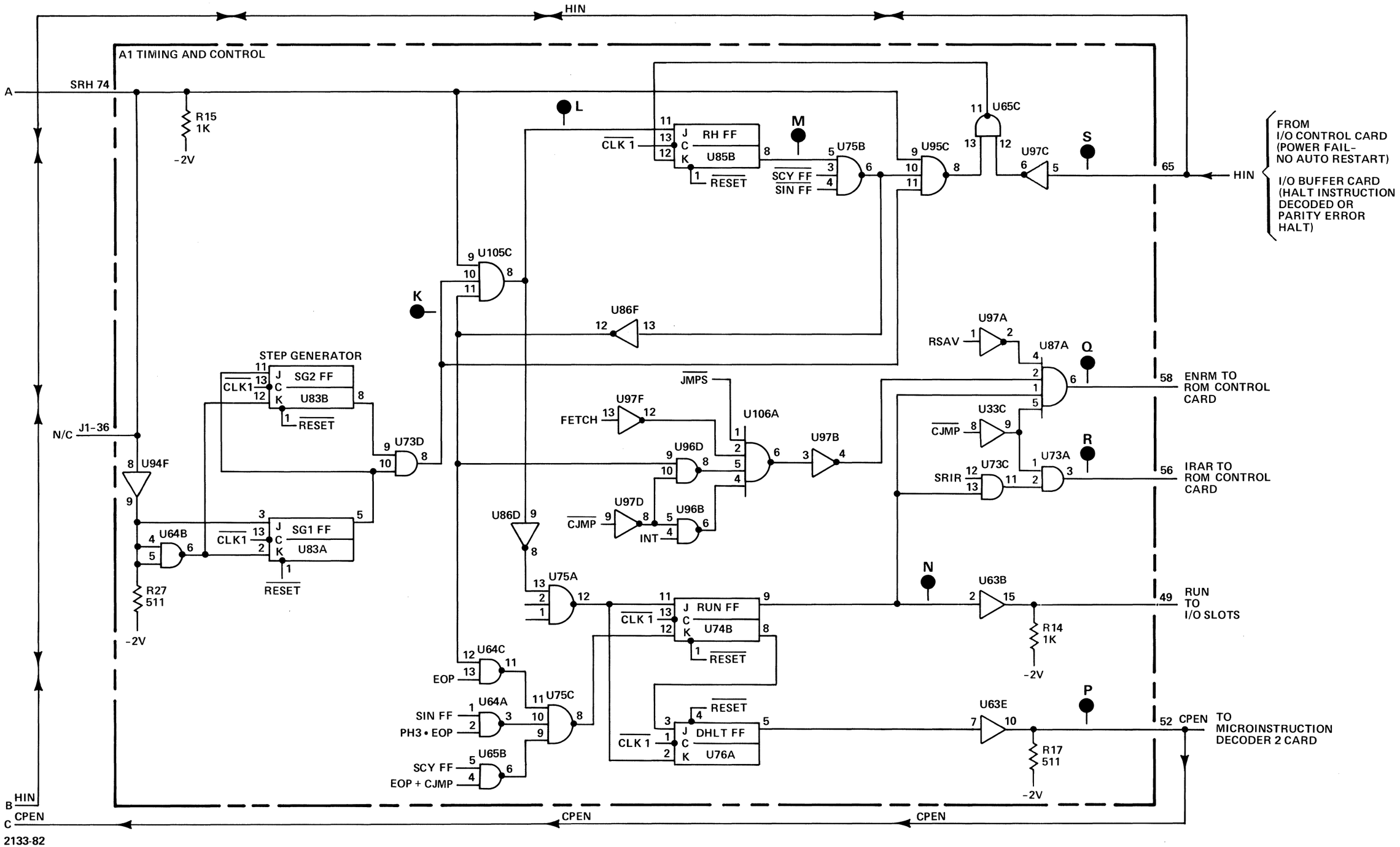


Figure 4-97. Run Switch Servicing Diagram (Sheet 2 of 2)

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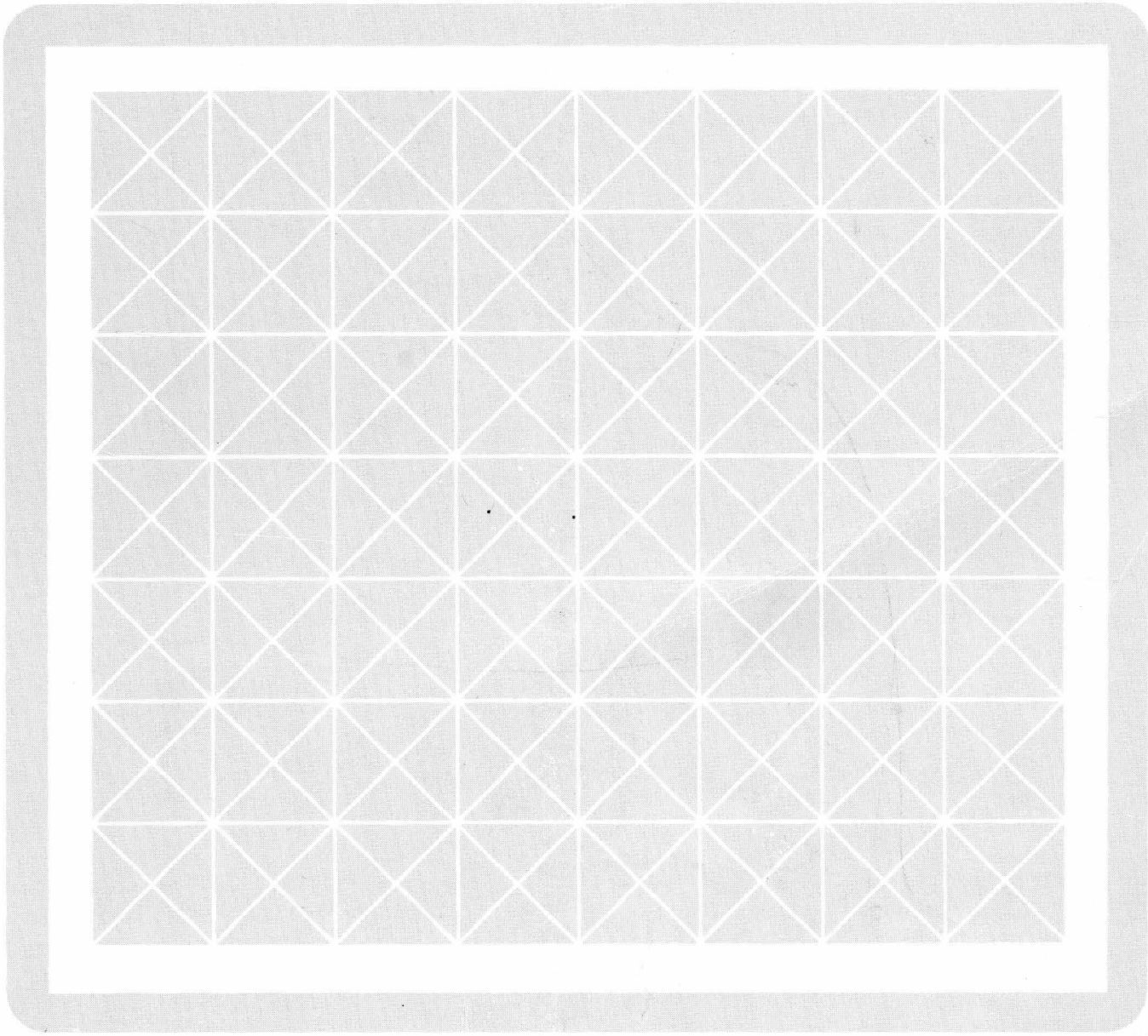

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