

CONTROL DATA
CORPORATION

Customer Engineering Diagrams

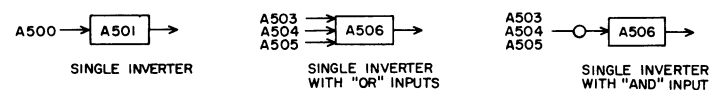
CONTROL DATA
160 COMPUTER

CONTENTS

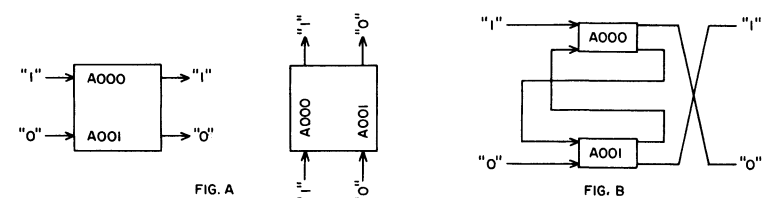
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SYMBOLS

SINGLE INVERTER - A single inverter inverts input signals so that a "1" input results in a "0" output and a "0" input results in a "1" output. Inputs to symbols are identified by arrowheads.

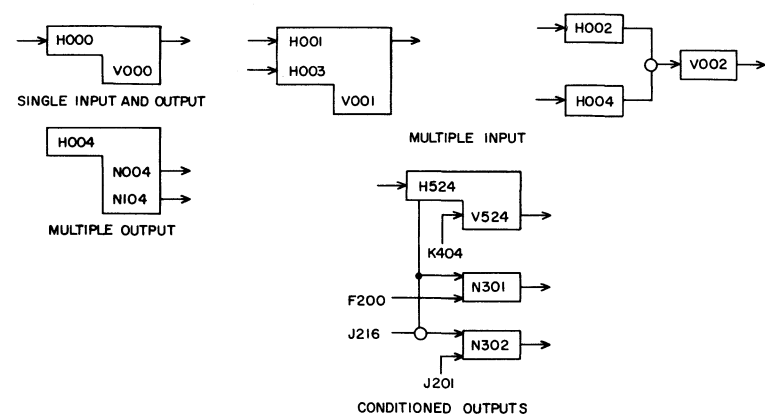


FLIP-FLOP (FF) - The flip-flop is a storage device with two stable states, designated "1" (or Set) and "0" (or Clear), and is composed of two inverters. The logical symbol (Fig. A) is a square that is formed by the combination of two single inverter symbols. By convention, "1" (or Set) inputs and outputs are shown with the upper or left half of the symbol and "0" (or Clear) inputs and outputs are shown with the lower or right half of the symbol. This diagrammatic convention simplifies the actual interconnection of the two inverters as shown in Fig. B.

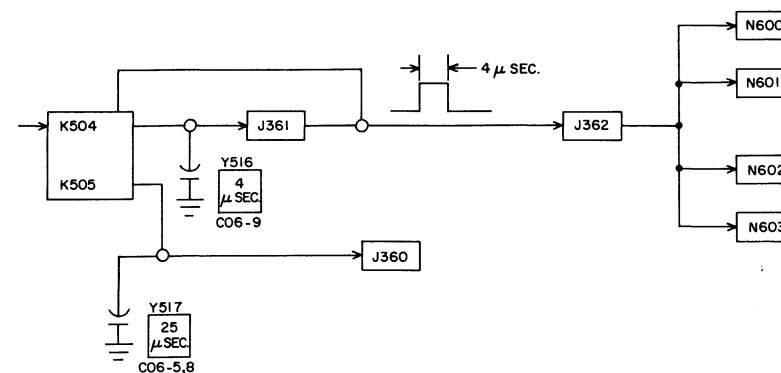


CONTROL DELAY - A control delay consists of an H--- part, which receives the input, and a V--- or N--- part, which provides the output. The output is a clocked pulse which is delayed with respect to the input pulse by one phase time of the clock (0.2 microseconds). Conventions which apply to control delays are:

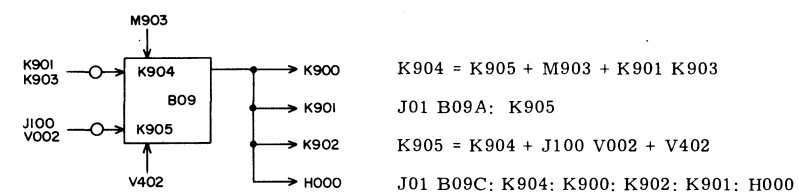
1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.
2. The logical number designation indicates the clock phase of the output signal. An odd number indicates an odd clock phase, and an even number indicates an even clock phase.
3. The time scales shown on all sequence diagrams are in 0.2 microsecond (1 clock phase time) intervals.



CAPACITIVE DELAY - A capacitive delay is used in an AND configuration to delay the "1" input to a logic element. The capacitor is shown with the curved (negative) plate adjoining the AND symbol. A small box shows the equation file symbol assigned to that delay, the duration of the delay, and the coordinate jack and pin number where physical connection to the capacitor(s) is made. The output waveform may be omitted.



SYMBOL REPRESENTATION OF TYPICAL EQUATIONS

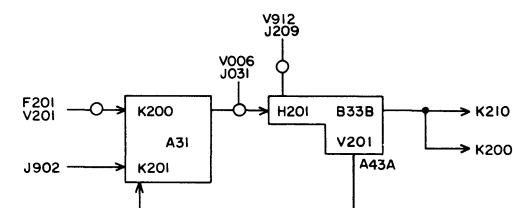


$$K904 = K905 + M903 + K901 \quad K903$$

$$J01 \text{ B09A: } K905$$

$$K905 = K904 + J100 \quad V002 + V402$$

$$J01 \text{ B09C: } K904; K900; K902; K901; H000$$



$$K200 = K201 + F201 \quad V201 + K201$$

$$J01 \text{ A31 A: } K201; J246$$

$$K201 = K200 + V201 + J902$$

$$J01 \text{ A31C: } K200; H201; F229; K200$$

$$H201 = C004 + K201 \quad J031 \quad V006 + J209 \quad V912$$

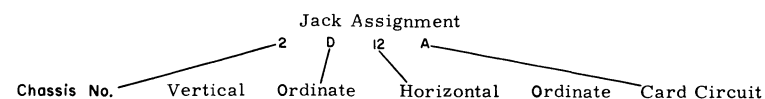
$$J01 \text{ B33B: } V201$$

$$V201 = H201 + C013$$

$$J01 \text{ A43A: } K201; K210$$

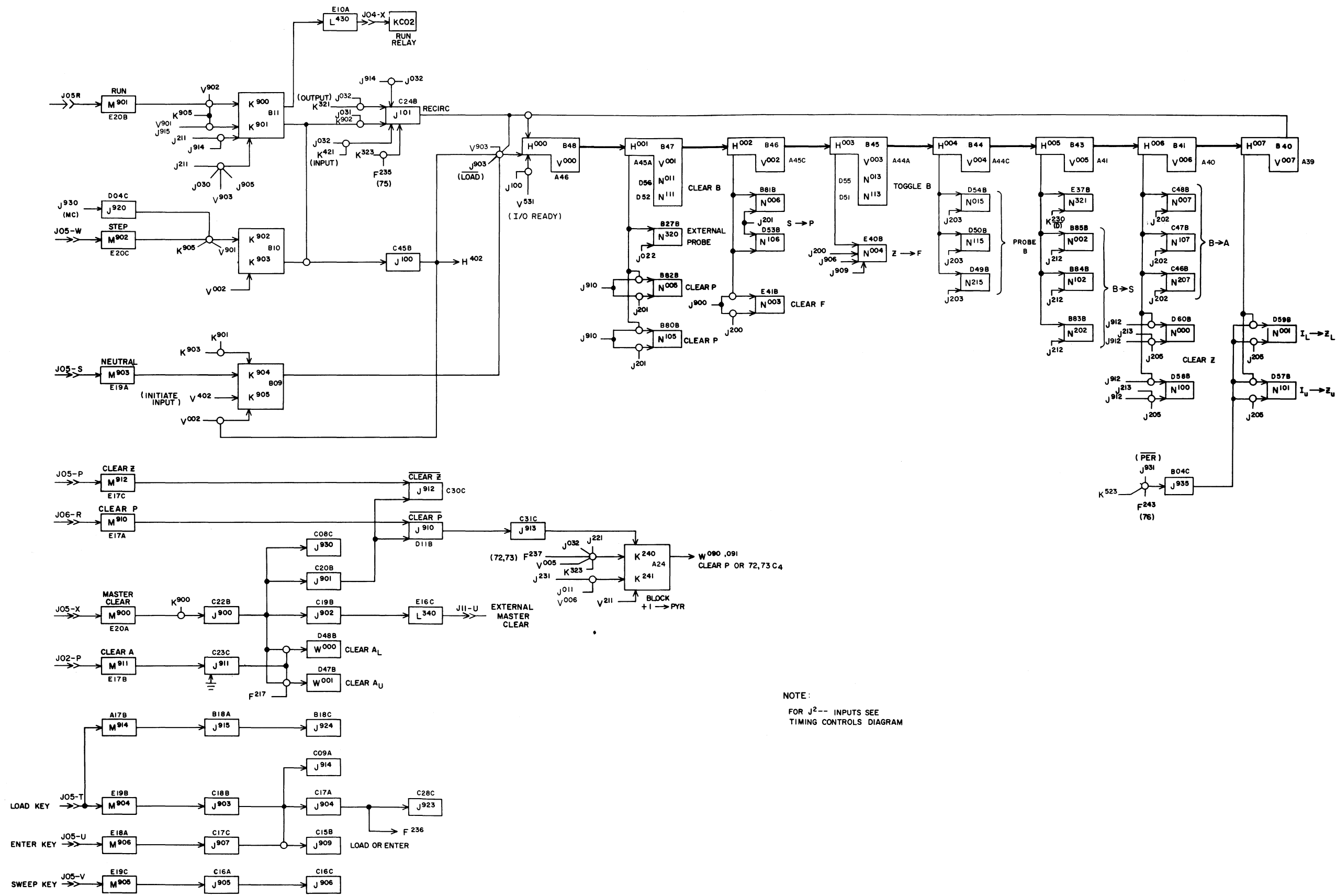
JACK ASSIGNMENTS

The jack assignments of the printed circuit cards associated with each logic symbol appear near the logical designation on the diagram. Jack assignments indicate the physical location of a printed circuit card.



- Conventions which apply to jack assignments shown on the diagrams:
1. When most of the jack assignments on a diagram are on a common chassis, the chassis number is omitted from the jack assignments for this chassis and specified in a note on the diagram.
 2. The omission of the card circuit letter from a jack assignment indicates card circuit B. (For flip-flops which indicate one jack assignment for both inverters, the omission of the card circuit letter indicates card circuit A for the even-numbered inverter and card circuit C for the odd-numbered inverter.)

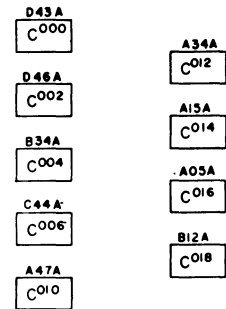
KEY TO SYMBOLS USED ON LOGIC DIAGRAMS



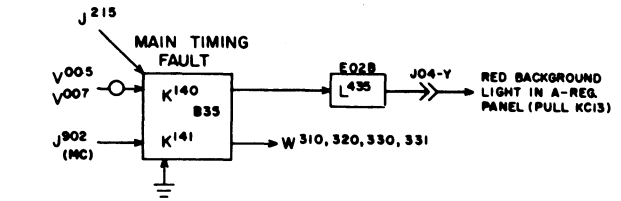
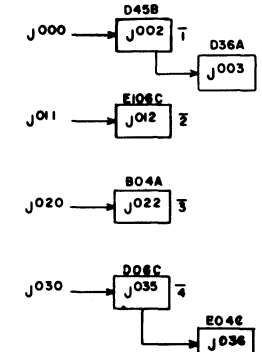
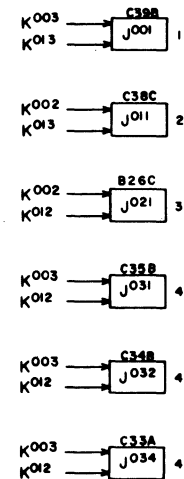
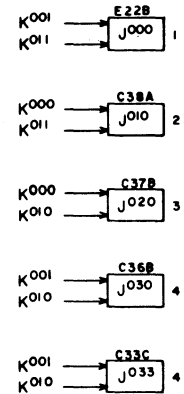
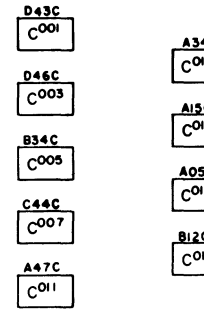
NOTE:
FOR J²-- INPUTS SEE
TIMING CONTROLS DIAGRAM

CLOCK

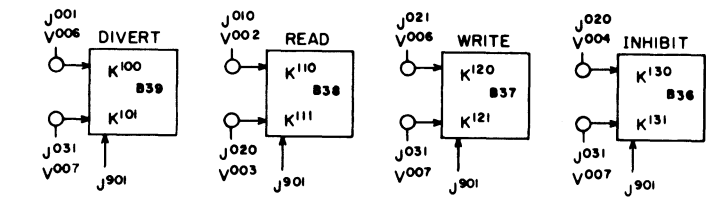
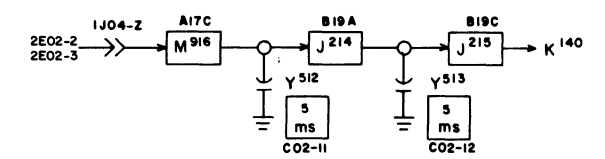
EVEN PHASE



ODD PHASE



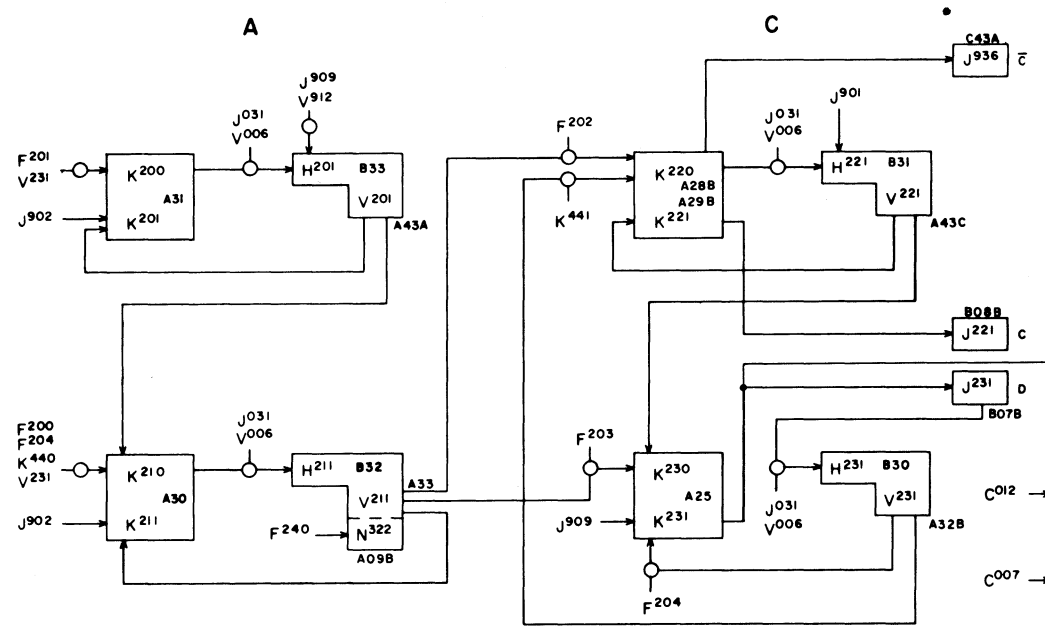
NON-VOLATILE STORAGE CONTROL



STORAGE REFERENCE CONTROL (SRC)

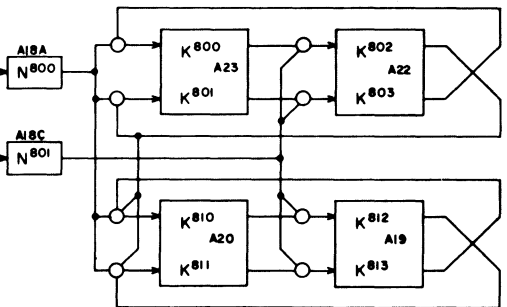
F TRANSLATORS

SYMBOL	FUNCTION
F200	\bar{I}
F201	i
F202	B → C
F203	B → D
F204	$\bar{D} \rightarrow \bar{D}$
F240	75

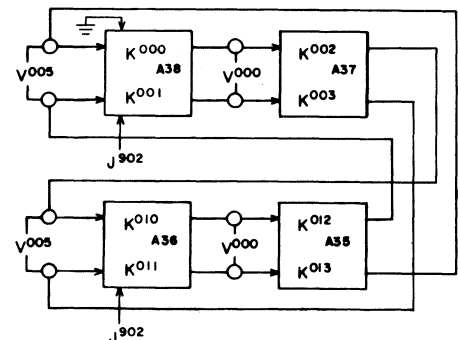


PRIMARY TIMING CONTROL

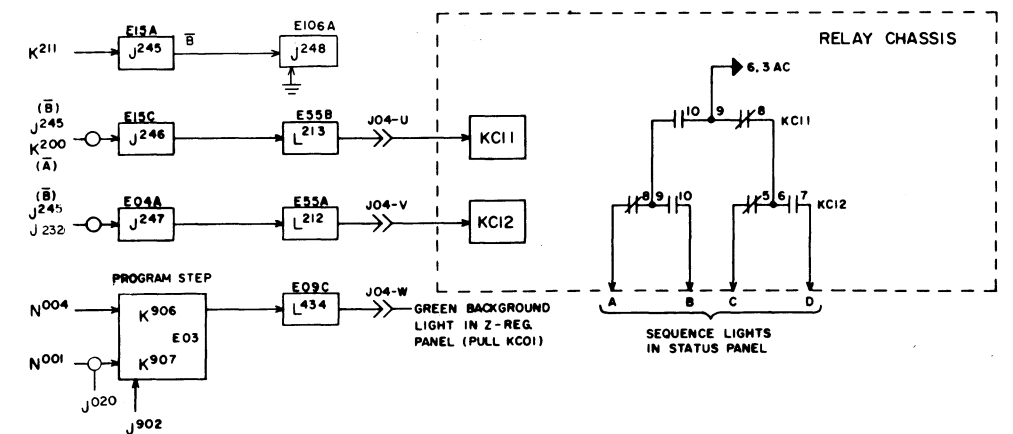
RESYNC COUNTER



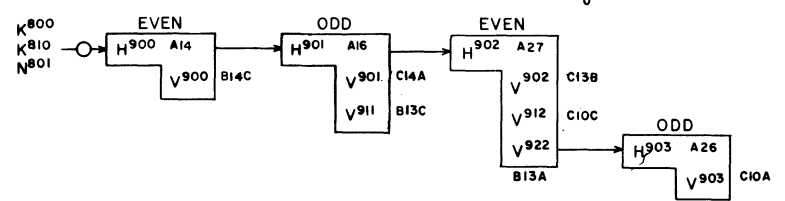
TIMING CHAIN EXCURSIONS COUNTER (EK)



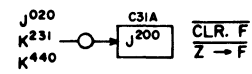
STORAGE SEQUENCE CONTROL (SSC)



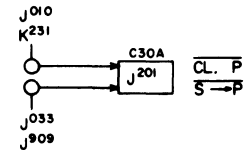
RESYNC TIMING



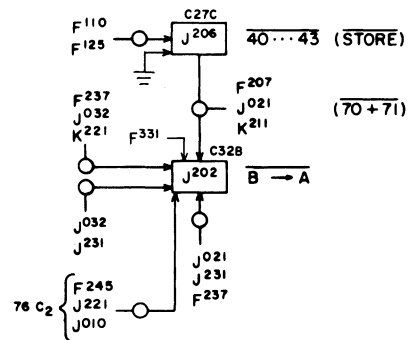
CONTROL DATA CORPORATION 3049 119809 F SMALL MEMORY STACK 2	REFERENCE NUMBERS COMPONENTS REVISIONS TITLE MAIN CONTROL	CONTROL DATA CORPORATION 3049 119809 F SMALL MEMORY STACK 2
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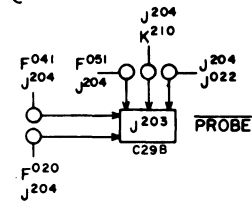
DOWN FOR
EARLY 3rd
D-CYCLE
FIRST TRANSFER ON I/O SEQUENCE



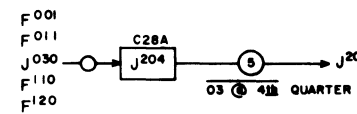
DOWN FOR
EARLY D₂
EARLY 4 ON LD OR ENTER



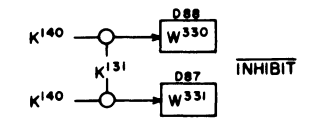
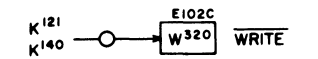
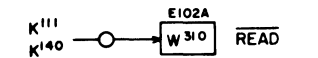
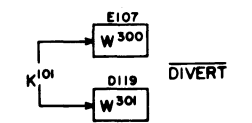
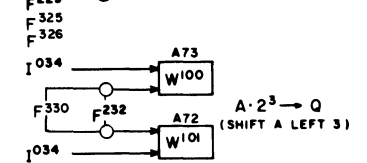
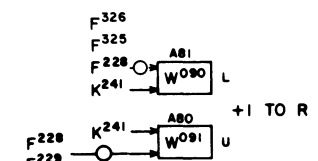
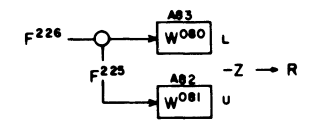
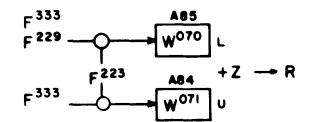
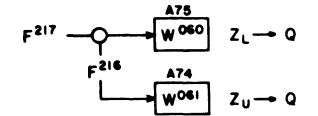
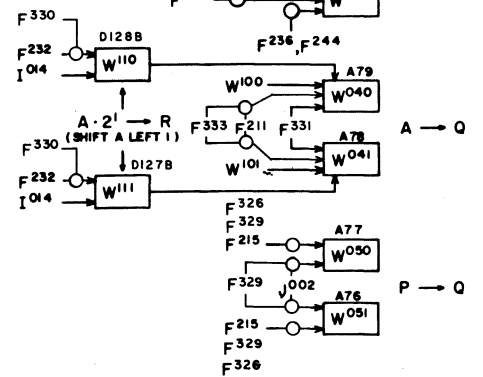
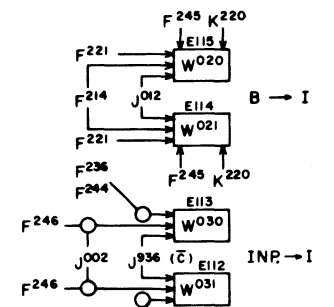
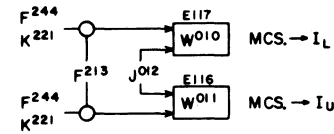
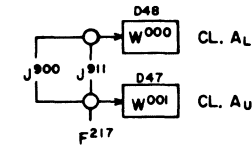
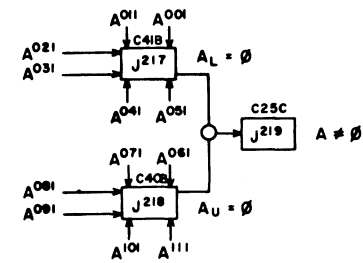
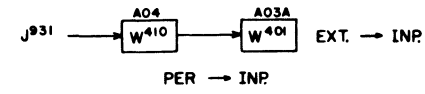
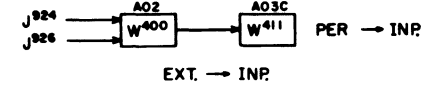
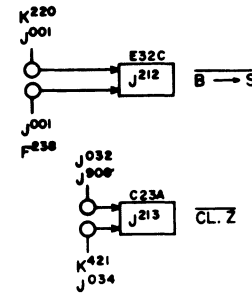
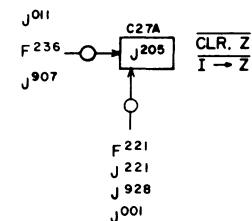
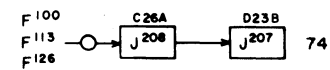
J202 IS DOWN FOR
40...43, 70, 71, 72, 73, D₃
72, 73, C₄
D₄
76 C₂ (EARLY)



J203 IS UP FOR LOGICAL SUM
INSTRUCTIONS ONLY.



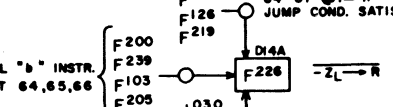
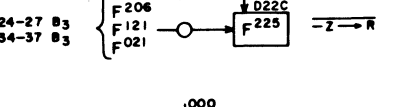
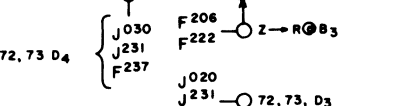
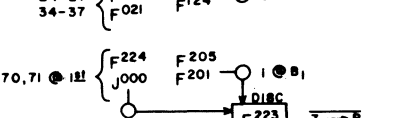
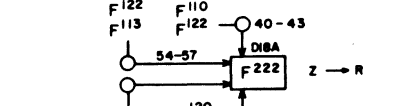
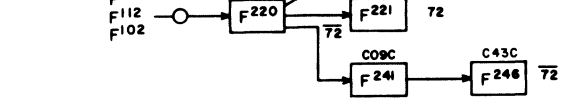
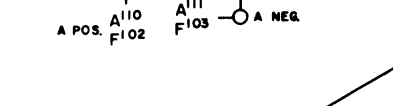
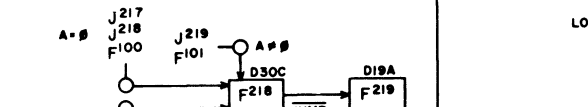
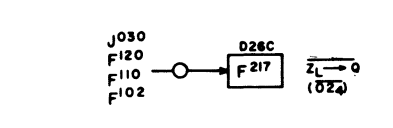
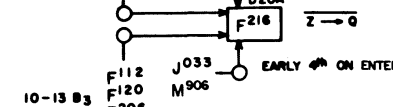
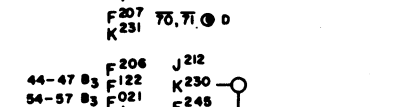
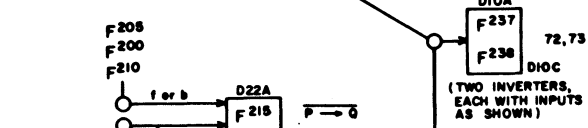
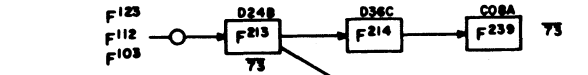
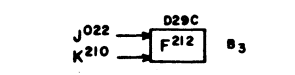
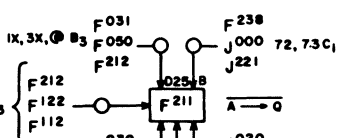
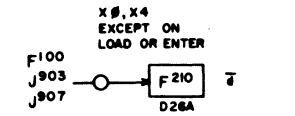
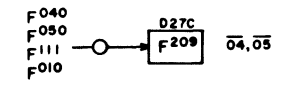
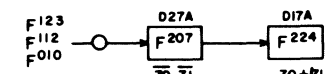
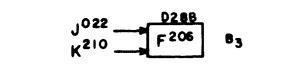
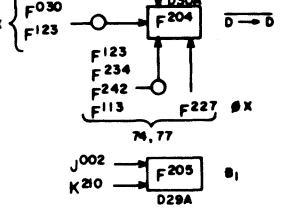
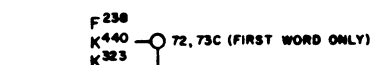
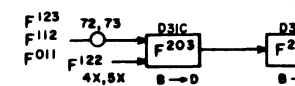
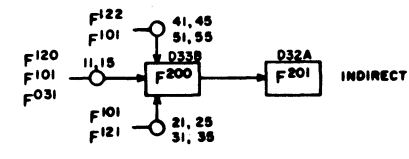
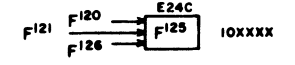
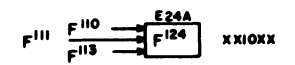
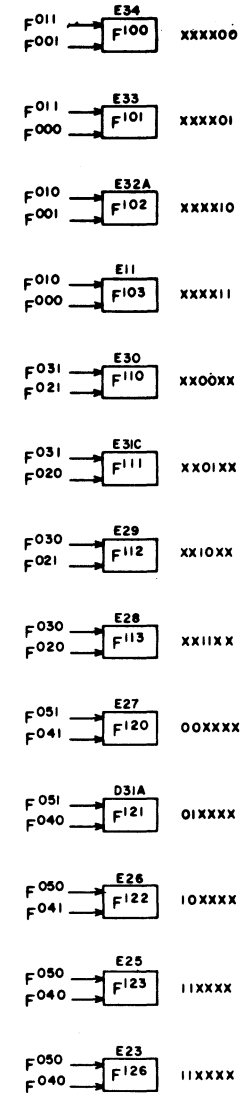
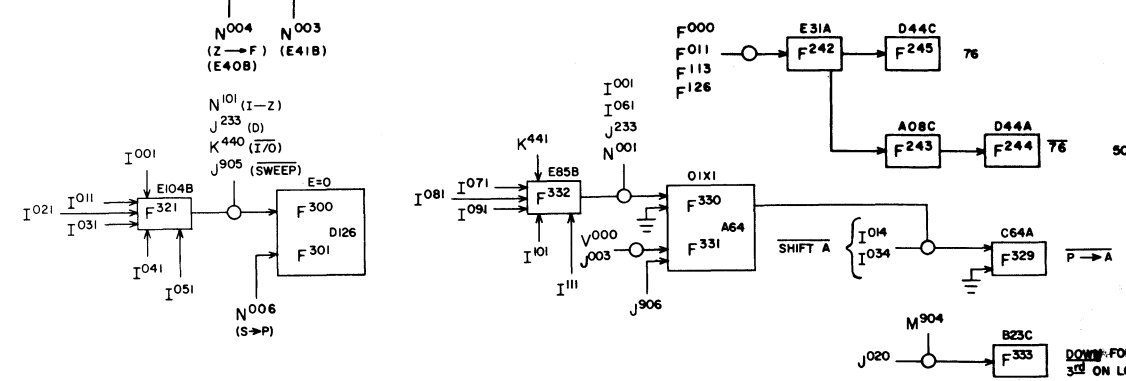
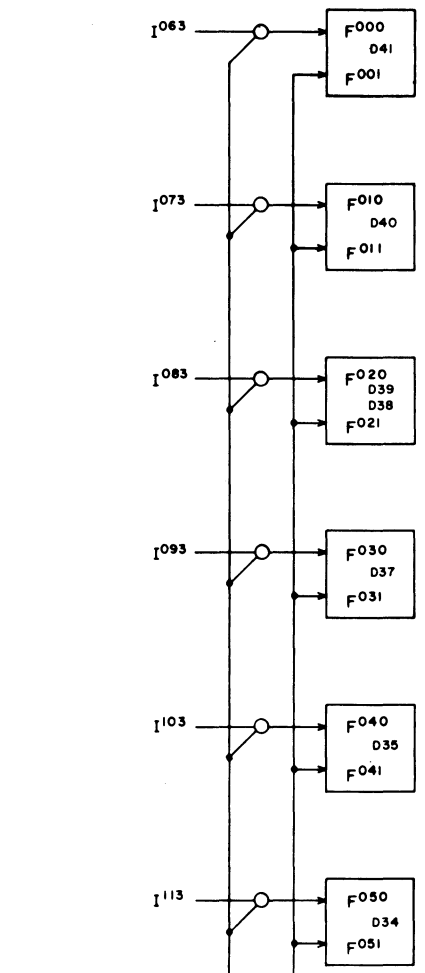
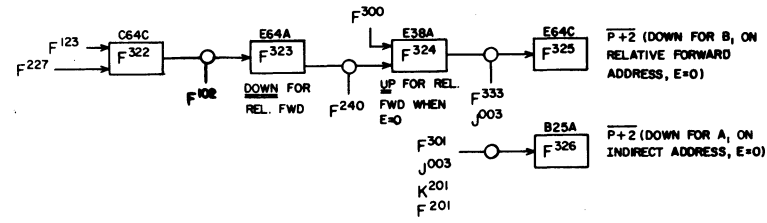
J204 IS DOWN FOR
LOGICAL SUM.



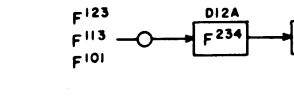
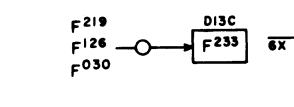
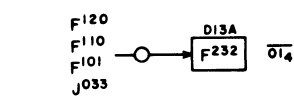
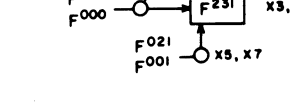
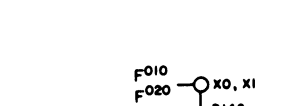
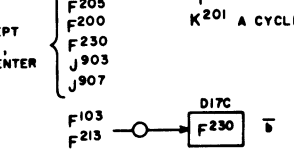
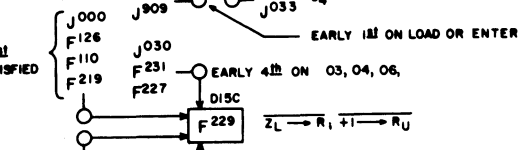
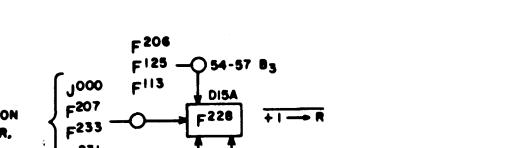
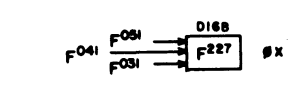
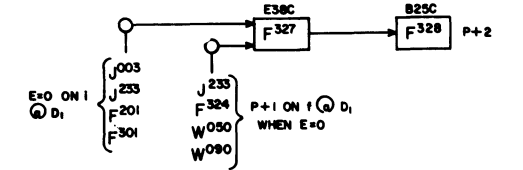
F TRANSLATORS

SYMBOL	FUNCTION
F211	A → 0
F213	73
F214	73
F215	F → 0
F216	Z → 0
F217	Z → 0
F221	72
F223	Z → R
F226	-Z → R
F228	+I → R
F229	Z → R
F232	A SHIFT
F236	72 C ON LOAD MODE
F237	72, 73
F238	72, 73
F244	76
F245	76
F246	72
F325	P+2 FOR REL. ADD.
F326	P+2 FOR IND. ADD.
F329	P → A
F330	OIXT
F331	OIXI

REFERENCE NUMBER				CONTROL DATA CORPORATION
3049				
DESIGNER'S NAME				119810 F
ECO 24				
TITLE				3
LOGIC DIAGRAM TIMING CONTROLS				

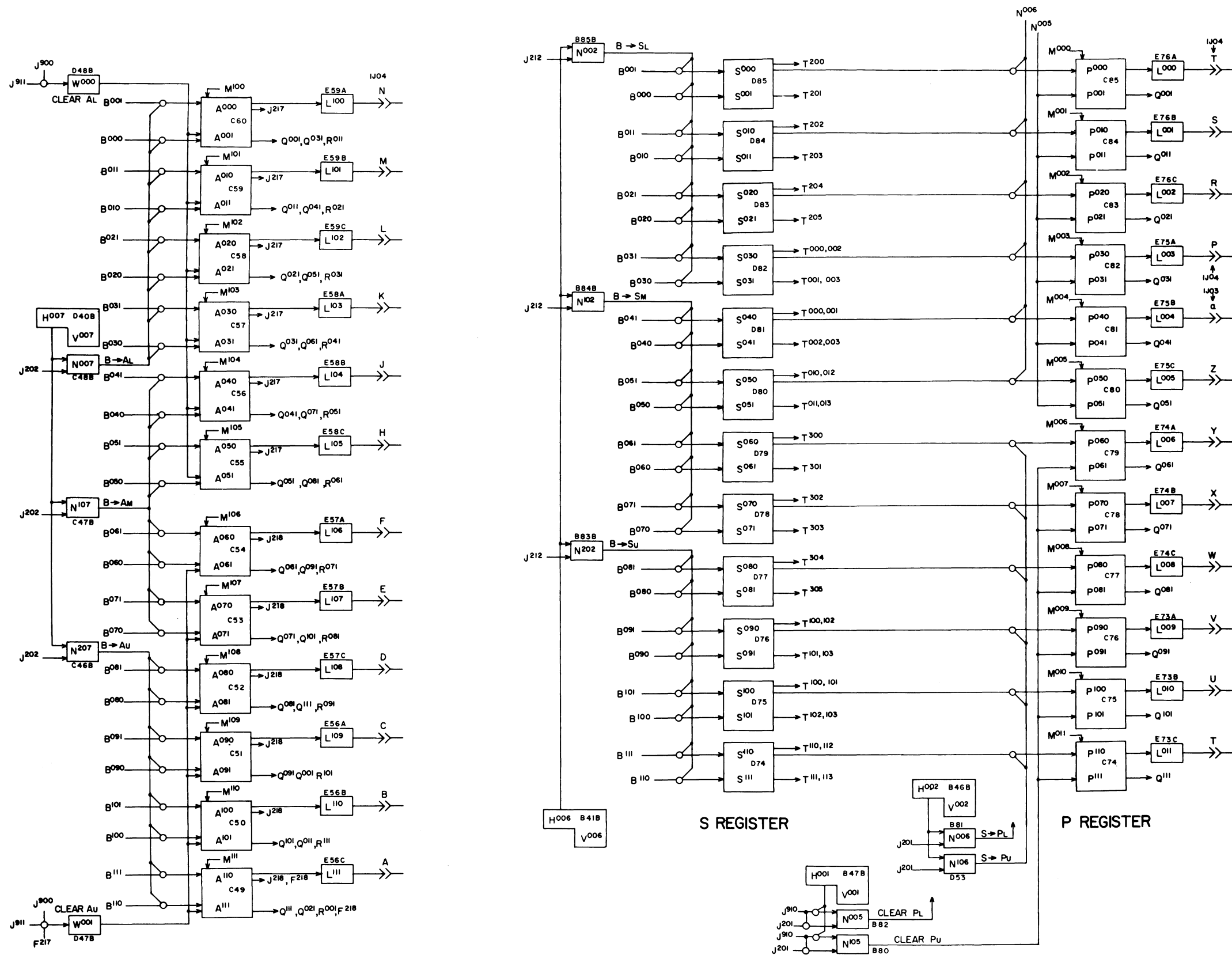


ALL "b" INSTR. EXCEPT 64, 65, 66



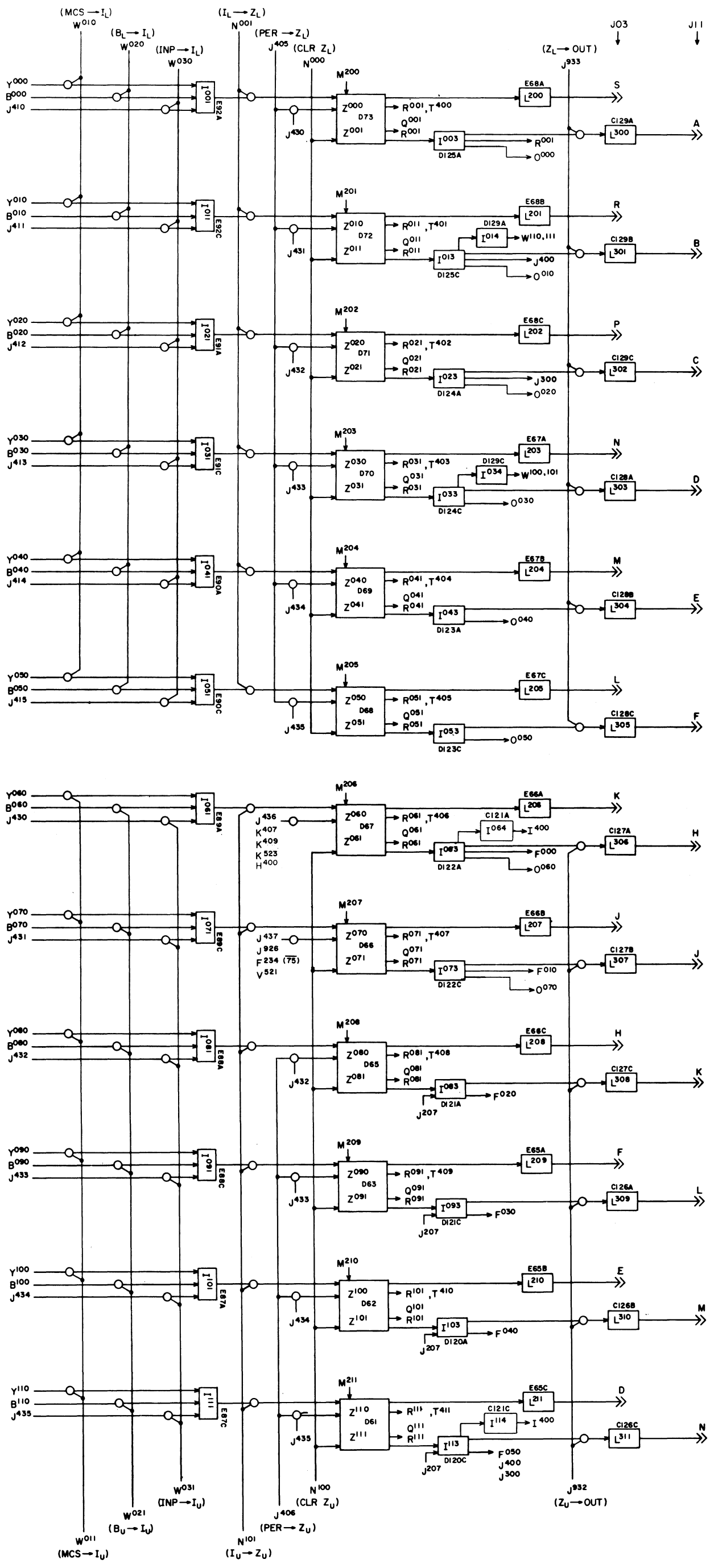
REVISIONS			
NO.	DATE	BY	REASON

CONTROL DATA CORPORATION	
3049	
119811-A	F
LOGIC DIAGRAM FUNCTION REGISTER	
4	



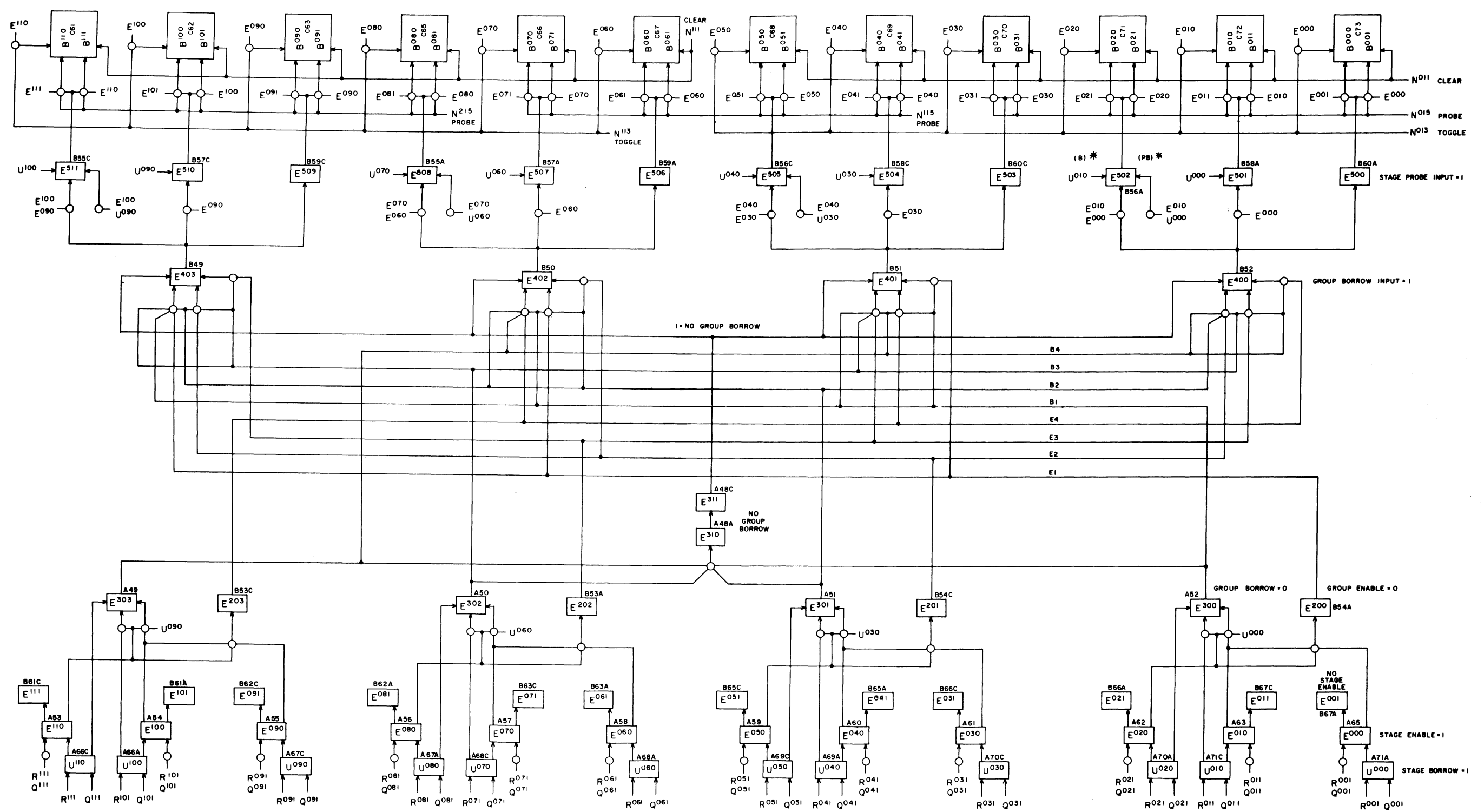
NOTE
 JACK CONNECTIONS SHOWN GO TO
 DIGITAL DISPLAY UNITS IN CONSOLE.

LOGIC DIAGRAM
 REGISTERS A, S, AND P



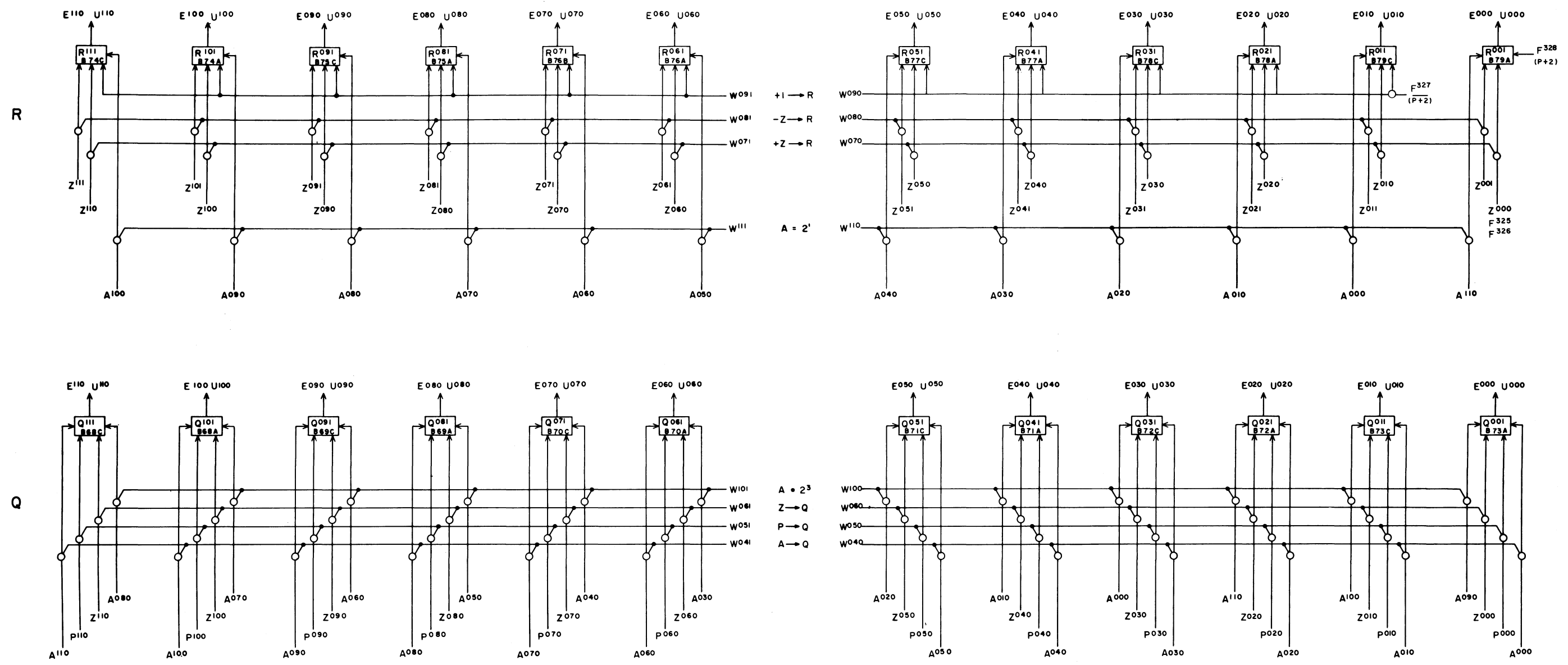
NOTES:
 L200...L211 OUTPUTS GO TO
 DIGITAL DISPLAY UNIT IN
 CONTROL CONSOLE.
 L300...L311 FEED THE OUTPUT
 CABLE

Z REGISTER	
3049	CONTROL DATA COMPARISON
119813-A	F
6	

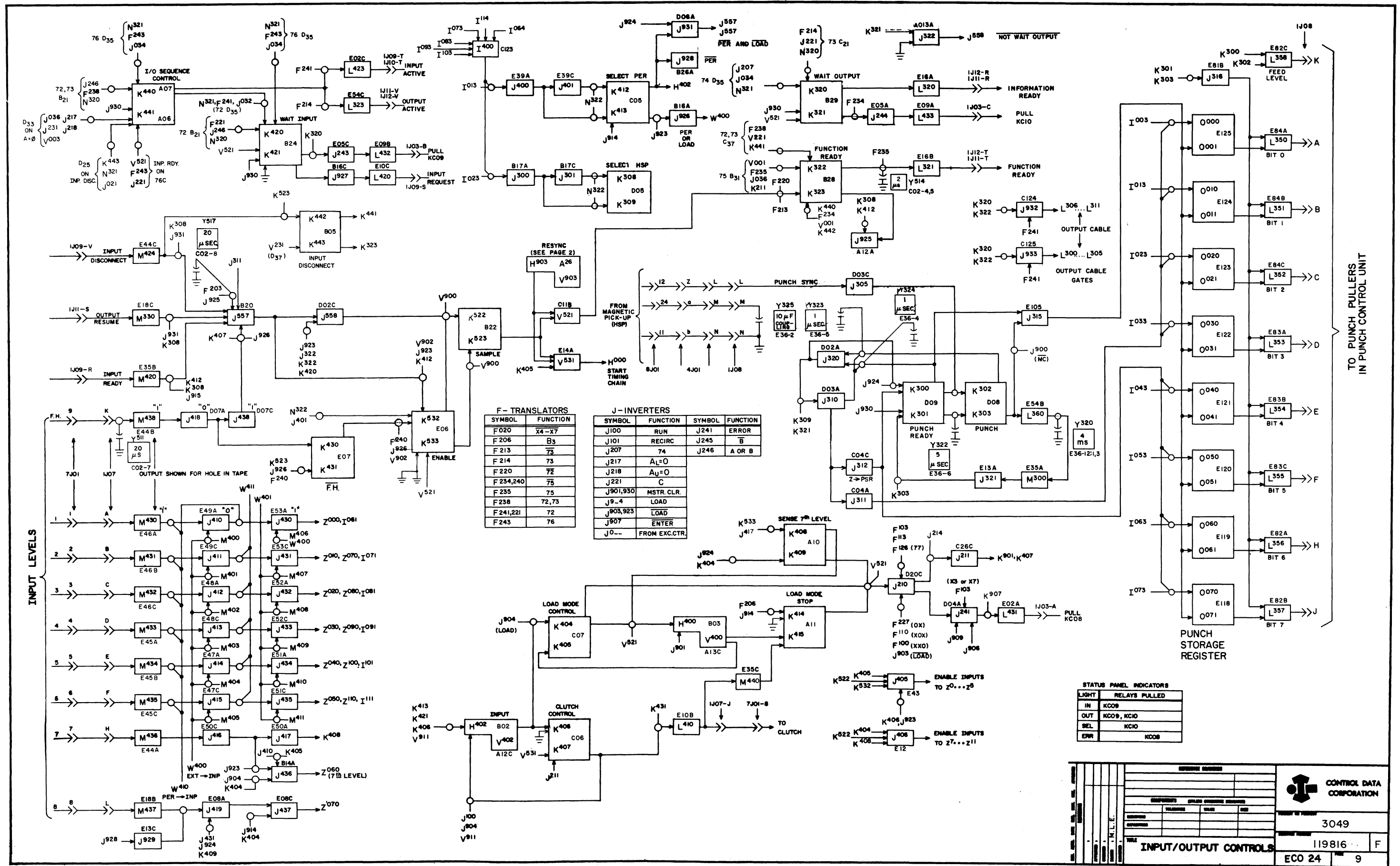


PYRAMD INPUTS
 +Z } R
 -Z }
 +1 }
 A-2 }
 P } Q
 A }
 A-2 }
 +Z }

* SEE TEXT FOR (B) & (PB) DESIGNATION. THESE TERMS APPLY TO THE CORRESPONDING INPUTS IN EACH OF THE OCTAL GROUPS.



LOGIC DIAGRAM
R & Q INVERTERS



F - TRANSLATORS

SYMBOL	FUNCTION
F020	X4-X7
F206	B3
F213	73
F214	73
F220	72
F234,240	75
F235	75
F238	72,73
F241,221	72
F243	76

J - INVERTERS

SYMBOL	FUNCTION	SYMBOL	FUNCTION
J100	RUN	J241	ERROR
J101	RECIRC	J245	B
J207	74	J246	A OR B
J217	73		
J218	A _L =0		
J221	A _U =0		
J901,930	C		
J9-4	LOAD		
J903,923	LOAD		
J907	MSTR. CLR.		
J0--	ENTER		
J0--	FROM EXC.CTR.		

STATUS PANEL INDICATORS

LIGHT	RELAYS PULLED
IN	KC09
OUT	KC09, KC10
SEL	KC10
ERN	KC08

CONTROL DATA CORPORATION

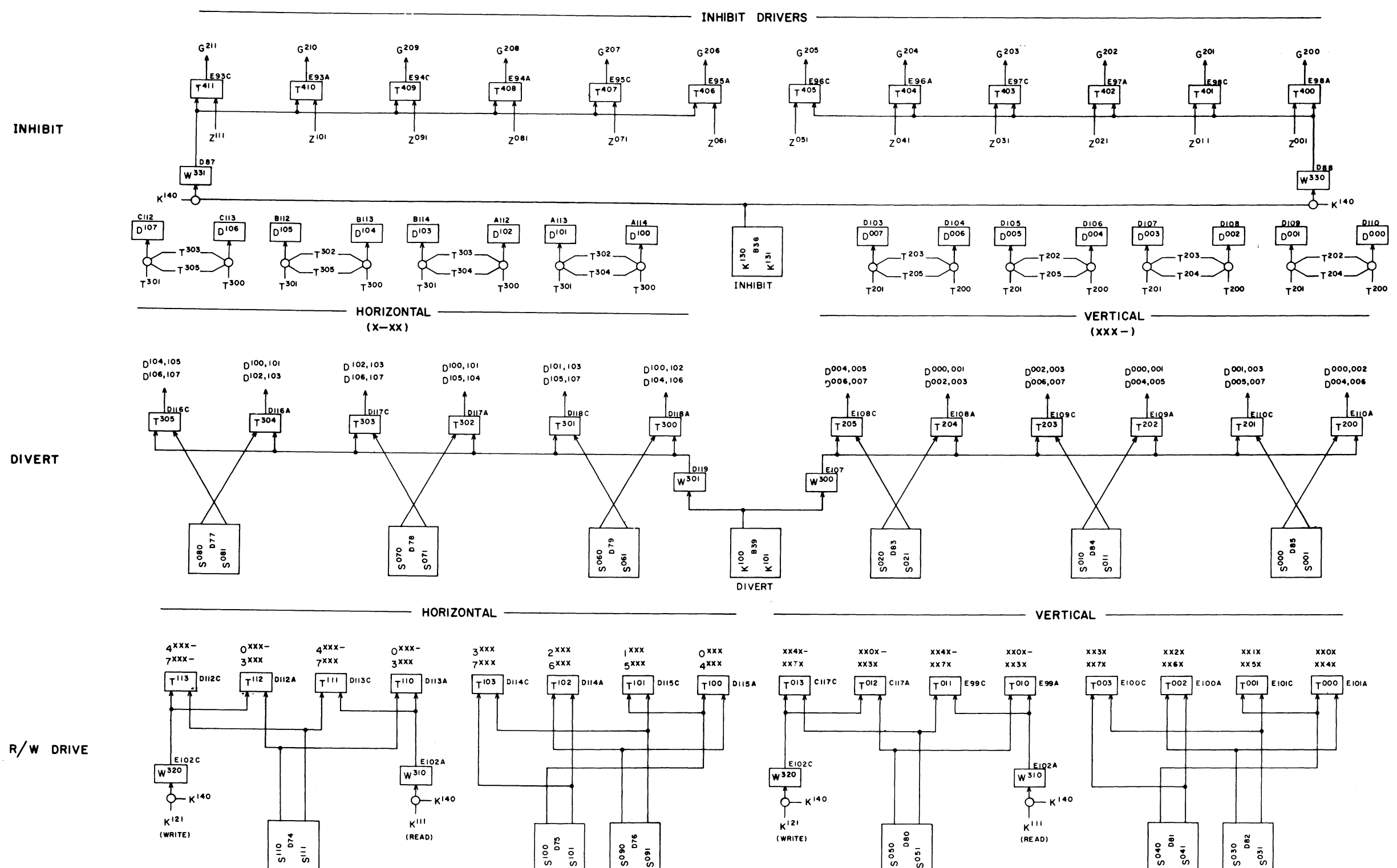
3049

119816 F

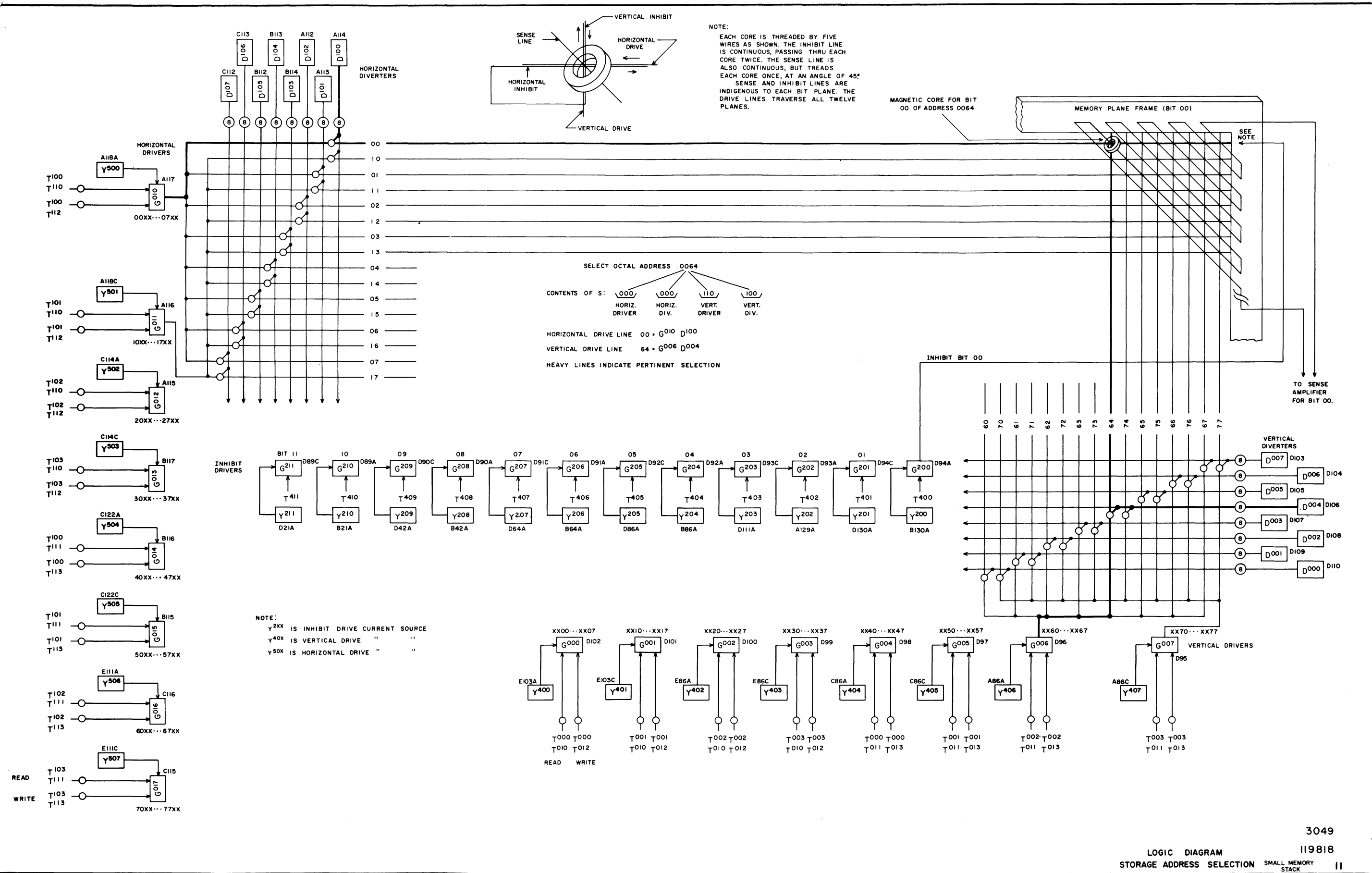
ECO 24 9

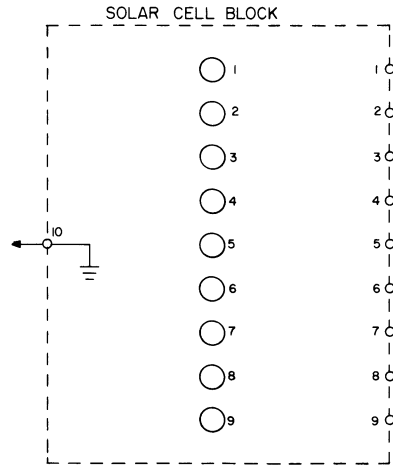
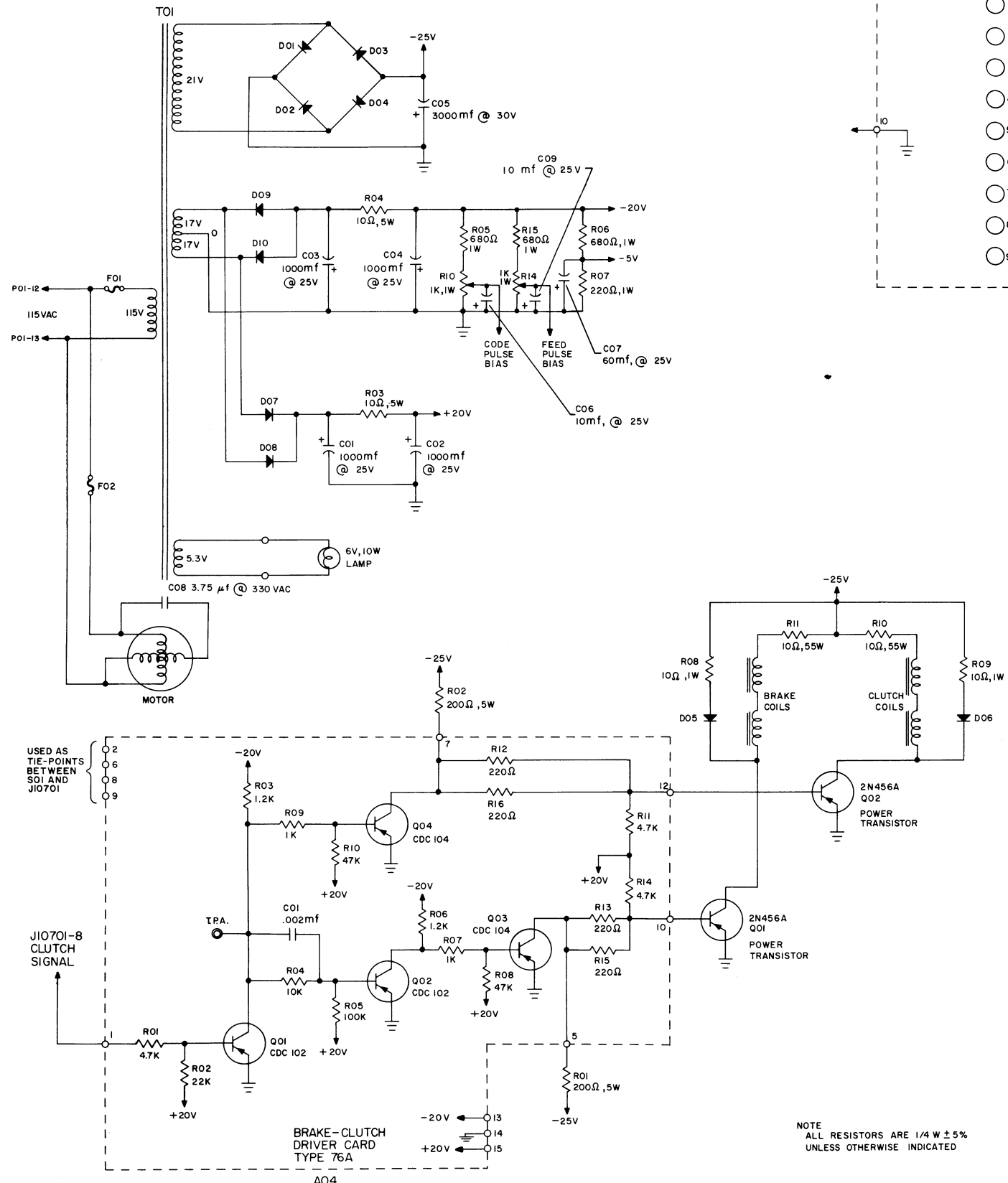
INPUT/OUTPUT CONTROLS

TO PUNCH PULLERS
IN PUNCH CONTROL UNIT

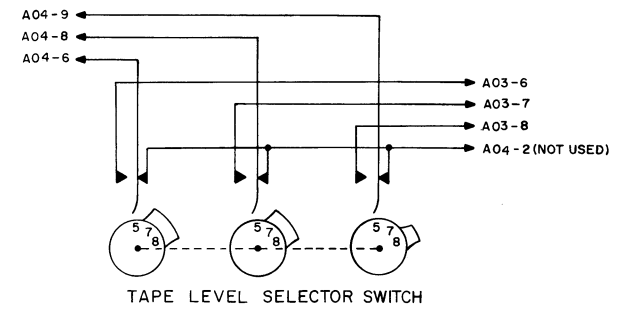
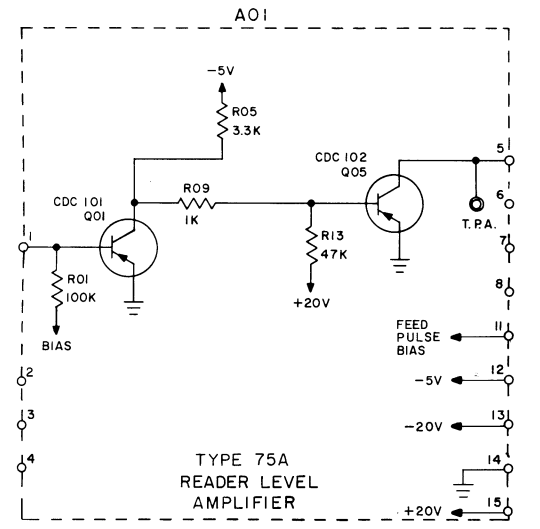
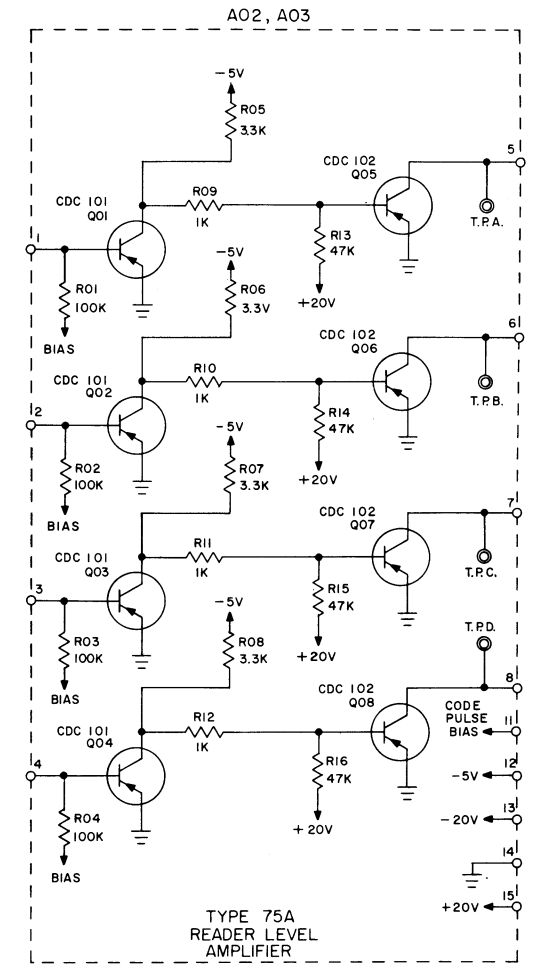
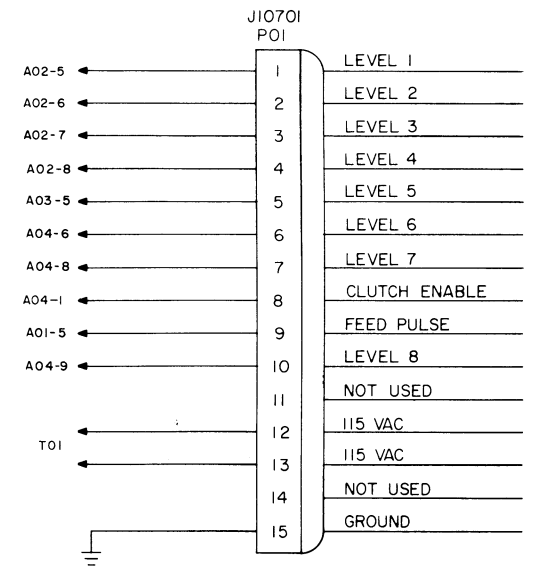


NOTE:
 LOW-ORDER DIGIT IN DESTINATION SYMBOL SIGNIFIES
 MAGNITUDE OF DIVERTER LINE SELECTED. THUS:
 D104,105 = X4XX OR X5XX
 D106,107 = X6XX OR X7XX
 OUTPUT DESIGNATIONS FROM T305, AND T205
 =XXX4,XXX5,XXX6,XXX7

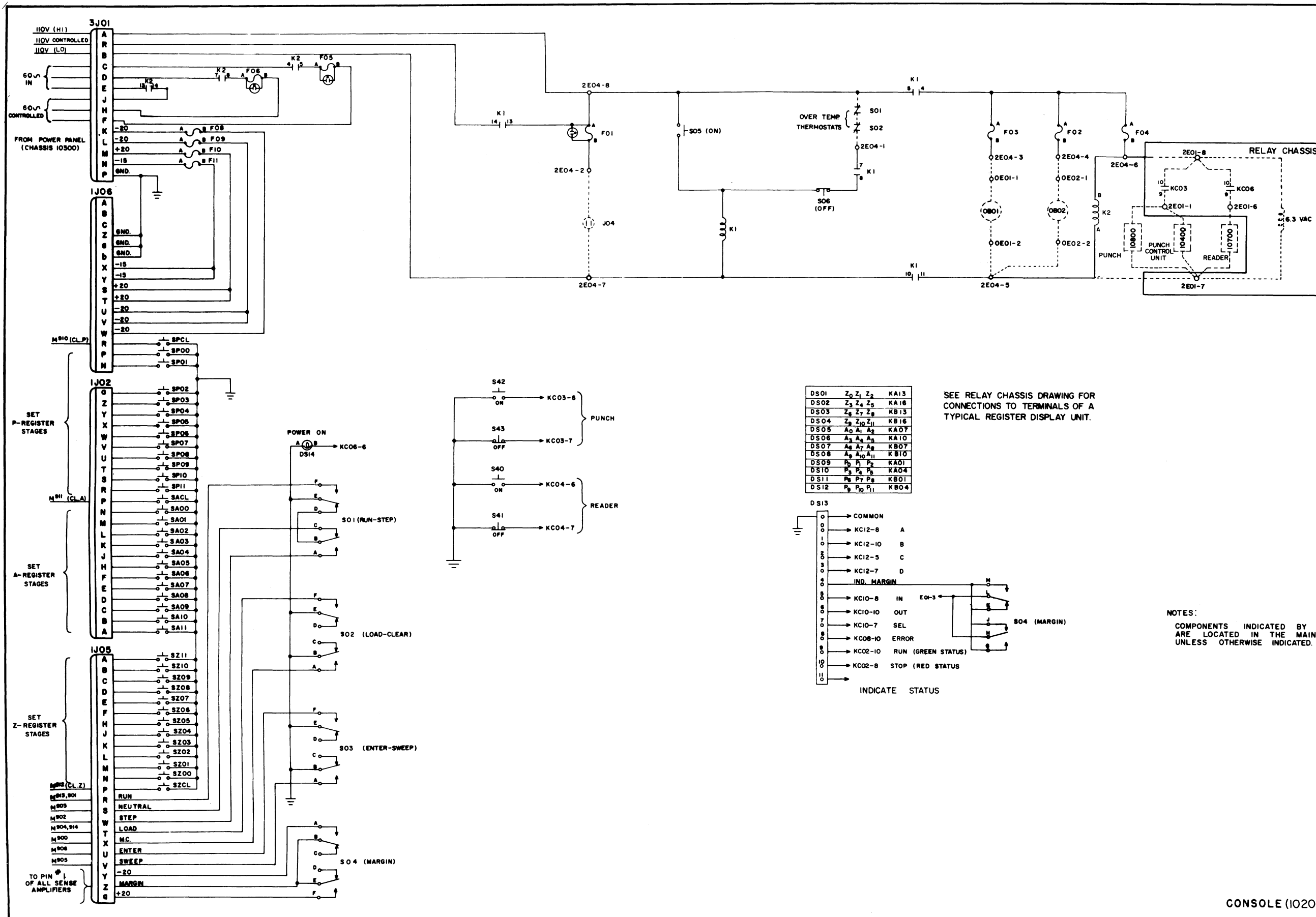




- 1 LEVEL 1 → A02-1
- 2 LEVEL 2 → A02-2
- 3 LEVEL 3 → A02-3
- 4 FEED HOLE → A01-1
- 5 LEVEL 4 → A02-4
- 6 LEVEL 5 → A03-1
- 7 LEVEL 6 → A03-2
- 8 LEVEL 7 → A03-3
- 9 LEVEL 8 → A03-4

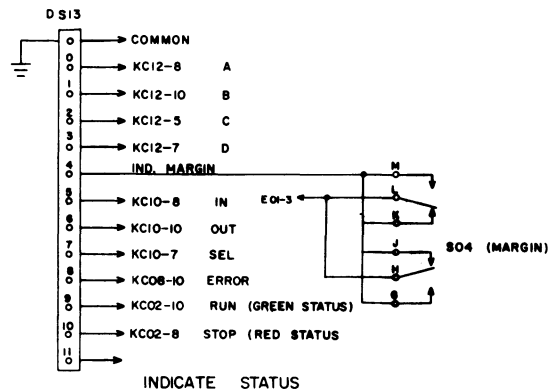


NOTE
ALL RESISTORS ARE 1/4 W ± 5%
UNLESS OTHERWISE INDICATED



DS01	Z ₀	Z ₁	Z ₂	KA13
DS02	Z ₃	Z ₄	Z ₅	KA16
DS03	Z ₆	Z ₇	Z ₈	KB13
DS04	Z ₉	Z ₁₀	Z ₁₁	KB16
DS05	A ₀	A ₁	A ₂	KA07
DS06	A ₃	A ₄	A ₅	KA10
DS07	A ₆	A ₇	A ₈	KB07
DS08	A ₉	A ₁₀	A ₁₁	KB10
DS09	P ₁	P ₂	P ₃	KA01
DS10	P ₄	P ₅	P ₆	KA04
DS11	P ₇	P ₈	P ₉	KB01
DS12	P ₁₀	P ₁₁	P ₁₂	KB04

SEE RELAY CHASSIS DRAWING FOR CONNECTIONS TO TERMINALS OF A TYPICAL REGISTER DISPLAY UNIT.



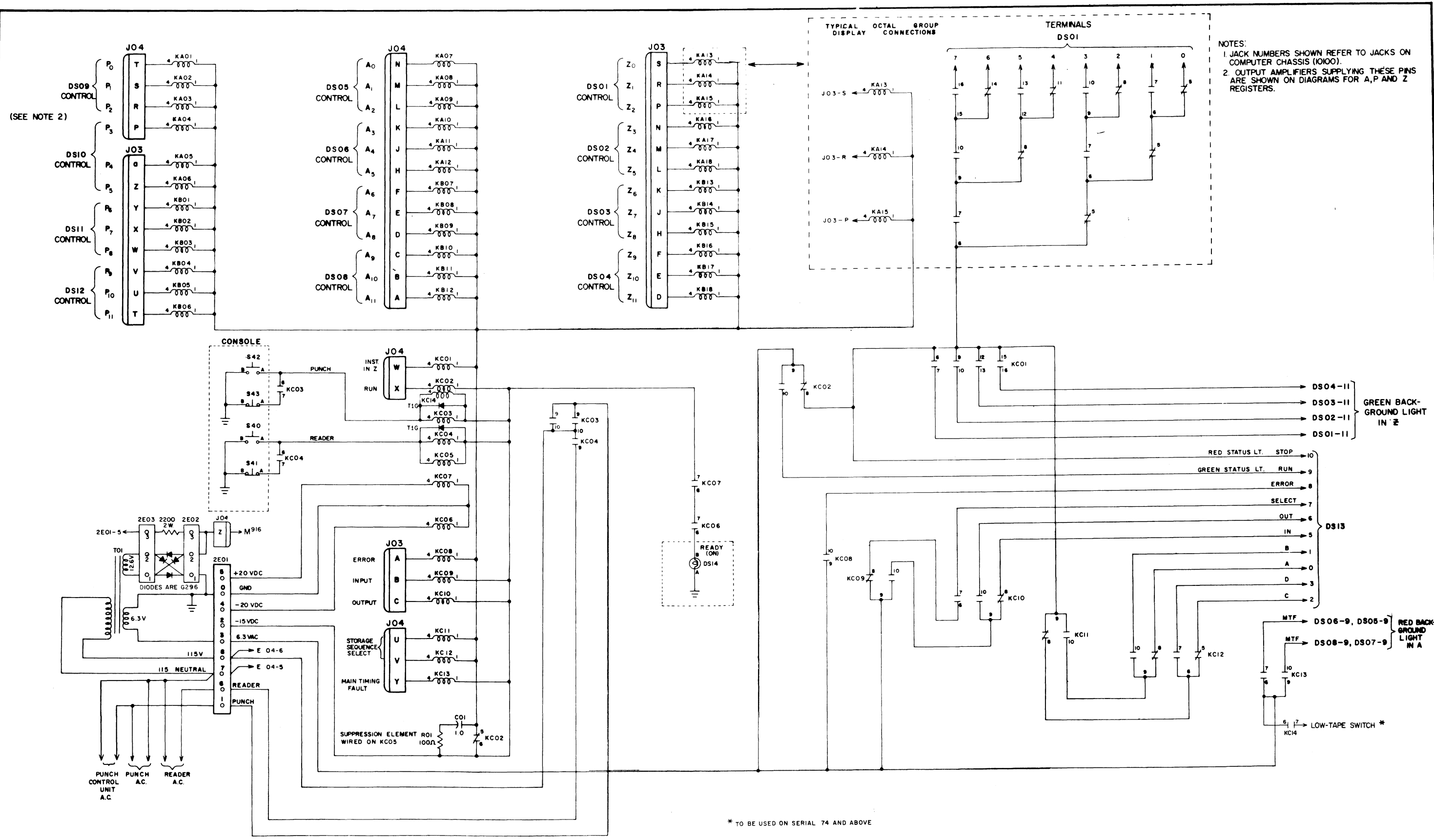
NOTES:
COMPONENTS INDICATED BY DASHED LINES ARE LOCATED IN THE MAIN CABINET UNLESS OTHERWISE INDICATED.

3064

CONSOLE (10200)

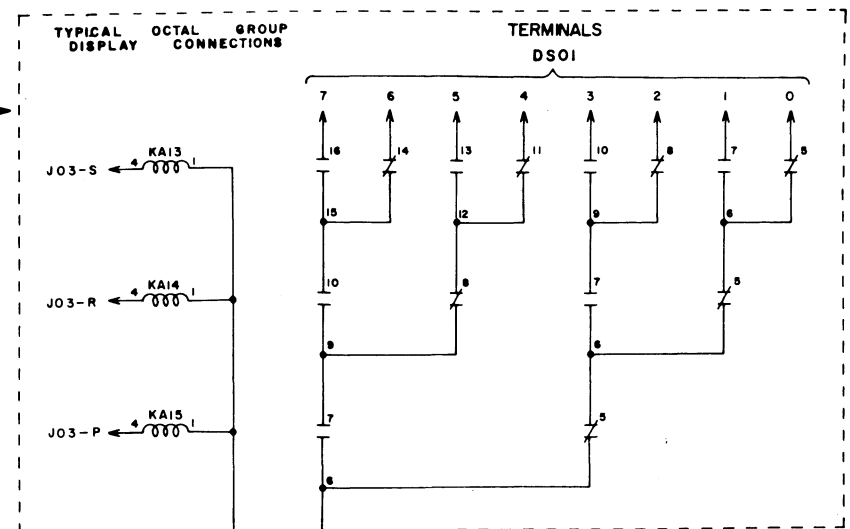
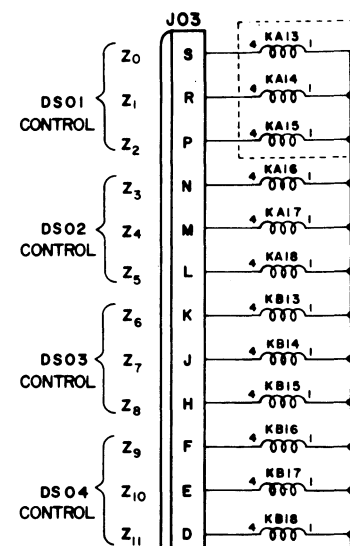
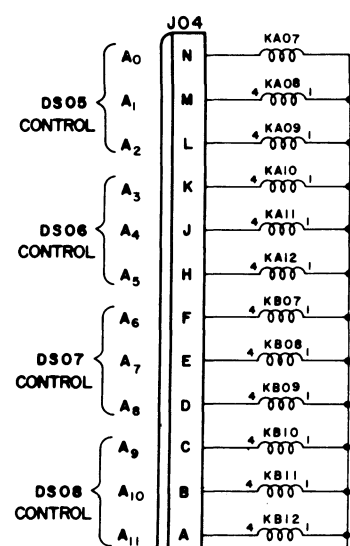
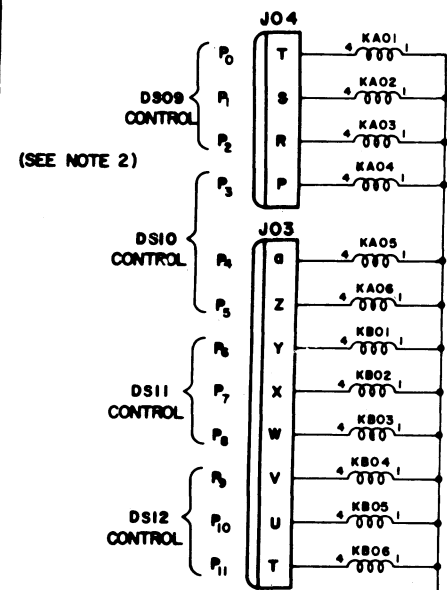
119820B

SERIAL 56 & UP 14

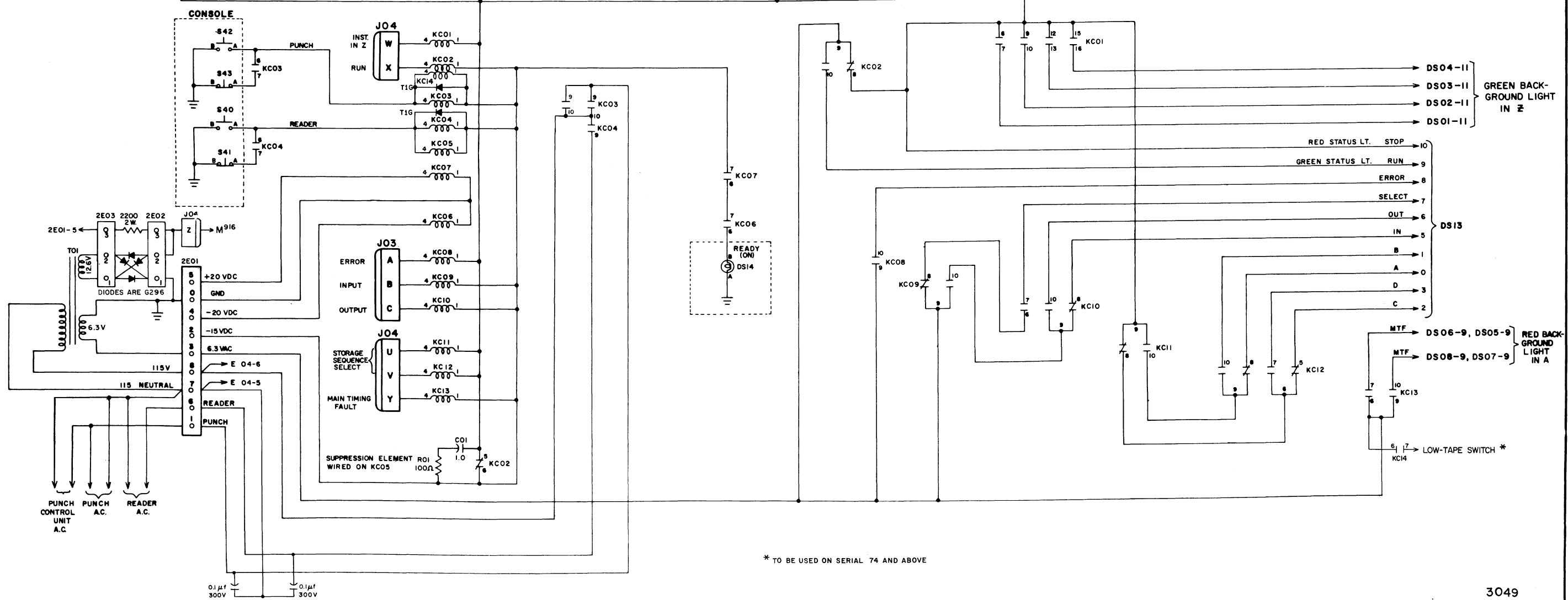


NOTES:
 1. JACK NUMBERS SHOWN REFER TO JACKS ON COMPUTER CHASSIS (1000).
 2. OUTPUT AMPLIFIERS SUPPLYING THESE PINS ARE SHOWN ON DIAGRAMS FOR A, P AND Z REGISTERS.

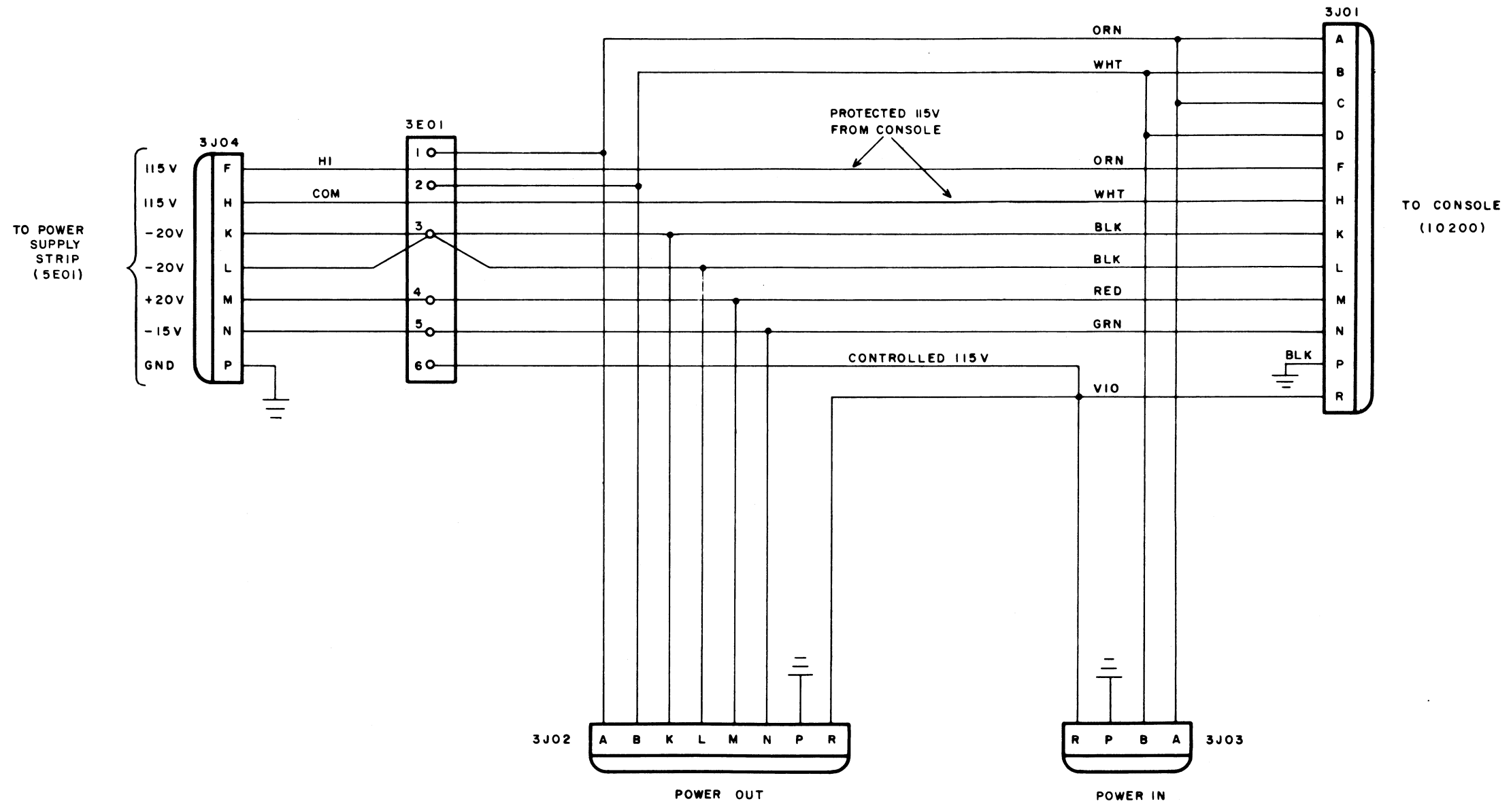
* TO BE USED ON SERIAL 74 AND ABOVE

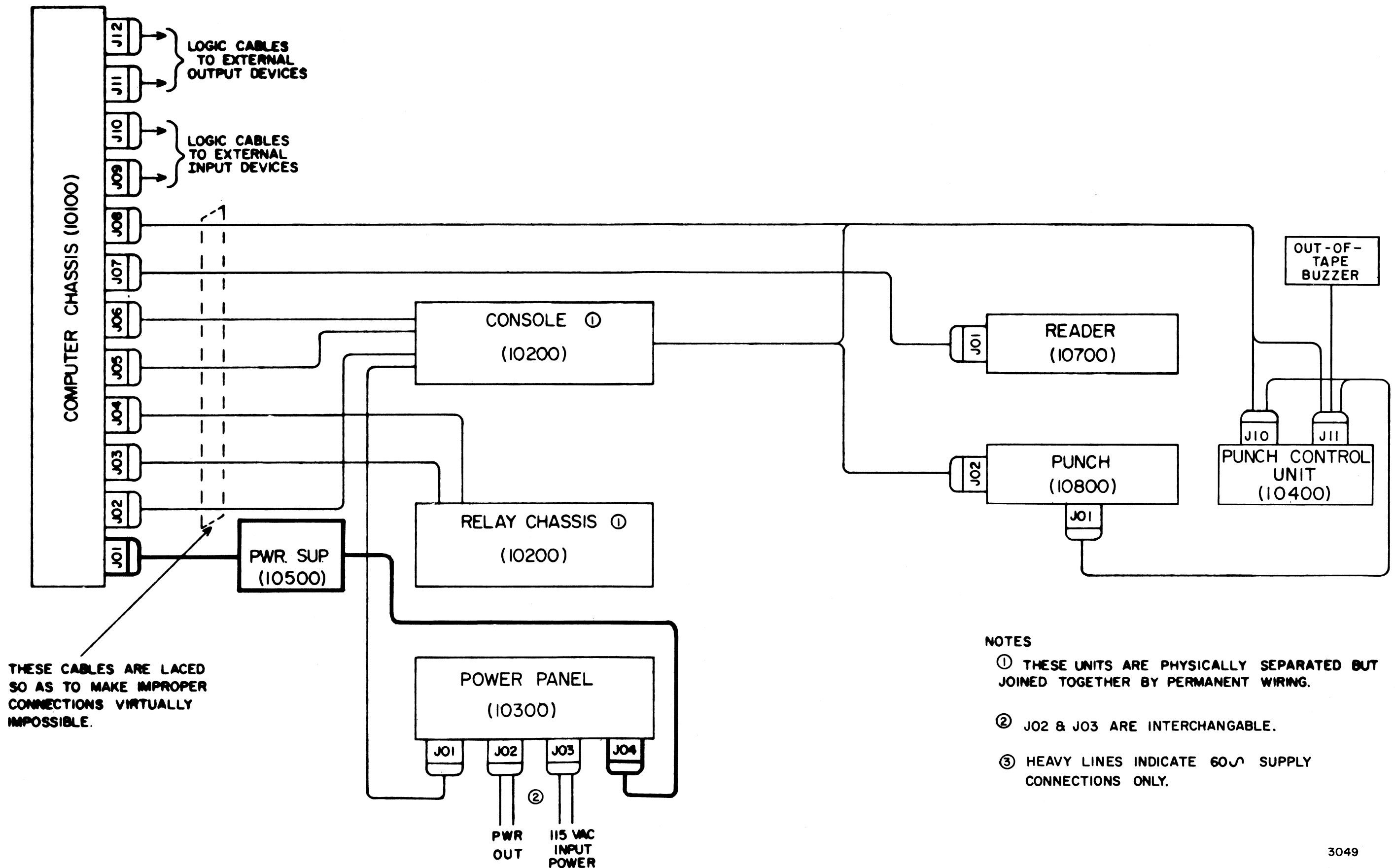


NOTES:
 1. JACK NUMBERS SHOWN REFER TO JACKS ON COMPUTER CHASSIS (10100).
 2. OUTPUT AMPLIFIERS SUPPLYING THESE PINS ARE SHOWN ON DIAGRAMS FOR A, P AND Z REGISTERS.

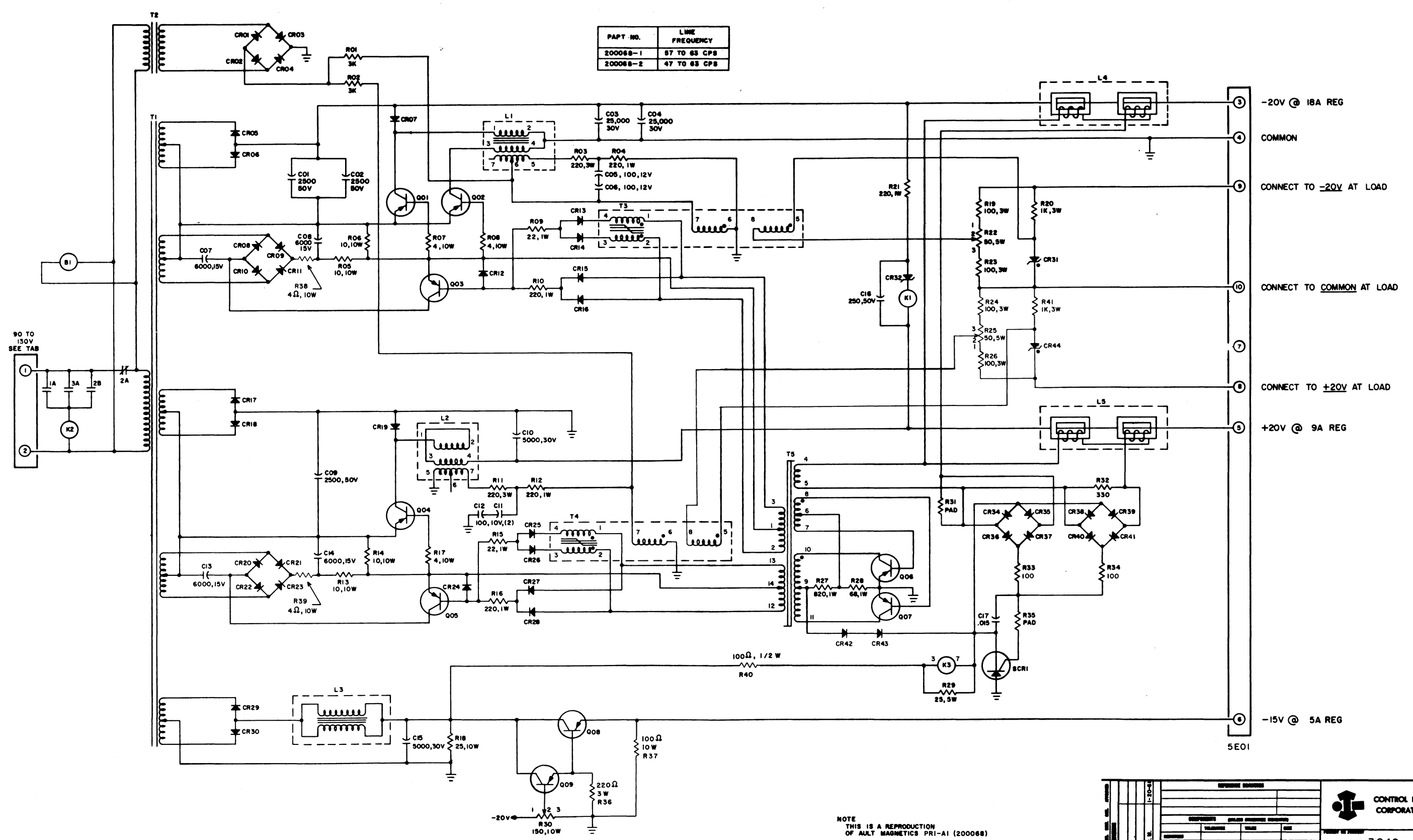


* TO BE USED ON SERIAL 74 AND ABOVE





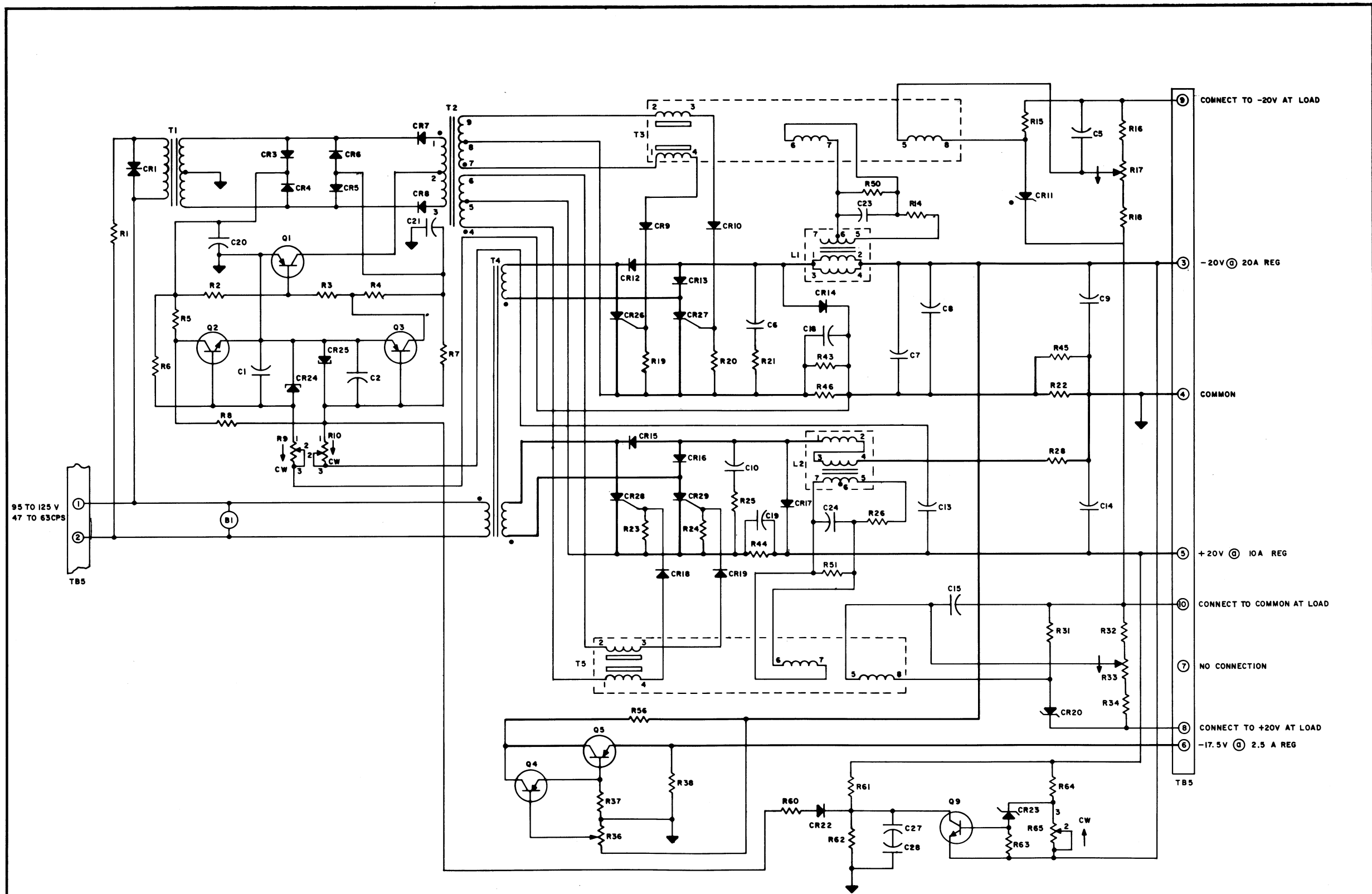
PART NO.	LINE FREQUENCY
200068-1	57 TO 63 CPS
200068-2	47 TO 63 CPS



90 TO 130V
SEE TAB

NOTE
THIS IS A REPRODUCTION
OF AULT MAGNETICS PRI-A1 (200068)
USE THROUGH 160 SERIAL 68 ONLY

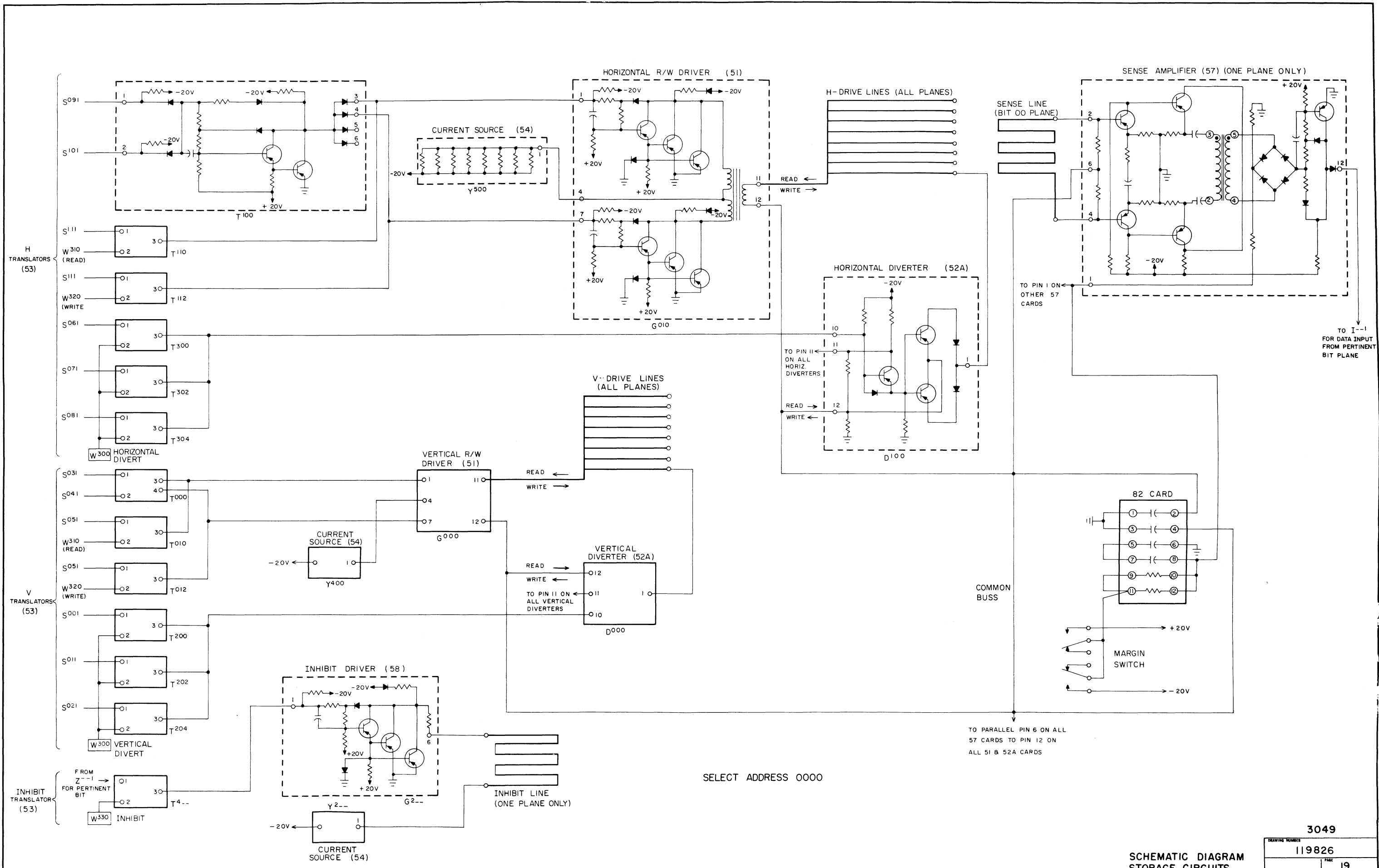
CONTROL DATA CORPORATION	
3049	
119822	F
60 CPS REGULATED POWER SUPPLY	ECO 26 18.0



CONTROL DATA
DEVELOPMENT
DIVISION

TITLE
**POWER SUPPLY -
AULT SCHEMATIC - PRI-C2
(200475)**

EQUIPMENT (SERIAL 69 160-B AND ABOVE)	
SIZE C	DRAWING NO. 60007000
SHEET	REV. F
PAGE 18.1	



3049

DRAWING NUMBER	119826
PAGE	19

**SCHEMATIC DIAGRAM
STORAGE CIRCUITS**

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MANUAL TITLE 160 COMPUTER CUSTOMER ENGINEERING DIAGRAMS

PUBLICATION NO. 60007000 REVISION _____

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MANUAL TITLE 160 COMPUTER CUSTOMER ENGINEERING DIAGRAMS

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